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/ Getting Started with the TJA1103EVB Evaluation Board

# Getting Started with the TJA1103EVB Evaluation Board

This page will guide you through the process of setting up and using the TJA1103EVB board.

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## Out of the Box

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state-of-the-art systems.

This page will guide you through the process of setting up and using the TJA1103EVB board.

#### **1.1 Kit Content and Packing List**

The TJA1103EVB contents include:

- Board: TJA1103EVB rev B
- Cable: UTP with 2x MATEnet connectors

### 1.2 Additional Hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this board.

- Cable: USB-A to Micro-USB for power supply option A and USB communication to PHY
- Power adapter: 5.0 V to 15 V DC, min. 250 mA, 2.1 mm coaxial power connector for power supply option B

#### 1.2 Software

The software used to communicate to the board via USB can be downloaded from NXP's website.

The software provides easy access to all settings within the PHY allowing interaction with all function modules. It is designed in such a way that basic functionality can be used via simple self explanatory dialogs and controls while at the same time giving access to all available registers, therefore not restricting the user to some predefined examples.

The following functions are supported by specifically guided dialogs:

- xMII / MDI configuration
- PHY status
- Loopback / test mode configuration
- TC10 wake/sleep
- BIST (internal frame generator/checker)
- FUSA (functional safety)

In addition, the following dialogs allow generic access:

- Global SMI access (PHY-address, register address and optional MMD (clause 45) configurable)
- Per-PHY SMI access (PHY-address predefined, register names automatically resolved)
- Per-PHY register table (interactive register description similar to data sheet with additional live view option)

Step #2 - Get to Know the Hardware

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