



PSMN2R3-100SSE

N-channel 100 V, 2.3 mOhm MOSFET with enhanced SOA in LFPAK88

16 December 2022

Product data sheet

1. General description

N-channel enhancement mode MOSFET in a LFPAK88 package qualified to 175 °C. Part of Nexperia's "ASFETs for hotswap" portfolio, the PSMN2R3-100SSE delivers very low R_{DSon} and a very strong linear-mode (SOA) performance in a high-reliability copper-clip LFPAK88 package.

PSMN2R3-100SSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn-on, low R_{DSon} to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- LFPAK88 package for applications that demand the highest performance and reliability

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	255	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	341	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	1.8	2.28	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 14 ; Fig. 13	8	27	62	nC
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13	80	161	242	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 82\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 137\text{ μs}$; Fig. 4	[1]	-	732	mJ

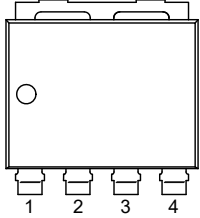
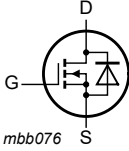
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Source-drain diode							
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; Fig. 18	[2]	-	68	-	nC

[1] Protected by 100% test

[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFLPAK88 (SOT1235)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN2R3-100SSE	LFLPAK88	plastic, single-ended surface-mounted package (LFLPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R3-100SSE	X2E3S10S

8. Limiting values

Table 5. Limiting values

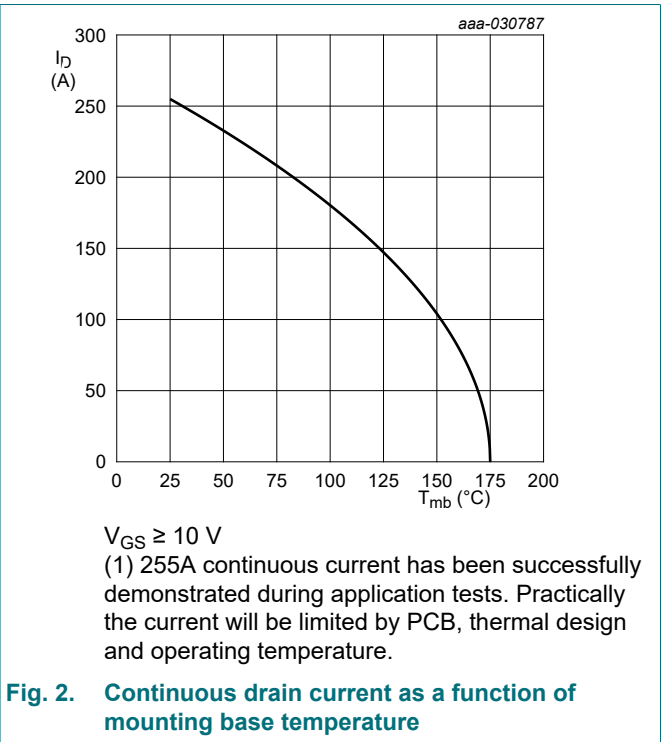
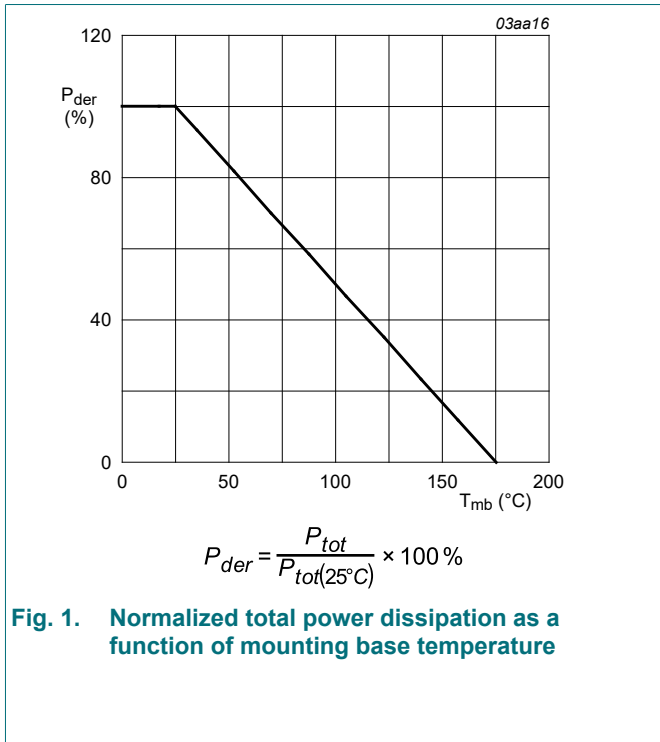
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	341	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	255	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	180	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	1020	A
T_{stg}	storage temperature		-55	175	°C

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Symbol	Parameter	Conditions	Min	Max	Unit
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	255	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	1020	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 82\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 137\text{ }\mu\text{s}$; Fig. 4	[1]	-	732 mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 100\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[1]	-	82 A

[1] Protected by 100% test



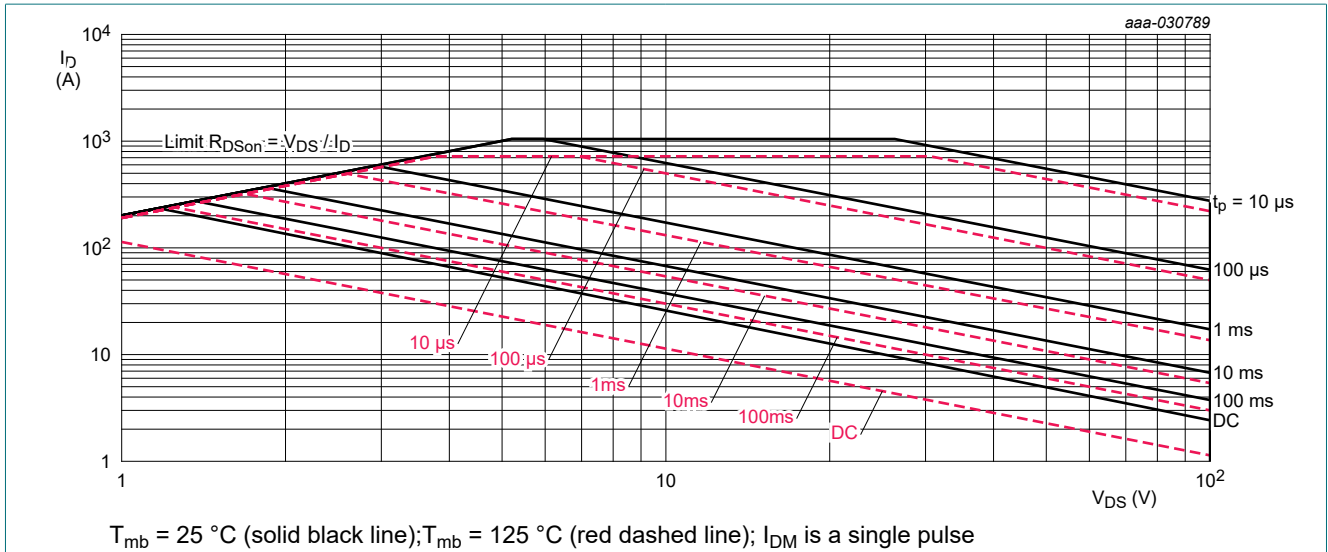


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

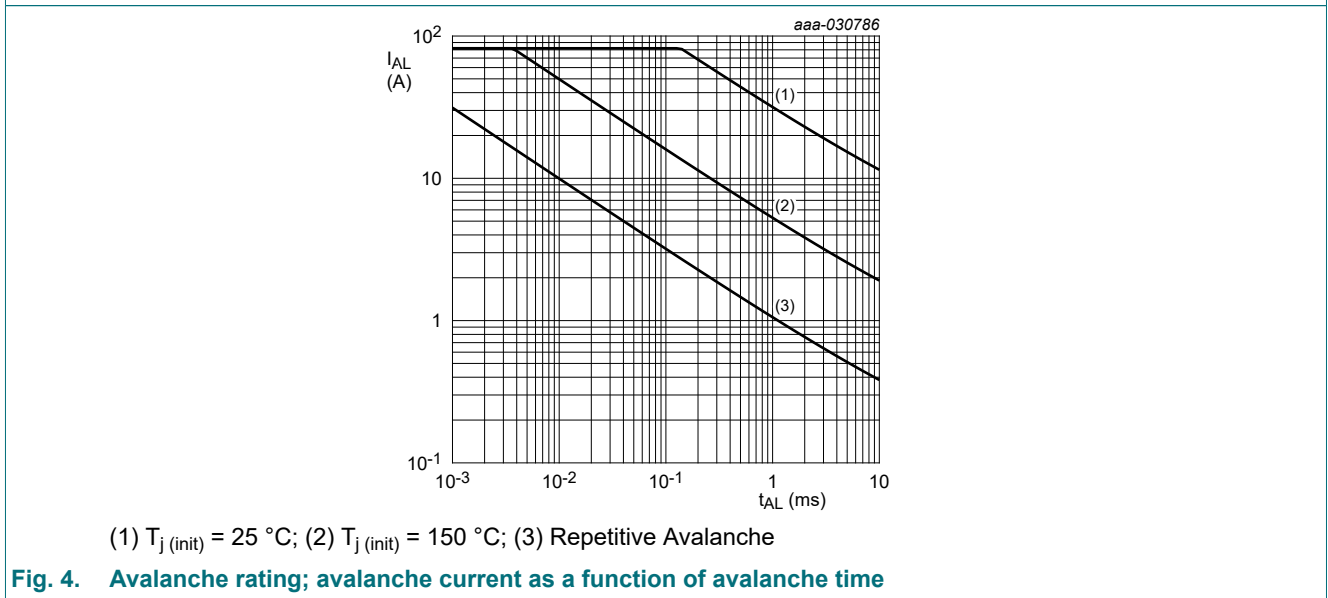


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.2	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	35	-	K/W
		Fig. 7	-	70	-	K/W

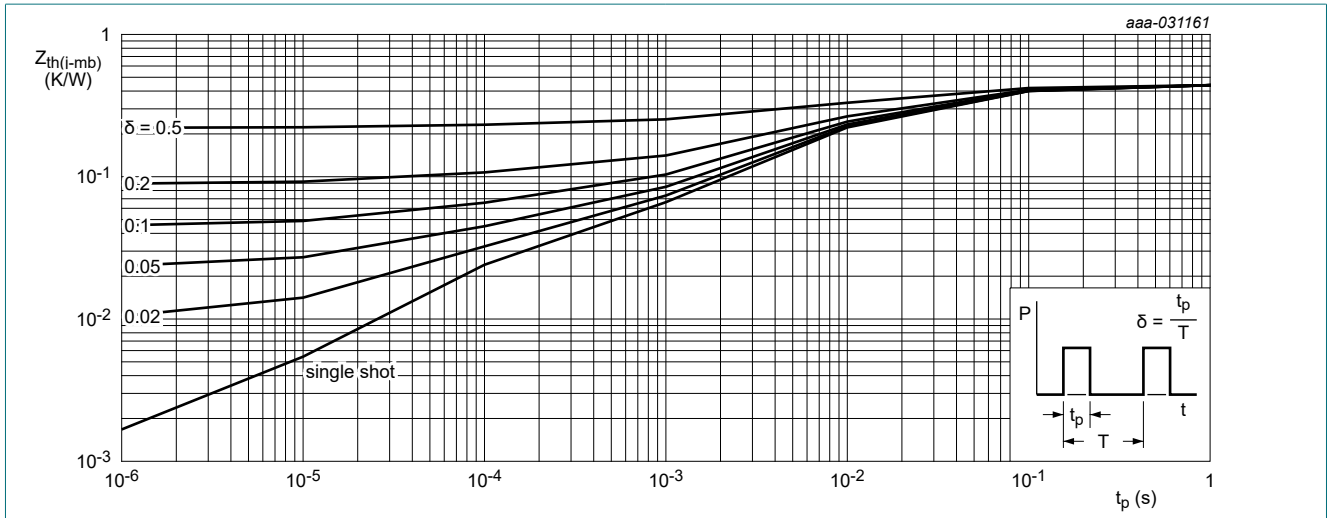
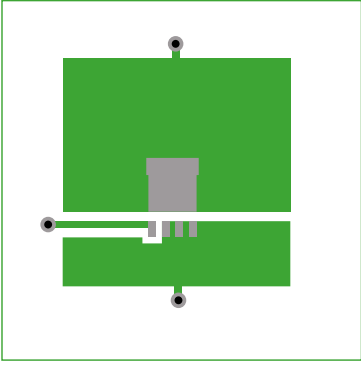
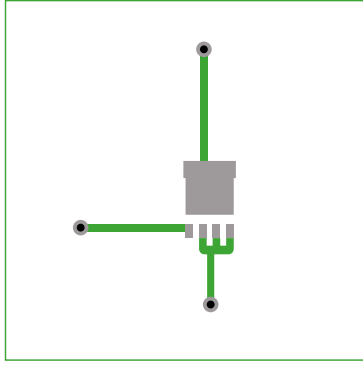


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



aaa-029383

Copper square 25.4 mm x 25.4 mm; 70 μm thick on FR4 board



aaa-029384

70 μm thick copper on FR4 board

Fig. 6. PCB layout for resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	2	2.6	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.6	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-6.2	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.1	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	20	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 11	-	1.8	2.28	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 100 °C; Fig. 12	-	2.9	3.6	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 12	-	3.7	5.2	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C	0.7	1.4	2.8	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 13	80	161	242	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; Fig. 14 ; Fig. 13	-	84	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 13	32	54	76	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	34	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	20	-	nC
Q _{GD}	gate-drain charge		8	27	62	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V; Fig. 14 ; Fig. 13	-	4.7	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 0.5 MHz; T _J = 25 °C; Fig. 16	7380	12300	17200	pF
C _{oss}	output capacitance		1600	2670	4300	pF
C _{rss}	reverse transfer capacitance		4	36	94	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω	-	41	-	ns
t _r	rise time		-	41	-	ns
t _{d(off)}	turn-off delay time		-	88	-	ns
t _f	fall time		-	54	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 17	-	0.8	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; Fig. 18	-	56	-	ns
Q _r	recovered charge		[1]	68	-	nC

[1] includes capacitive recovery

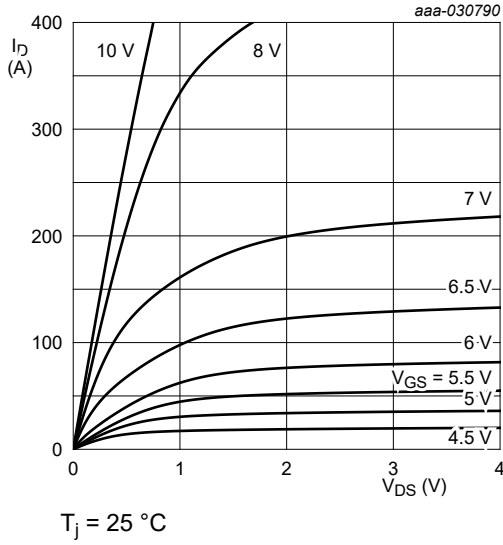


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

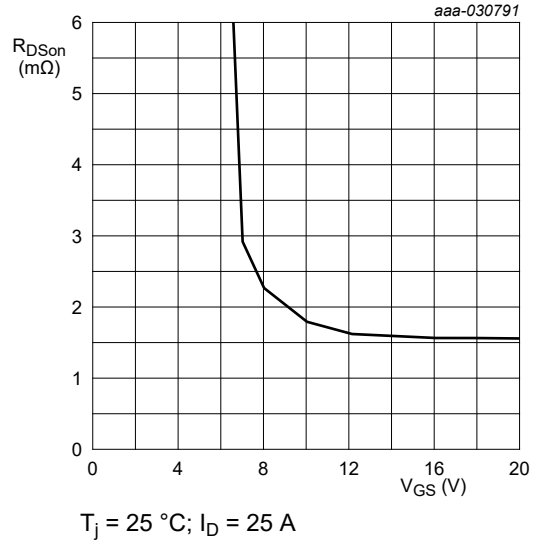


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

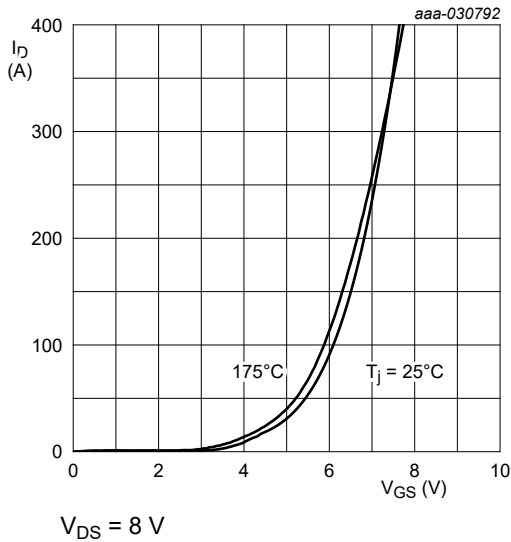


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

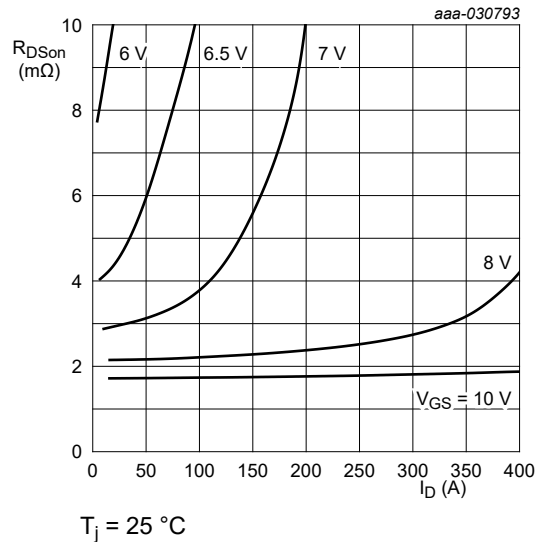
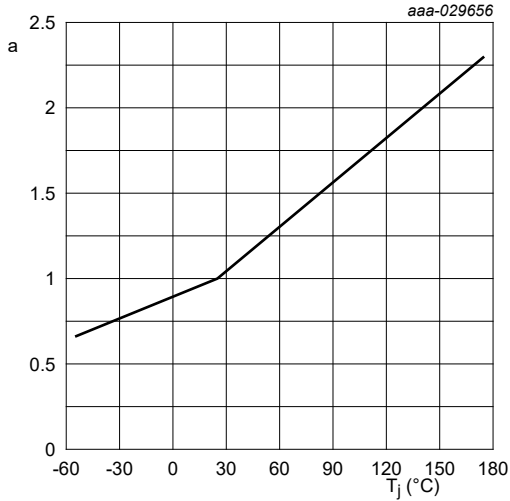


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

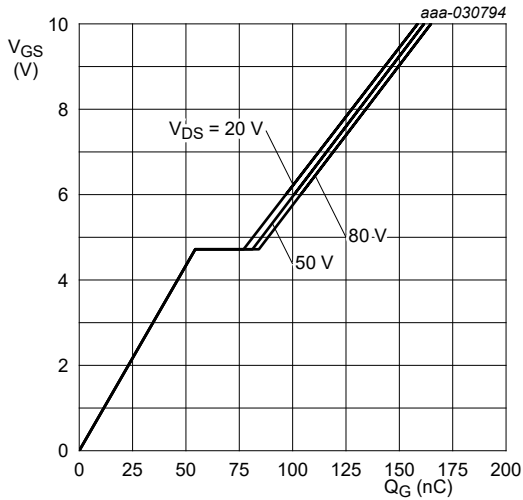


$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



Fig. 13. Gate charge waveform definitions



$T_j = 25^{\circ}C; I_D = 25 A$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

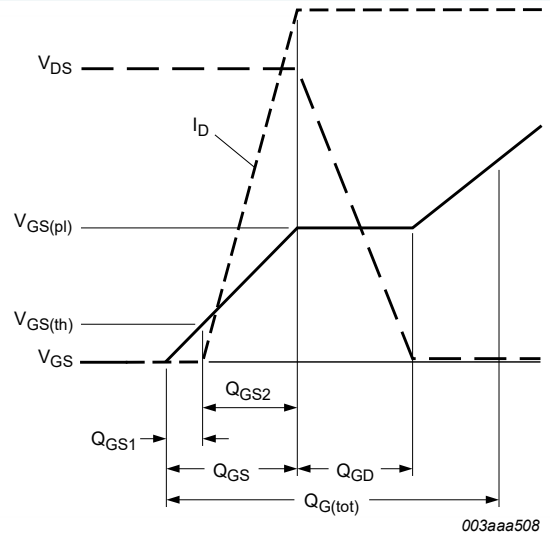
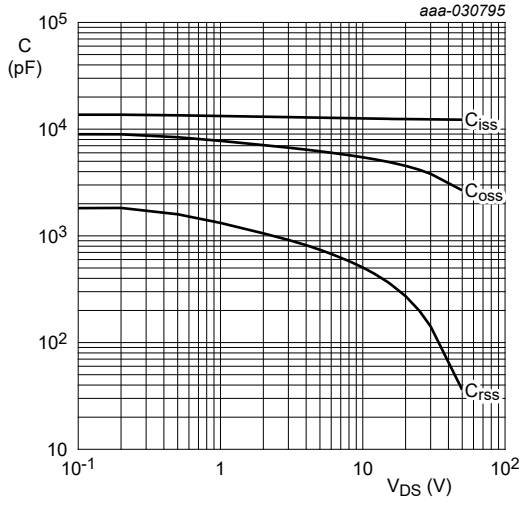
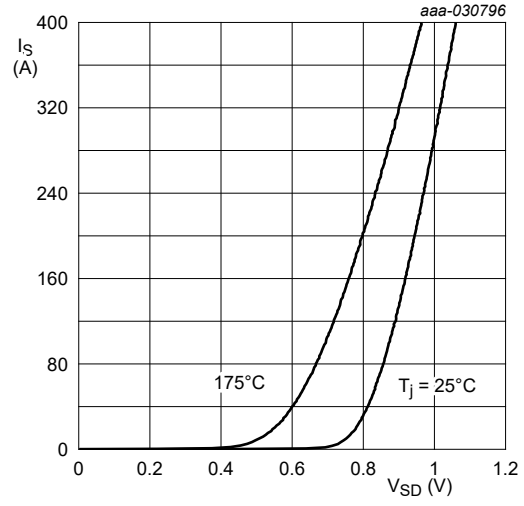


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$ V; $f = 1$ MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0$ V

Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

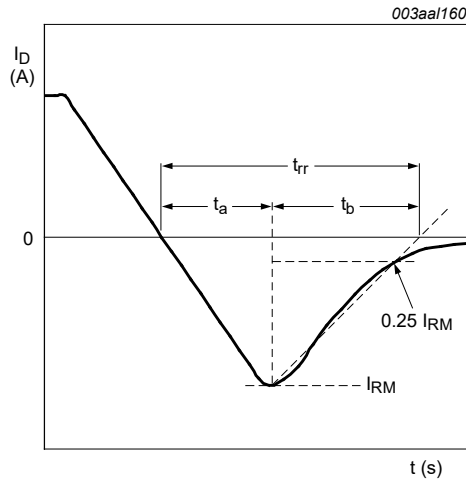


Fig. 18. Reverse recovery timing definition

11. Package outline

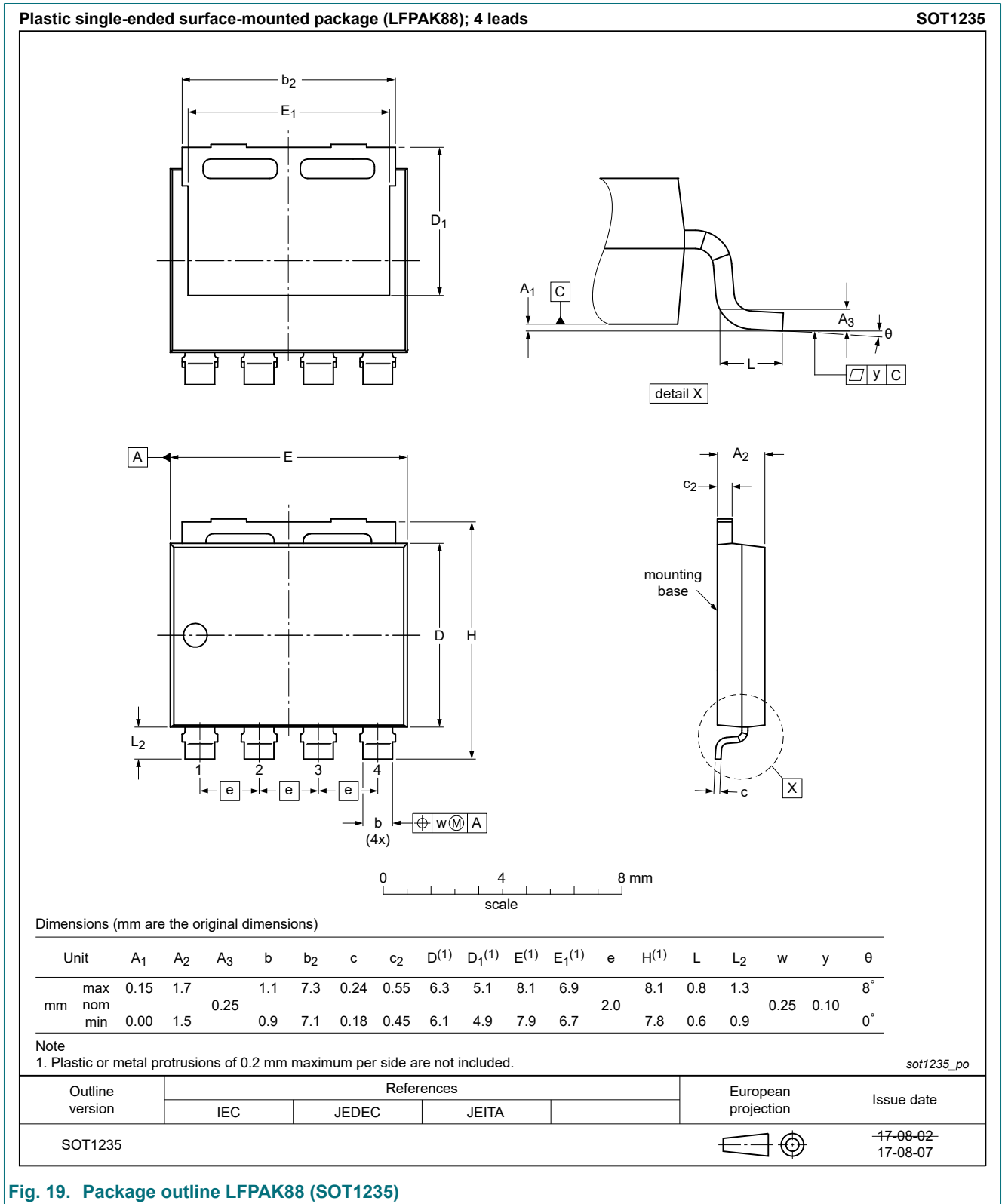


Fig. 19. Package outline LPAK88 (SOT1235)

12. Soldering

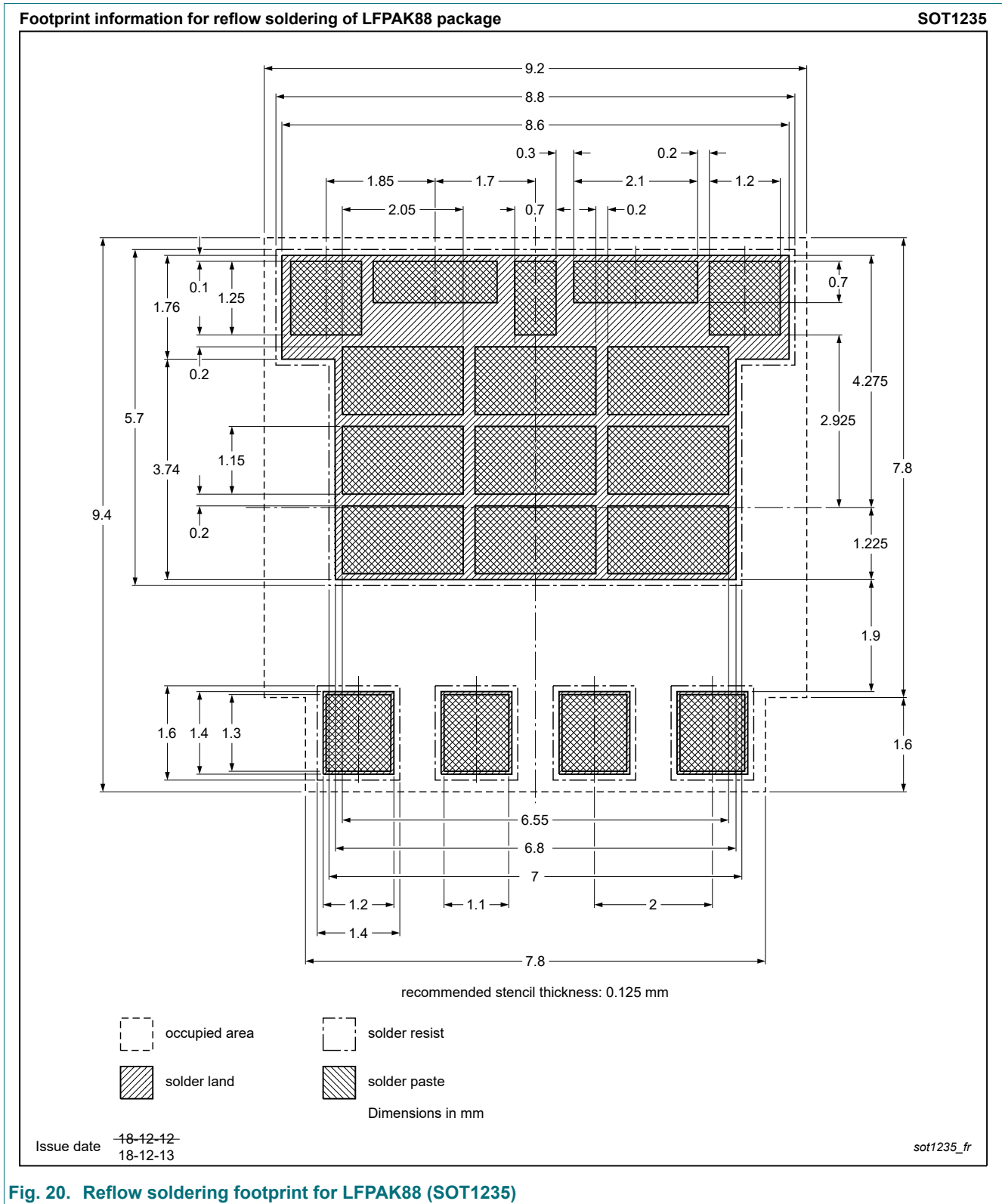


Fig. 20. Reflow soldering footprint for LPAK88 (SOT1235)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 16 December 2022
