OXFORD SEMICONDUCTOR

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EV-OXU200-PCI and EV-OXU200 Evaluation Board User Guide

Oxford Semiconductor, Inc.
1900 McCarthy Boulevard, Suite 210
Milpitas, CA 95035
USA

http://www.oxsemi.com

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Contents

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Preface

This manual documents the EV-OXU200-PCI and EV-OXU200 Evaluation Board hardware.

Revision Information

Table I documents the revisions of this manual

Table I Revision Information

Revision	Modification
Feb 2007	First publication
Mar 2007	Added the Certified USB logo to the cover page

Typographic Conventions

In this manual, the conventions listed in Table II apply.

Table II Typographic Conventions

Convention	Meaning
Italic Letters With Initial Capital Letters	A cross-reference to another publication
`Courier Font`	Software code, or text typed in via a keyboard
1, 2, 3	A numbered list where the order of list items is significant
■	A list where the order of items is not significant
"Title"	Cross-refers to another section within the document
	Significant additional information

Ordering Information

The following boards are available:

- EV-OXU200-PCI Evaluation Board (EV-OXU200-PCI-120)
- EV-OXU200 Evaluation Board (EV-OXU200-120)
- PCI104 Bridge Board (TDPCI104-1000-01)

Contacting Oxford Semiconductor

See the Oxford Semiconductor website (http://www.oxsemi.com) for further details about Oxford Semiconductor devices, or email sales@oxsemi.com.

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Chapter 1

EV-OXU200-PCI

Overview

The EV-OXU200-PCI Evaluation Board is a system for OXU200 customer evaluations and internal software development in the PC environment. The EV-OXU200-PCI Evaluation Board allows the user to install and use the EV-OXU200 in any PCI-based computer. Application software running on the system has access to the OXU200 via the PCI memory space.

The EV-OXU200-PCI Evaluation Board is a two-board combination of the following:

- An EV-OXU200 Evaluation Board
- A 33 MHz, 32-bit PCI Bridge Board, the PCI104

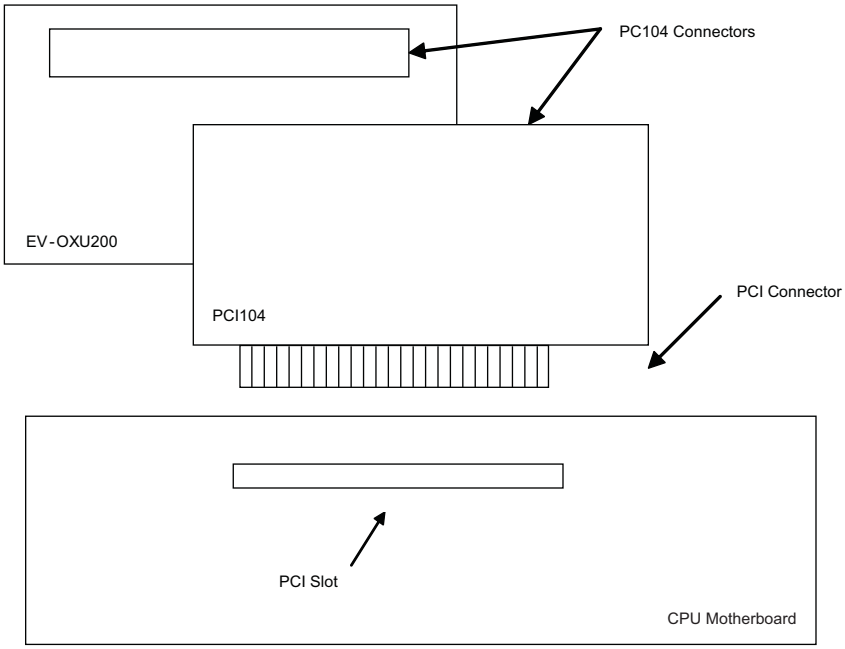
The EV-OXU200 Evaluation Board contains the OXU200 and all the USB-specific hardware.

The PCI104 Bridge Board contains a PCI-to-local-bus bridge chip that bridges the PCI bus to the OXU200. Power and control signals to the PCI bus are maintained by the PCI bridge chip, while initialization and configuration of the PCI bridge chip is maintained by the on-board serial EEPROM.

Figure 1-1 illustrates the orientation of the two boards. The combined boards are approximately one inch thick and require space for two PCI devices, but only one PCI slot. The OXU200 peripheral USB connector is accessible through the opening in the computer case.

Chapter 2 describes the EV-OXU200 Evaluation Board. Chapter 3 describes the PCI104 Bridge Board. For complete information about the OXU200 device, see the *OXU200 Hardware Reference Manual*.

Figure 1-1 EV-OXU200-PCI System Board Orientation



PCI Operation

Every PCI implementation has a PCI configuration space, where the PCI configuration registers are found. PCI configuration registers are accessed with read/write to configuration space, which is separate from memory and I/O space. Table 1-1 lists the standard PCI configuration register space for all PCI functions on the PCI bus.

Table 1-1 Standard PCI Configuration Register Space

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID		Vendor ID		00h
Status Register		Command Register		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Register 0 (BAR 0)				10h
Base Address Register 1 (BAR 1)				14h
Base Address Register 2 (BAR 2)				18h
Base Address Register 3 (BAR 3)				1Ch
Base Address Register 4 (BAR 4)				20h
Base Address Register 5 (BAR 5)				24h
CardBus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capabilities Pointer	34h
Reserved				38h
Max Latency	Min Grant	Interrupt Pin	Interrupt Line	3Ch

The PCI104 can be identified on the PCI bus during enumeration by the following PCI configuration registers:

Table 1-2 PCI Configuration Registers

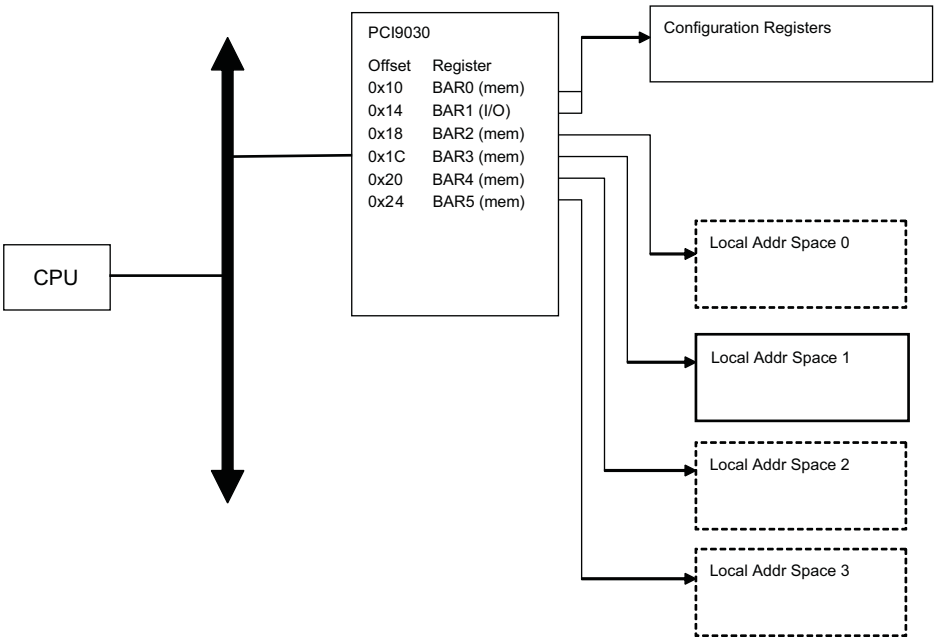
Register	Power-On Value
Vendor ID	192Eh
Device ID	016Bh
Revision	0001h
Class Code	0680h
Subsystem ID	016Bh
Subsystem Vendor ID	192Eh

Most operating systems provide functions for finding devices on the PCI bus. These functions typically key off the Vendor and Device IDs, or the Class Code. Because the Class Code for the PCI104 appears as a PCI Bridge with sub class code “other”, the search should be keyed to the Vendor and Device IDs.

Configuration

The EV-OXU200-PCI has two memory mapped register spaces and one I/O mapped register space. The address locations of the various spaces are determined by the Base Address Registers of the PCI configuration registers. Base Address Register 0 (BAR0) of the PCI configuration registers contains the address of the memory mapped PCI bridge controller registers. BAR1 contains the I/O address for the same PCI bridge controller registers. The PCI bridge controller registers are mapped into both memory and I/O space, so that these registers can be accessed via memory accesses or I/O addressing. BAR3 contains the address of the memory mapped OXU200 registers. Figure 1-2 illustrates the register mappings within a PCI system.

Figure 1-2 PCI104 Register Mappings



The Base Address Registers are typically initialized by the system BIOS or by the operating system. Software generally does not have to manually set the addresses of the mapped locations, however, this is system dependent. If these registers are not initialized, the three spaces should be manually mapped into system memory and I/O space accordingly. Care must be taken to ensure no conflicts exist between the mapped regions and other devices on the PCI bus.

Serial EEPROM Registers

The PCI9030 PCI bridge controller provides an interface to program the attached serial EEPROM. The serial EEPROM should be pre-programmed with the default values in Table 1-3. The table is for informational purposes only. If the default values are modified, the behavior of the PCI104 will change.

Table 1-3 Serial EEPROM Registers

Serial EEPROM Offset	Description	Default
00h	PCI Device ID	016Bh
02h	PCI Vendor ID	192Eh
04h	PCI Status Register	0290h
06h	PCI Command Register	0003h
08h	PCI Class Code	0680h
0Ah	PCI Class Code / Revision Number	0001h
0Ch	PCI Subsystem ID	016Bh
0Eh	PCI Subsystem Vendor ID	192Eh
10h	MSB New Capability Pointer	0000h
12h	LSB New Capability Pointer	0040h

Table 1-3 Serial EEPROM Registers

Serial EEPROM Offset	Description	Default
14h	(Maximum Latency and Minimum Grant are not loadable)	0000h
16h	Interrupt Pin (Interrupt Line Routing is not loadable)	0100h
18h	MSW of Power Management Capabilities	4801h
1Ah	LSW of Power Management Next Capability Pointer / Power Management Capability ID	4801h
1Ch	MSW of Power Management Data /PMCSR Bridge Support Extension	0000h
1Eh	LSW of Power Management Control/Status	0000h
20h	MSW of Hot Swap Control/Status	0000h
22h	LSW of Hot Swap Next Capability Pointer / Hot Swap Control	4C06h
24h	PCI Vital Product Data Address	0000h
26h	PCI Vital Product Data Next Capability Pointer / PCI Vital Protocol Data Control	0003h
28h	MSW of Local Address Space 0 Range	0000h
2Ah	LSW of Local Address Space 0 Range	0000h
2Ch	MSW of Local Address Space 1 Range	FFFFh
2Eh	LSW of Local Address Space 1 Range	8000h
30h	MSW of Local Address Space 2 Range	0000h
32h	LSW of Local Address Space 2 Range	0000h
34h	MSW of Local Address Space 3 Range	0000h
36h	LSW of Local Address Space 3 Range	0000h
38h	MSW of Expansion ROM Range	0000h
3Ah	LSW of Expansion ROM Range	0000h
3Ch	MSW of Local Address Space 0 Local Base Address (Remap)	0000h
3Eh	LSW of Local Address Space 0 Local Base Address (Remap)	0000h
40h	MSW of Local Address Space 1 Local Base Address (Remap)	0000h
42h	LSW of Local Address Space 1 Local Base Address (Remap)	0001h
44h	MSW of Local Address Space 2 Local Base Address (Remap)	0000h
46h	LSW of Local Address Space 2 Local Base Address (Remap)	0000h
48h	MSW of Local Address Space 3 Local Base Address (Remap)	0000h
4Ah	LSW of Local Address Space 3 Local Base Address (Remap)	0000h
4Ch	MSW of Expansion ROM Local Base Address (Remap)	0010h
4Eh	LSW of Expansion ROM Local Base Address (Remap)	0000h
50h	MSW of Local Address Space 0 Bus Region Descriptor	0080h
52h	LSW of Local Address Space 0 Bus Region Descriptor	0000h
54h	MSW of Local Address Space 1 Bus Region Descriptor	4040h
56h	LSW of Local Address Space 1 Bus Region Descriptor	A040h
58h	MSW of Local Address Space 2 Bus Region Descriptor	0000h
5Ah	LSW of Local Address Space 2 Bus Region Descriptor	0000h
5Ch	MSW of Local Address Space 3 Bus Region Descriptor	0080h
5Eh	LSW of Local Address Space 3 Bus Region Descriptor	0000h

Table 1-3 Serial EEPROM Registers

Serial EEPROM Offset	Description	Default
60h	MSW of Expansion ROM Bus Region Descriptor	0000h
62h	LSW of Expansion ROM Bus Region Descriptor	0000h
64h	MSW of Chip Select 0 Base Address	0BFFh
66h	LSW of Chip Select 0 Base Address	FFC1h
68h	MSW of Chip Select 1 Base Address	0000h
6Ah	LSW of Chip Select 1 Base Address	4001h
6Ch	MSW of Chip Select 2 Base Address	0000h
6Eh	LSW of Chip Select 2 Base Address	0000h
70h	MSW of Chip Select 3 Base Address	0000h
72h	LSW of Chip Select 3 Base Address	0000h
74h	Serial EEPROM Write-Protected Address Boundary	0030h
76h	LSW of Interrupt Control/Status	0041h
78h	MSW of Target Response, Serial EEPROM, and initialization Control	0870h
7Ah	LSW of Target Response, Serial EEPROM, and initialization Control	0000h
7Ch	MSW of General Purpose I/O Control	0024h
7Eh	LSW of General Purpose I/O Control	9864h
80h	MSW of Hidden 1 Power Management Data Select	0000h
82h	LSW of Hidden 1 Power Management Data Select	0000h
84h	MSW of Hidden 2 Power Management Data Select	0000h
86h	LSW of Hidden 2 Power Management Data Select	0000h

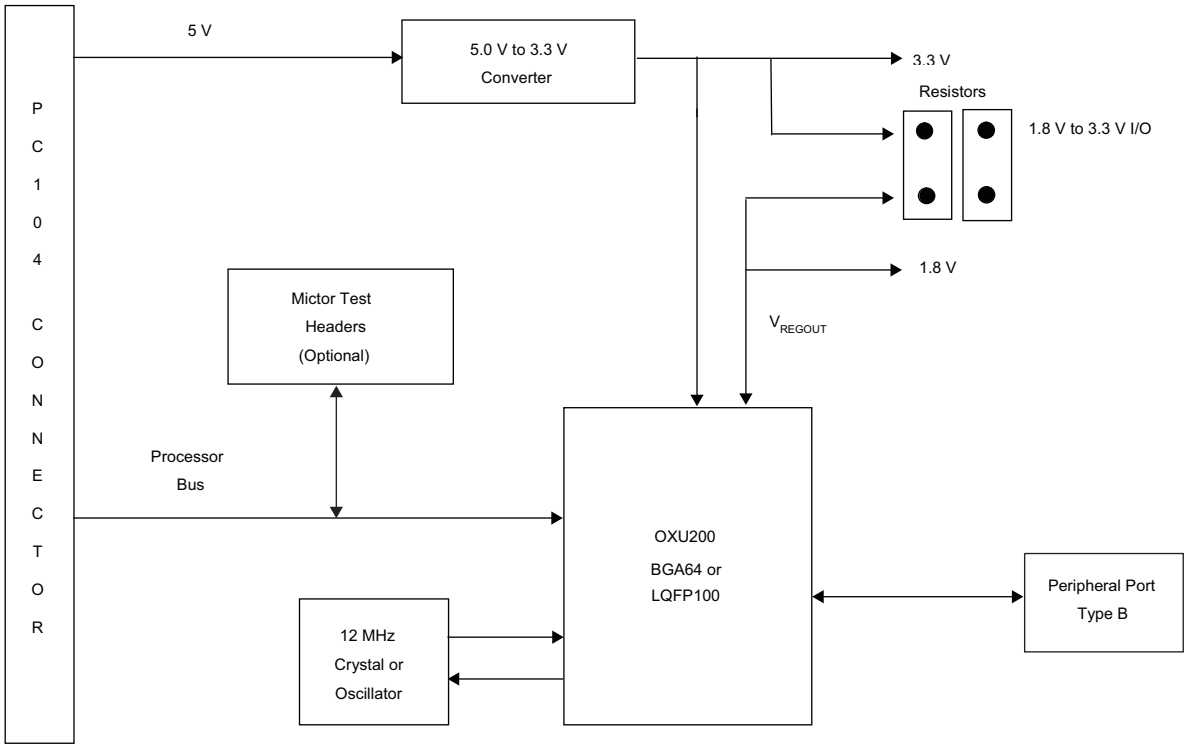
Chapter 2

EV-OXU200 Evaluation Board

Overview

This chapter describes the hardware operation and configuration options available for the EV-OXU200 in stand-alone mode. These options allow customers to directly connect the OXU200 to their embedded processor or CPU without going through a PCI bus. The use of this board without the PCI bridge card increases performance and allows driver development in real-world applications of the product. Figure 2-1 shows the EV-OXU200 block diagram.

Figure 2-1 EV-OXU200 Block Diagram



Board Operation Requirement

The EV-OXU200 requires a DC power source capable of supplying 5 V ± 10% at 1.0 A through a power switch.

Default Configurations

Zero-Ohm resistors are used to set the following factory default configurations:

- R1, R3 (0 Ω) populated to route 5 V from the PC104 connectors
- R30, R31 (0 Ω) populated, R29 (0 Ω) removed to use on-board 12 MHz crystal
- R28 (0 Ω) populated, R27 (0 Ω) removed to set V_{DDW} to 3.3 V I/O

Power Distribution

In the default mode, the EV-OXU200 receives all its power from the 5 V pins of the PC104 connector. The 5 V supply drives the 3.3 V DC regulator. Alternative power-supply options are described below.

The power for the core voltage ($V_{DD1.8}$ pins) comes from the OXU200's internal regulator. This regulator can also be selected to drive the 1.8 V I/O option for V_{DDW}.

5 V Power Supply

The EV-OXU200 5 V power is supplied by one of two sources:

1. From the PC104 connector 5 V pins: J2.D16, J3.B29, J3.B3 (default setting).
2. From an external power supply connected to JP5.3. To enable this mode, remove R1 and R3 (0 Ω). Protection circuitry is not provided.

3.3 V Power Supply

The EV-OXU200 3.3 V power is supplied by a 5 V-to-3.3 V DC regulator (U5).

1.8 V Core Power Supply

The EV-OXU200 1.8 V power is supplied by the internal regulator via V_{REGOUT}. No external power supply should be connected to drive 1.8 V or else chip damage will result.

3.3/1.8 V V_{DDW} Wide Range I/O Power Supply

The EV-OXU200 provides either 1.8 V or 3.3 V for V_{DDW}, the wide range power. The voltage is selected through the intallation or removal of resistors as described below. While the OXU200 allows any voltage in this range, any other value is customer specific and is not directly supported by this evaluation board. The EV-OXU200 V_{DDW} power is supplied by one of two sources:

1. From the 3.3 V power rail (default setting). Install R28 (0 Ω) and remove R27 (0 Ω).
2. From the OXU200's 1.8 V internal regulator. Install R27 (0 Ω) and remove R28 (0 Ω).

Oscillator Input

The EV-OXU200 uses a 12 MHz crystal at Y1 for the OXU200 OSC_1/OSC_2 clock source.

A 12 MHz oscillator can be soldered at the U6/U7 dual-footprint by the customer and used as the OXU200 clock source. To enable this mode, install R29 (0 Ω) and remove R31 (0 Ω). Also, remove R30 (0 Ω)because the OSC_2 pin must be floating in this configuration. Below are the oscillator part numbers that Oxford Semiconductor has used for internal design and testing. Other components meeting the OXU200 requirements may be used (see the *OXU210HP, OXU140CM, OXU121HP, and OXU200 External Crystal Selection* application note).

- 12 MHz crystal: Citizen America, HCM49-12.000MABJUT, 18 pF internal load (RoHS compliant)
- 12 MHz oscillator: Ecliptek, EH1345HSTS-12.000M, 50 ppm, 8-pin DIP (RoHS compliant)

OXU200 Reset

The /RESET pin of the OXU200 is brought out to the PC104 connector to allow control of the /RESET through a CPU GPIO. /RESET can also be asserted manually using the S1 switch.

D_P/D_M Signals

- Pads are provided for the D_P/D_M signals to enable use of an external ESD protection device. The pad locations are designated U2 on the schematic and circuit board. See the *OXU200 External ESD Protection* application note
- These traces are impedance controlled to 90 Ω ± 10%

V_{BUS} Over-Voltage Protection

Besides the ESD transient protection provided by the external ESD devices, the OXU200 V_{BUS} pin is also protected against steady-state voltages above 5.1 V (typical) by the voltage divider resistor (R32 = 390 Ω) and the Zener diode D2. When the OXU200 is connected to a host, the Zener diode protects the OXU200 from damage.

- Zener diode: ON Semiconductor® BZX84C5V1LT1G, 225 mW, 5.1 V breakdown

LEDs

The EV-OXU200 has the following LEDs to enable monitoring of the normal operation of the board:

- D5: 1.8 V Power Rail Indicator
- D3: 3.3 V Power Rail Indicator
- D4: 5.0 V Power Rail Indicator
- D1: Peripheral Port V_{BUS} Power Indicator

Mounting Holes

The EV-OXU200 board has four un-plated standoff holes, one near each corner of the board. Each hole is 0.146 inch in diameter. The placement matches the PCI104 PCI board which together make the EV-OXU200-PCI.

Test Points

The following test points are furnished on the EV-OXU200:

- Ground test points JP1, JP2, JP6, and JP7
- V_{BUS} 5 V test point TP1
- Power supplies 5 V (JP5), 3.3 V (JP4), 1.8 V (JP3), and V_{DDW} test point TP2

All the microprocessor signals are routed to Mictor connector J1. The Mictor connectors are not installed but can be obtained from
AMP/Tyco Electronics
Part Number: 2-5767004-2
Description: Receptacle, 38 positions, .025 vertical

Chapter 3

PCI104 Bridge Board

Overview

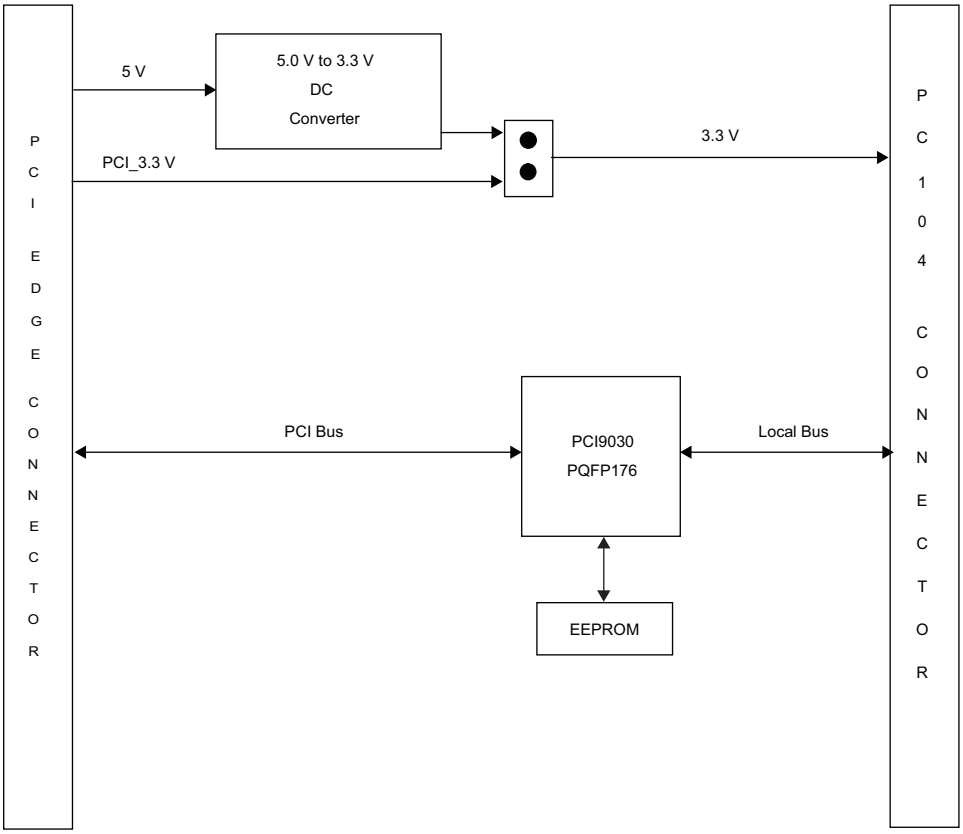
The PCI104 Bridge Board, measured at 5.55 in. (140.9 mm) by 3.00 in. (76.2 mm), can be employed to:

- Evaluate the Oxford Semiconductor OXU200 USB peripheral controller
- Run OXU200 demonstrations
- Develop user software for OXU200-based applications
- Serve as a subassembly in an OEM product to provide USB OTG and host controller functionality

While the EV-OXU200-PCI can be used to evaluate the OXU200, it will not result in optimal performance due to the long access times of the PCI bus. For optimal performance evaluation, the OXU200 should be placed directly on the system bus using the EV-OXU200 board as described in Chapter 2 .

The PCI104 board bridges between the PCI bus and the OXU200 local bus. The local bus is routed out to the standard PC104 connectors (J1 and J2). The EV-OXU200 interfaces to the PCI104 Bridge Card via these three female connectors. Another proprietary, non-PC104 connector (J3) was added to support a 32-bit interface and additional signals not included in the PC104 signal definition. Figure 3-1 shows the PCI104 block diagram.

Figure 3-1 PCI104 Bridge Board



The PCI104 board uses the PCI9030 bridge device. The PCI configuration registers are stored in an on-board EEPROM.

Power Distribution

The PCI104 board receives its 5 V power from the standard PCI bus edge connector (U2 – eight 5 V pins). The 5 V supply is routed directly to the EV-OXU200 via the PC104 connectors (J1.D16, J2.B3, J2.B29).

The PCI104 board 3.3 V power is supplied by one of two sources:

1. 5.0 V-to-3.3 V DC regulator (U1). Install jumper on JP2 pin 1-2, 3-4 (default setting) and remove 5-6 and 7-8.
2. The standard PCI bus edge connector (U2 – twelve 3.3 V pins). Install jumper on JP2 pin 5-6, 7-8 and remove 1-2 and 3-4.

Local Bus Configuration

The PCI9030 local bus is connected directly to the EV-OXU200 board via the PC104 connectors. Refer to the *PCI9030 Data Book* for a detailed explanation of its operation.

PCI9030 CS1L chip select is routed to the EV-OXU200. Register Space 1 of the PCI9030 controls CS1L. The number values programmed into Space 1 registers of the EEPROM are shown below. Changing values in the EEPROM requires an application from PLX operating across the PCI bus. Space 1 has 16-bit local and PCI space and contains 32 Kb memory space size. There is no prefetch on space 1.

- Space 1 Range 0xFFFF_8000
- Space 1 Remap 0x0000_0001
- Space 1 Descriptor 0x4040_A040
- Space 1 Base Address 0x0000_4001
- Space 1 Initialization Control 0x0024_9864

The local timing is one WAIT state for READs (address-to-data) and one for WRITEs (address-to-data) to make the PCI104 backwards compatible with previous Oxford Semiconductor chips. The other WAIT states are: zero RD (data-to-data), one RD/WR (data-to-address), zero WR (data-to-data), and one WR cycle hold. An optimum bus access will not create a significant increase in performance in the EV-OXU200-PCI system. For better performance evaluation, the OXU200 should be embedded directly on the system bus using the EV-OXU200 board.

Local Bus Speed

LCLK, the local bus clock, operates at frequencies up to 60 MHz and is asynchronous to the PCI bus clock, BCLK. BCLK is routed back into LCLK, setting the default local bus speed at 33 MHz.

An oscillator up to 60 MHz can be soldered at the U4/U5 dual-footprint by the customer to increase the local bus speed. R10 (33 ohms) must be installed and R11 removed in this configuration. More WAIT states may have to be added to meet the OXU200 interface timing when increasing the local bus frequency.

LEDs

The PCI104 has two LEDs to enable verification of the normal operation of the board.

- D1: 3.3 V Power Rail Indicator
- D2: 5.0 V Power Rail Indicator

Mounting Holes

The PCI104 board has four un-plated standoff holes, one near each corner of the board. Each hole is 0.146” in diameter. The placement matches the EV-OXU200 evaluation board which together make the EV-OXU200-PCI.

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Chapter 4

Schematics

Overview

This chapter provides the EV-OXU200 and PCI104 schematics. The EV-OXU200 uses a dual footprint so either the LQFP100 (U4) or the BGA64 (U3) package can be installed, but not both.

Figure 4-1 EV-OXU200 Top-Level Schematic

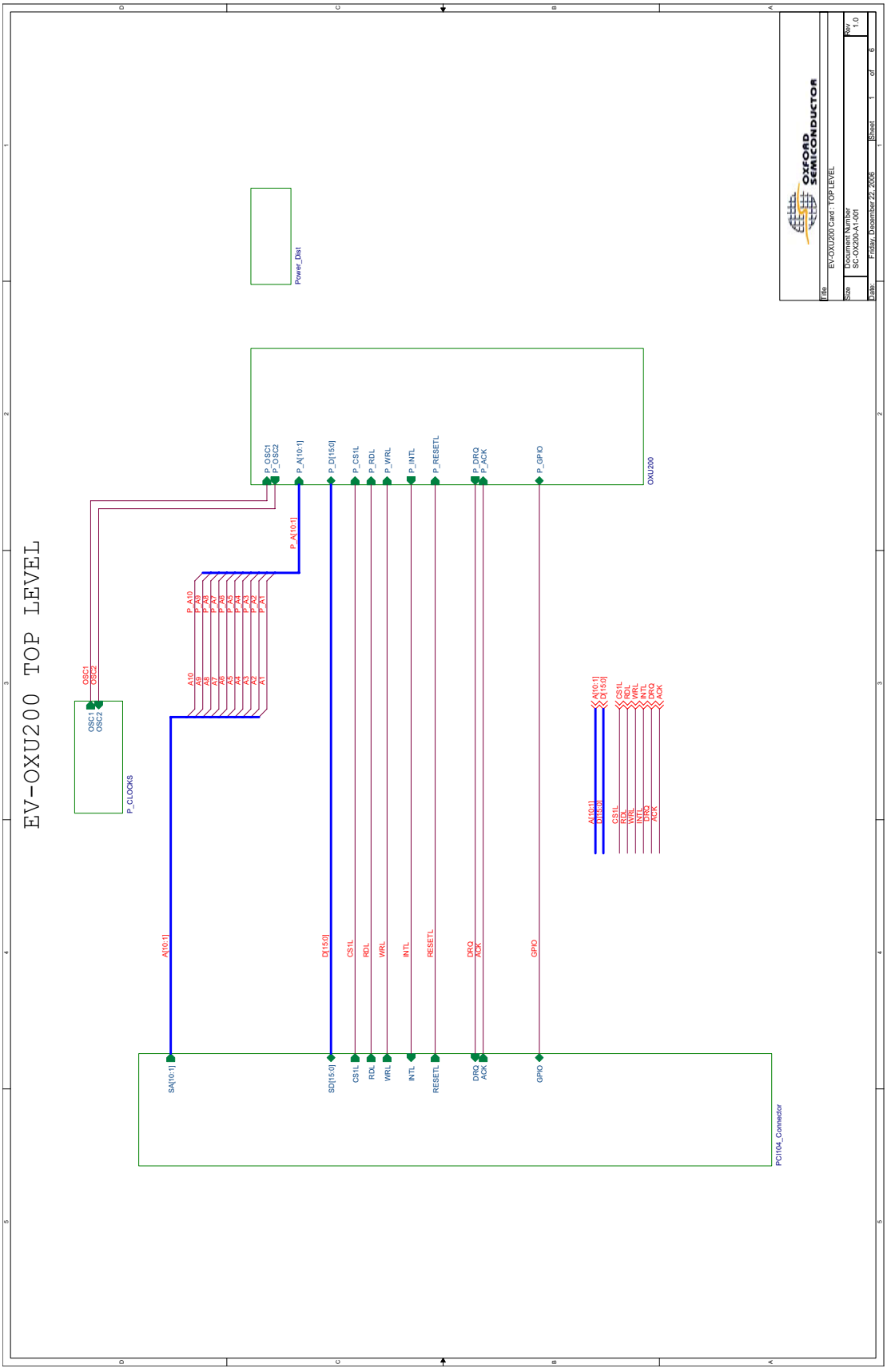

Figure 4-2 EV-OXU200 Test Headers

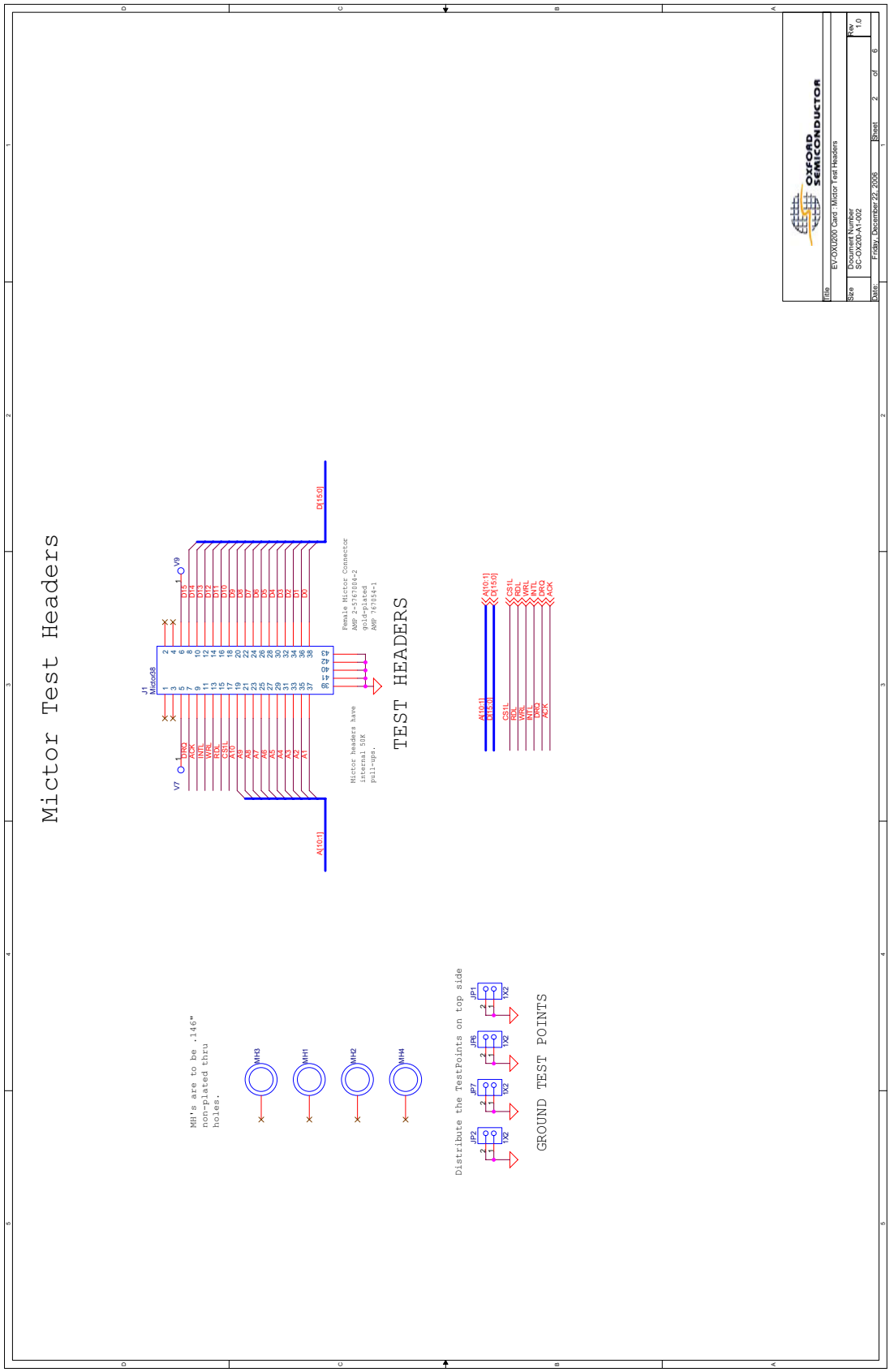

Figure 4-3 EV-OXU200 PC104 Connectors

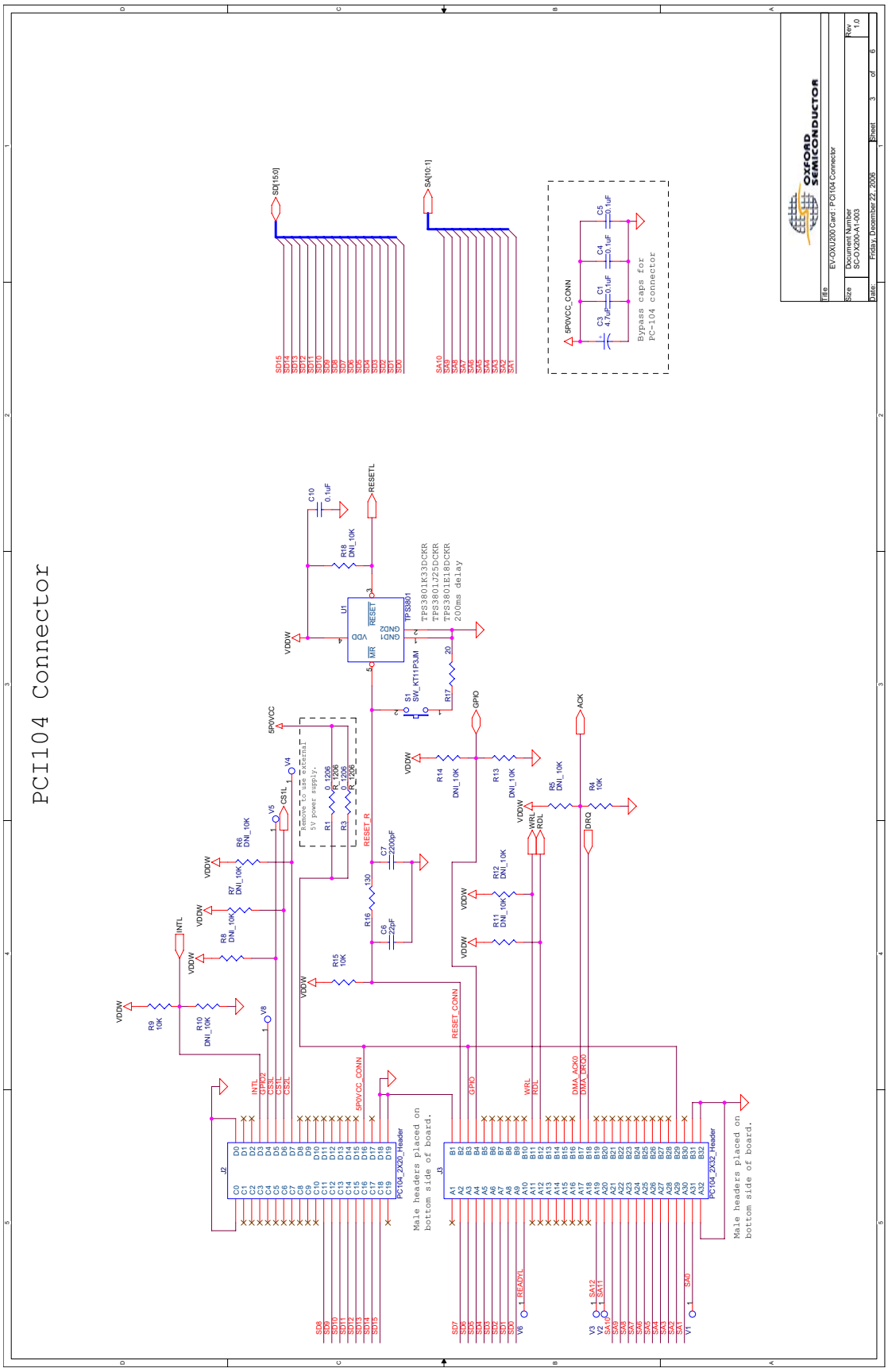

Figure 4-4 OXU200 Schematic

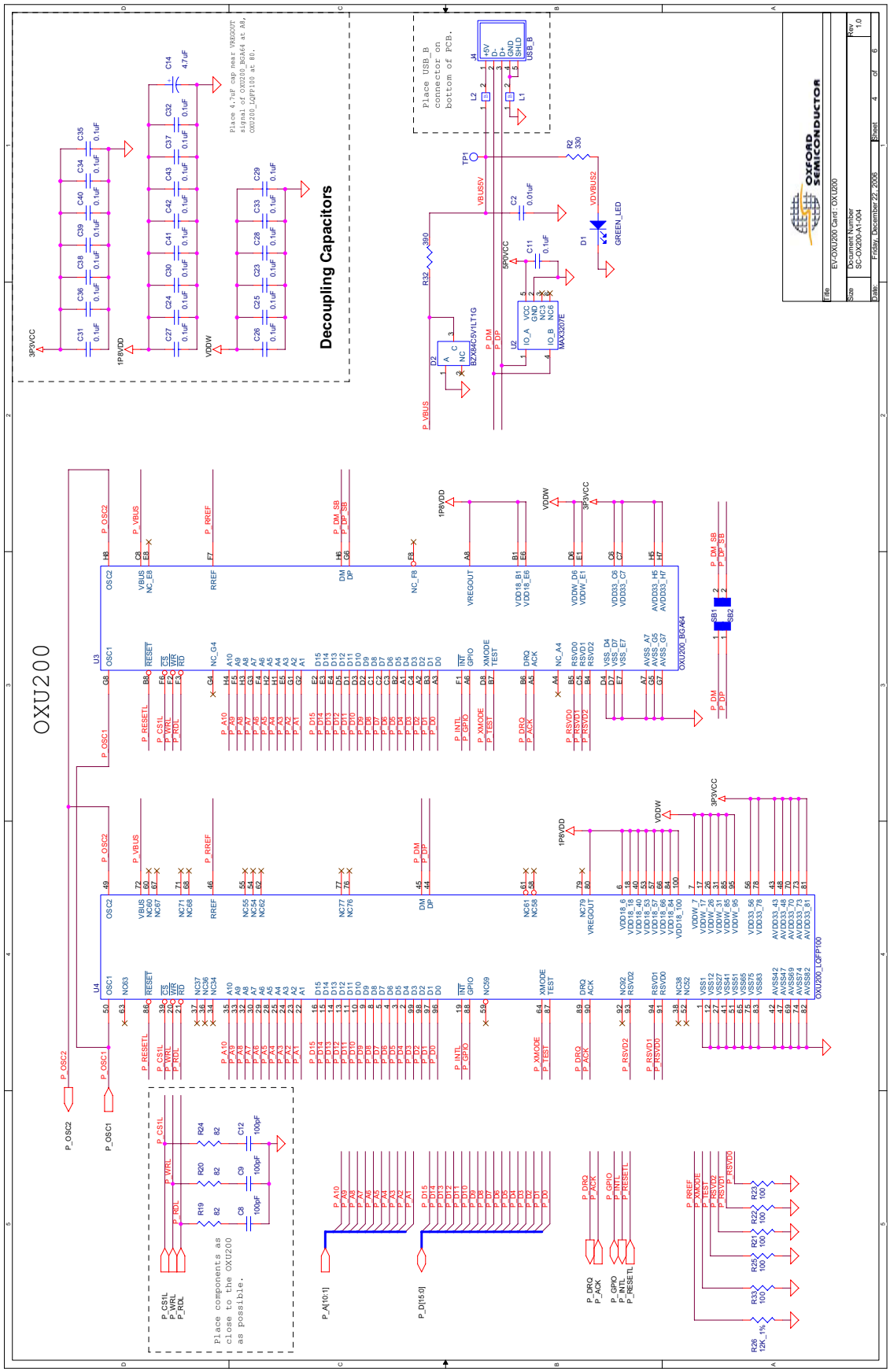

Figure 4-5 EV-OXU200 Clocks

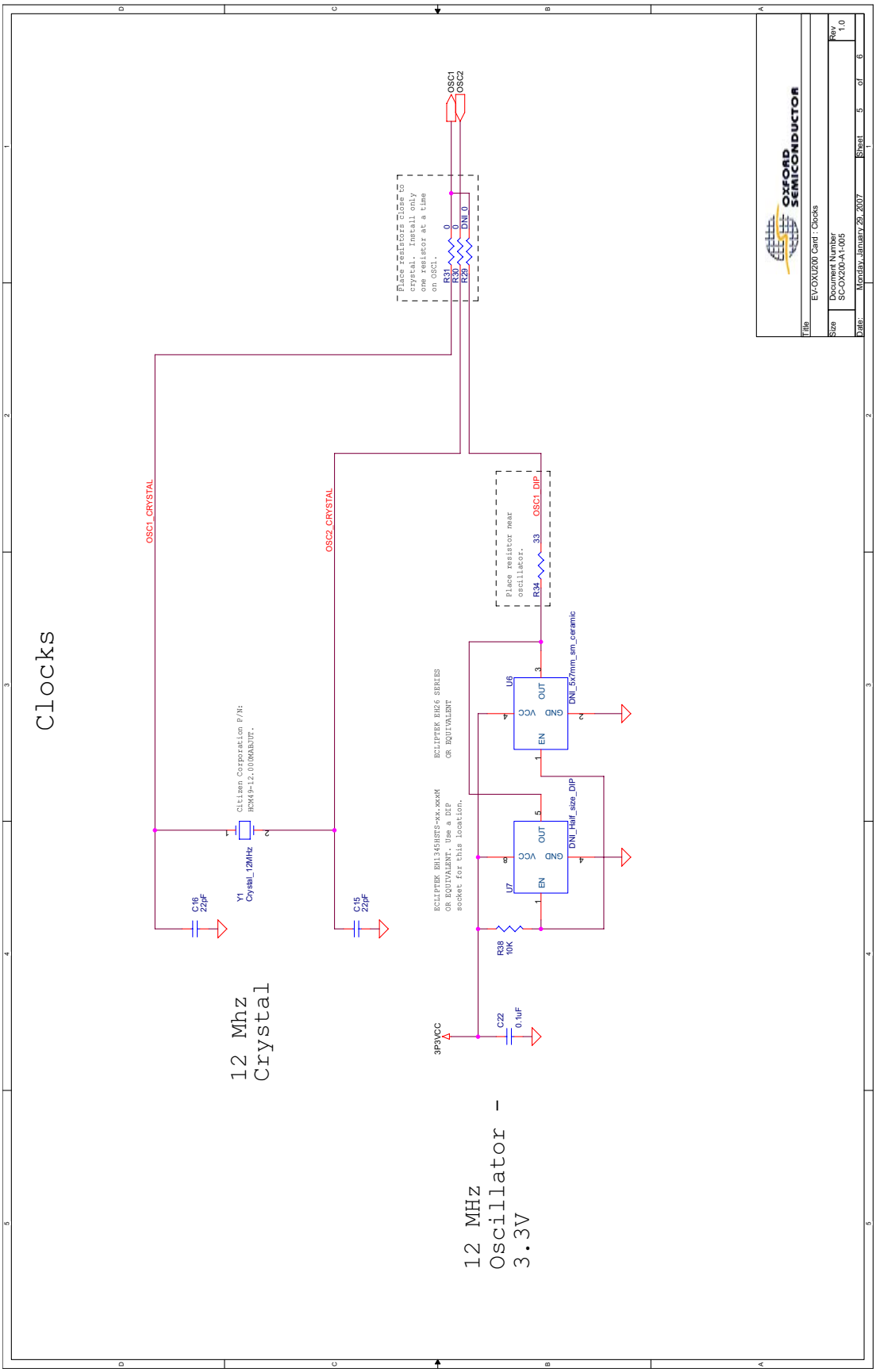

Figure 4-6 EV-OXU200 Power Distribution

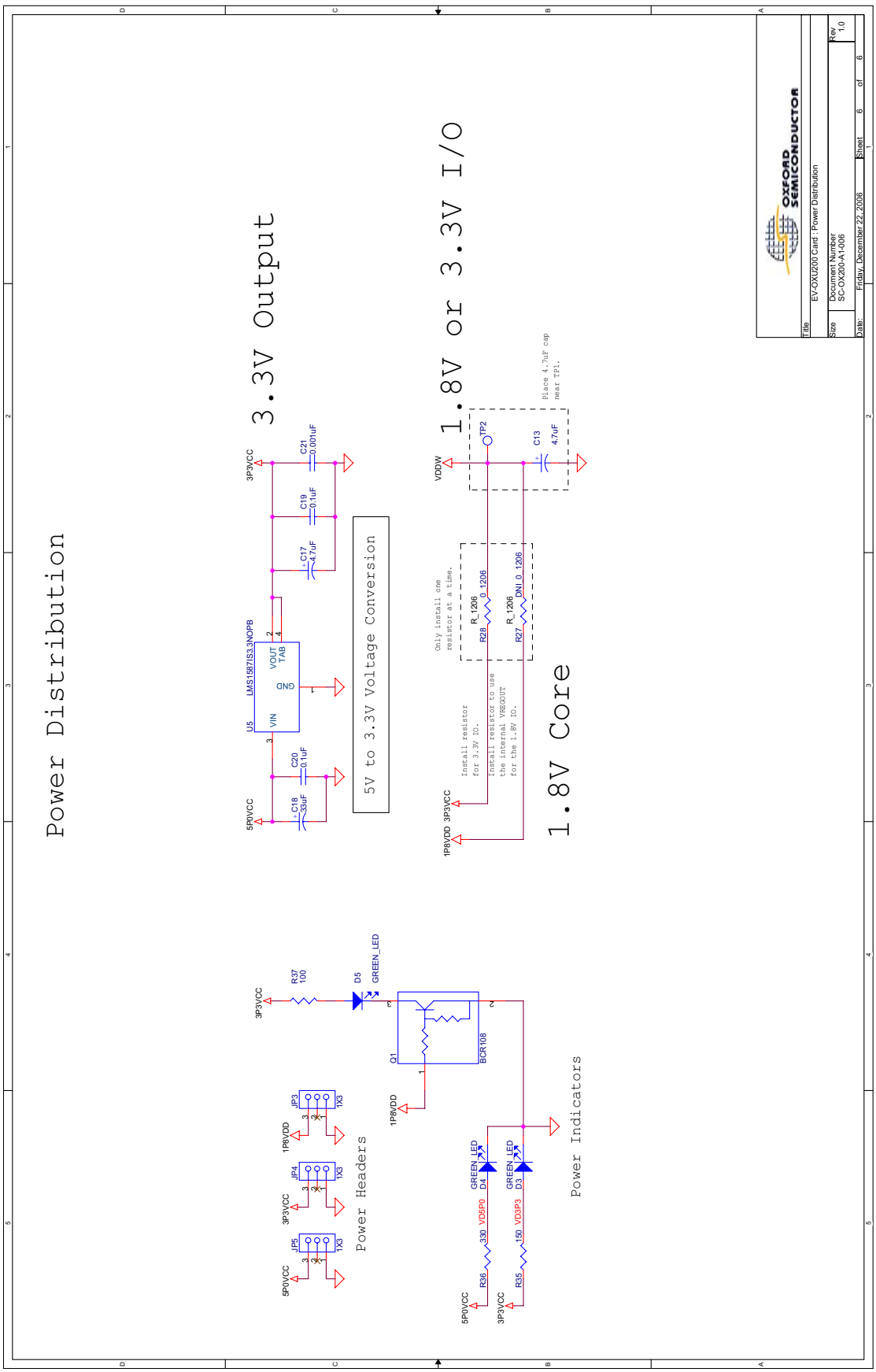

Figure 4-7 PCI104 Top-Level Schematic

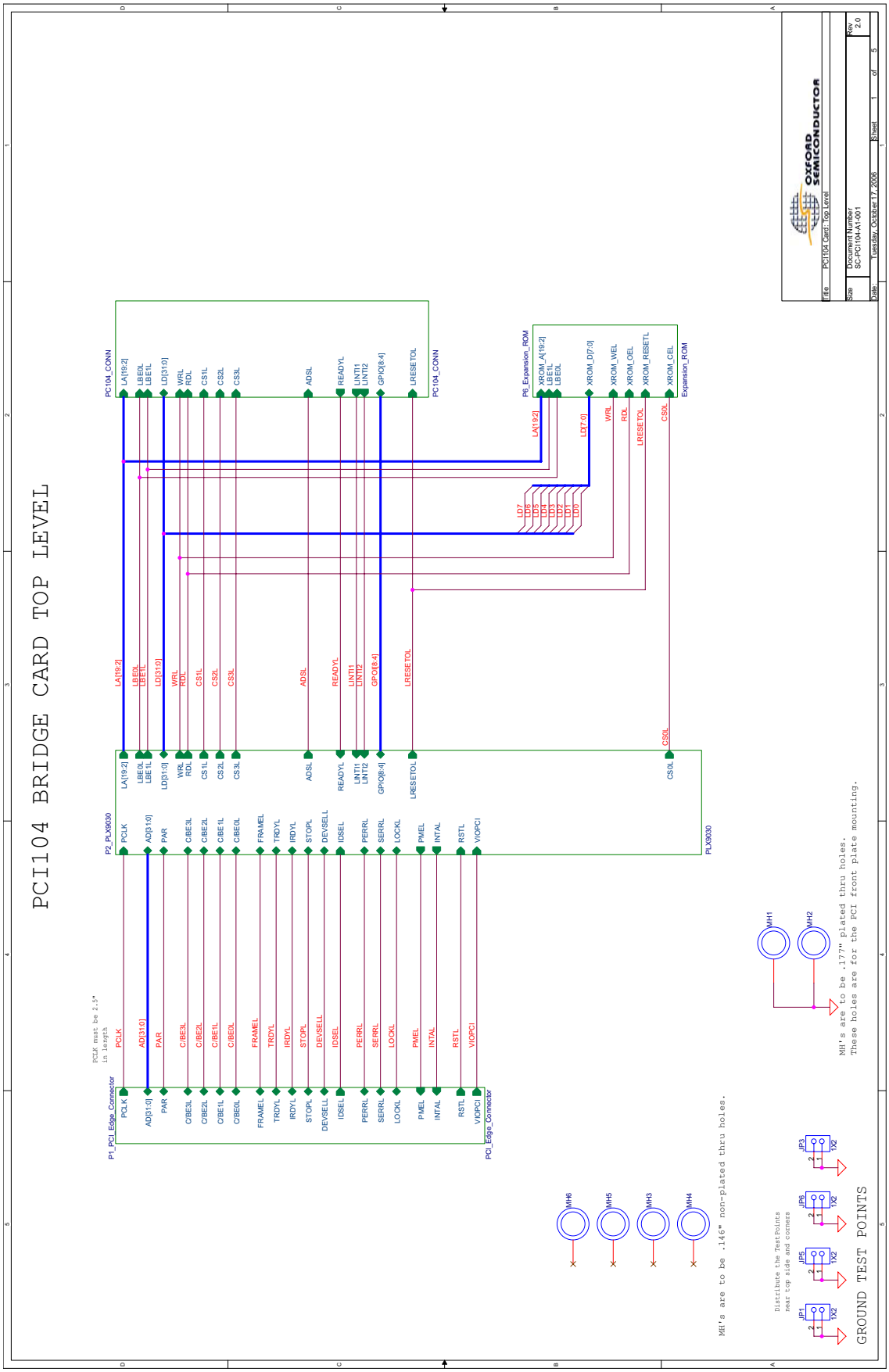

Figure 4-8 PCI104 PCI Connector

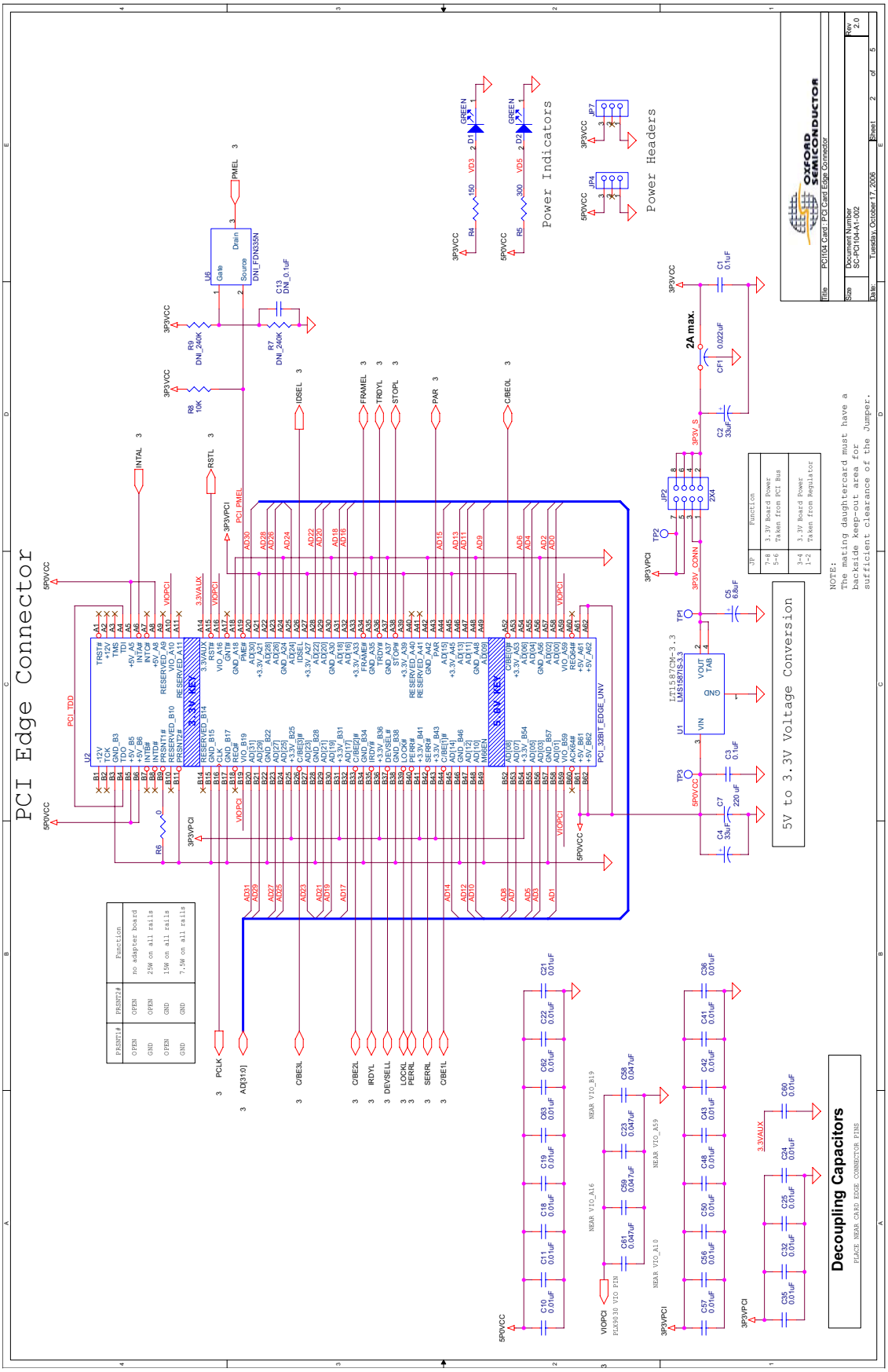

Figure 4-9 PCI9030 Bridge Chip

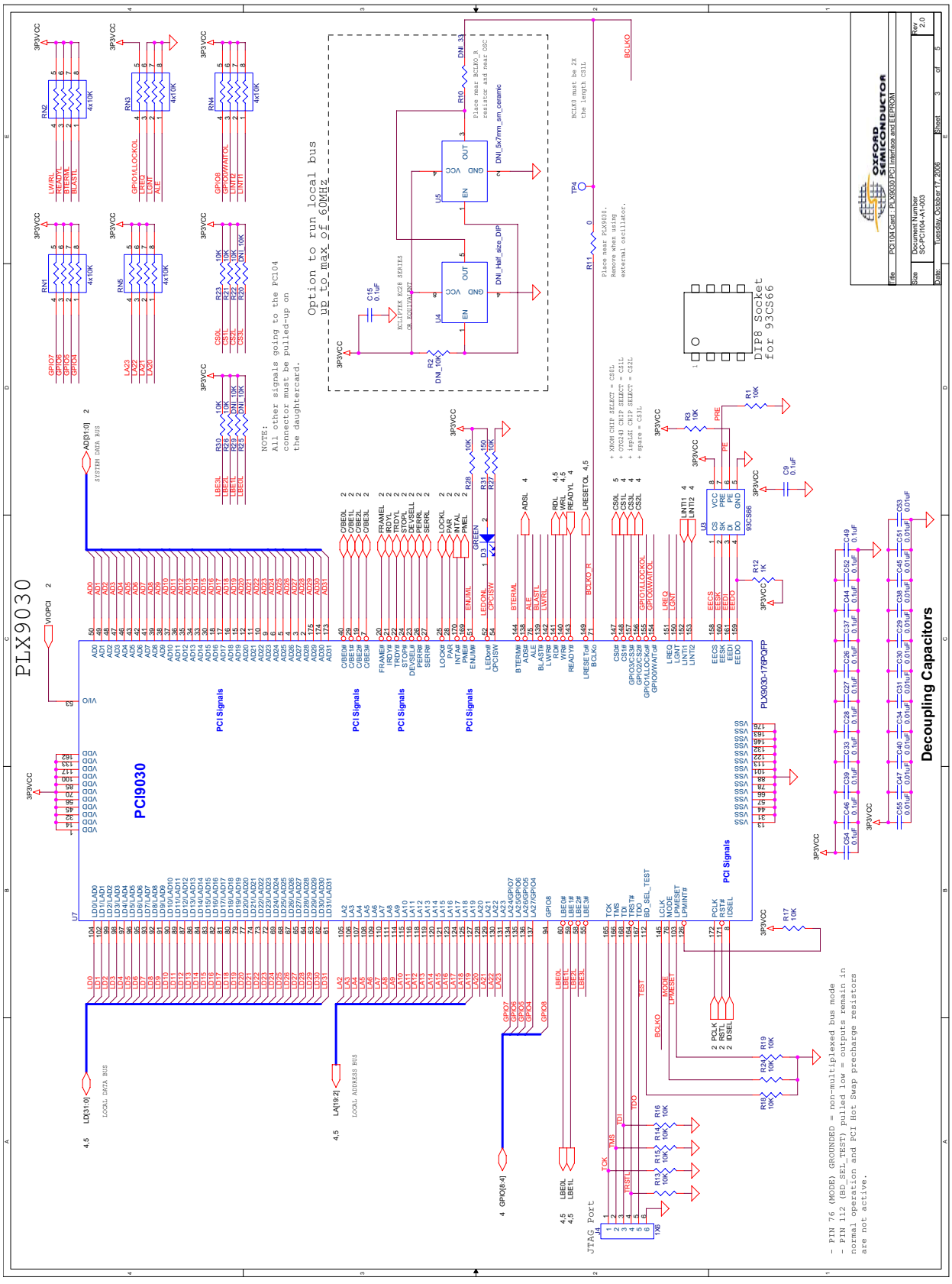

Figure 4-10 PC104 Connectors

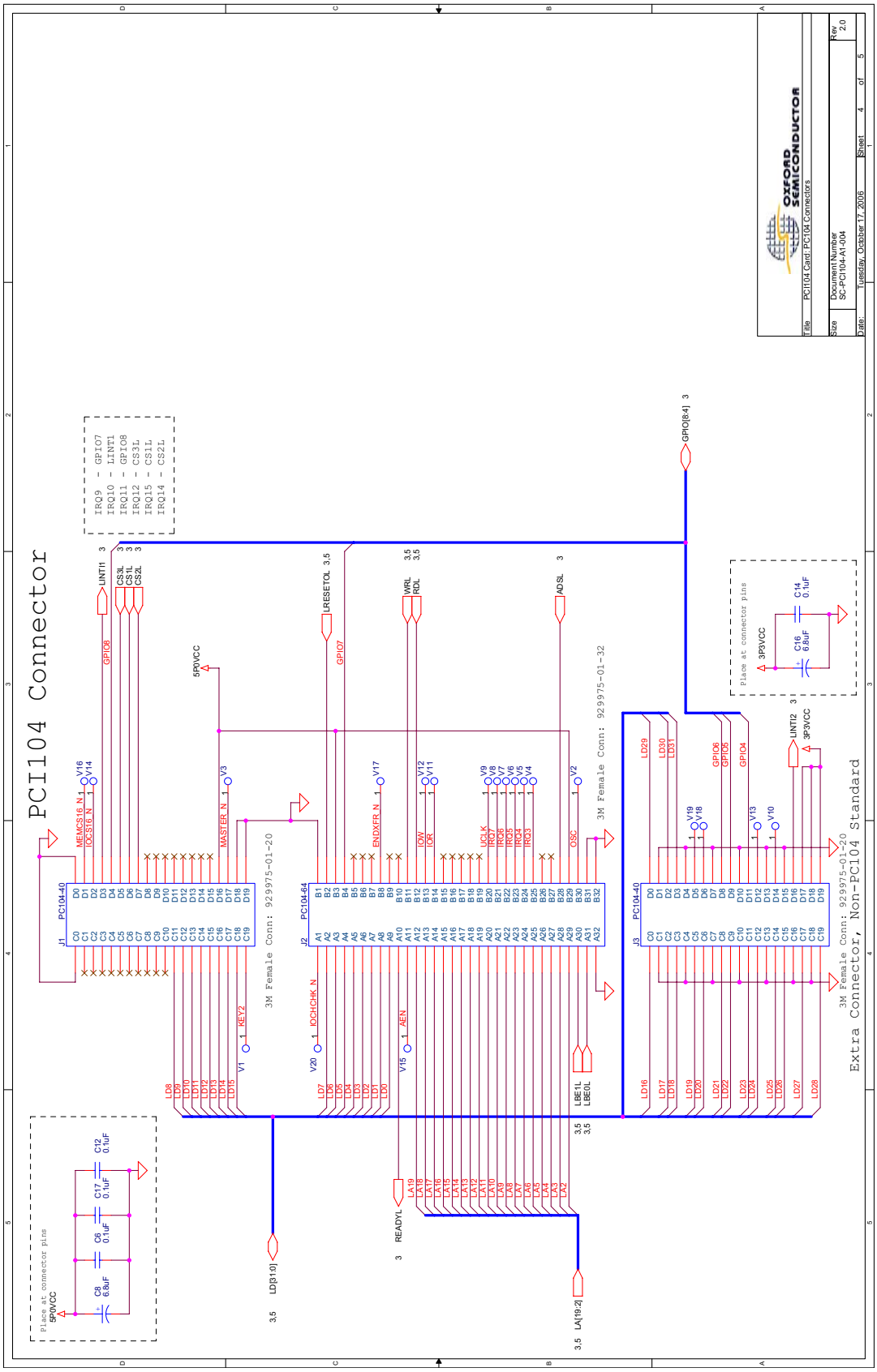

Figure 4-11 PC104 Expansion ROM