OXFORD SEMICONDUCTOR

Data Sheet

TDUHC122
USB Host Controller

Features

- USB host controller for embedded applications (set-top box, PDA, cell phone, digital camera, Bluetooth USB HCI physical bus, etc.)
- Compatible with the *Universal Serial Bus Specification, Revision 2.0*
- Standard 8-bit microprocessor bus interface
- Supports batch processing of up to 16 USB transactions without interrupting the MCU
- Supports both full speed (12 Mbps) and low speed (1.5 Mbps) USB transfers
- Supports all four types of USB transfers (control, bulk, interrupt, and isochronous with maximum packet size of 1023 bytes)
- Supports double and circular buffering for all four types of host controller transactions
- Direct device-to-device data transfer in one frame
- Separate transaction descriptor and data memory space
- Hardware generated Start of Frame (SOF)
- 2 KB data memory
- Supports in-place processing in the data memory – used for applications requiring peer-to-peer data transfer between USB devices
- Supports transaction spill over
- Power management with host suspend, remote wakeup, and power saving modes
- Fully qualified, market proven root hub with two downstream ports and integrated analog transceivers
- Supports OHCI/UHCI compliant USB host stack
- 6 MHz crystal/oscillator to reduce cost and EMI
- Single 3.3 V power supply
- 10×10 mm LQFP, 64-pin, RoHS compliant
- Operating temperature range: -40° to 85° C

Device Overview

The Oxford Semiconductor TDUHC122 is a two-port, single-chip USB host controller that is specifically designed for embedded systems, mobile communications, and consumer products. It is a non-PCI controller that is fully compliant with the USB Specification for full-speed (12Mb/s) and low-speed (1.5Mb/s) USB devices.

The TDUHC122 has unique, patent-pending features that are indispensable for achieving high data throughput and low interrupt rates, including batch processing, multiple interrupt modes, separate data and descriptor memory, and double buffering. It is optimized for cost, performance and ease of development. Low interrupt rates, low CPU overhead and low software overhead are essential criteria for embedded designs, and the TDUHC122 excels at all three metrics. It can be interfaced to CISC or RISC microprocessors, microcontrollers, or digital signal processors (DSPs) and is ideal for providing USB host functions to a wide range of applications including mobile devices, cell phones, PDAs, point-of-sale systems, test equipment, internet appliances, as well as serving as an interface for USB to Bluetooth controllers.

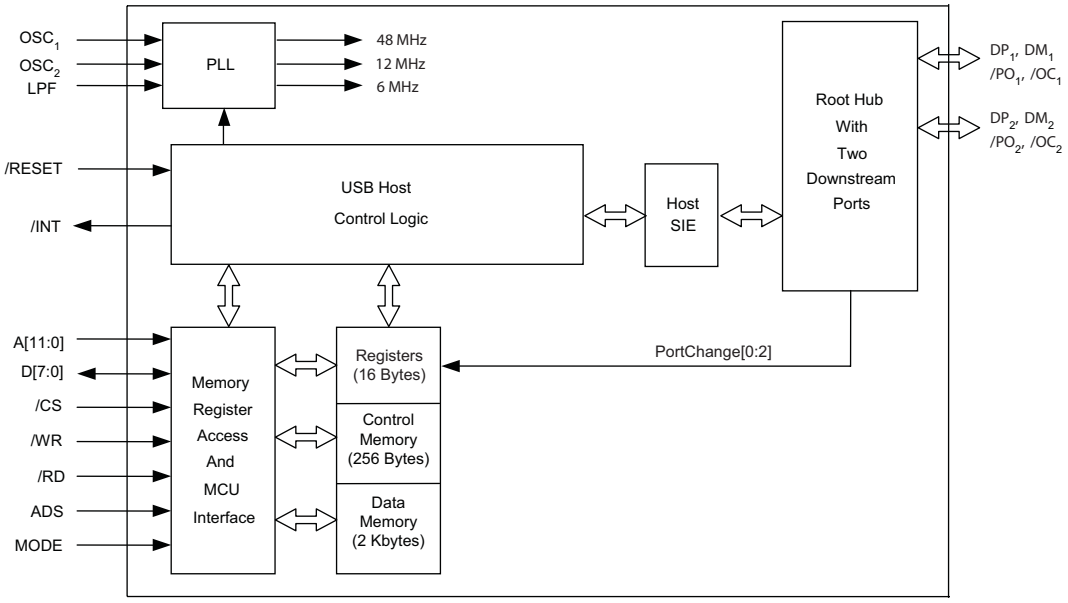
Because the TDUHC122 was designed specifically for embedded designs, it is the only non-PCI controller that has been proven to sustain full USB data rates, even while running under a full USB stack. With our competition, most USB devices like printers, MP3 players, zip drives and cameras will run slower, resulting in customer dissatisfaction. For real time data like audio or video, lower performance means that some peripherals may not work at all.

Software solutions for the TDUHC122 include USB device drivers and the Oxford Semiconductor USBLink™ product suite. USBLink Peripheral has been ported to a wide variety of real time operating systems including VxWorks®, ThreadX®, and Nucleus®.

In addition, Oxford Semiconductor also makes available low-level controller drivers for other native USB stacks such as those included with Windows® CE 5.0 and Linux® 2.6.x.

Figure 1 shows the TDUHC122 architectural diagram.

Figure 1 TDUHC122 Architectural Diagram



Development Support

The TDUHC122 product suite includes the USB controller as well as the protocol stacks and the driver software that enable a wide variety of USB applications. This unique ability to deliver a total hardware and software solution sets Oxford Semiconductor apart from other semiconductor companies and benefits customers by:

- Shortening time to market
- Reducing risk
- Offering a single source for hardware and software, thereby reducing the number of suppliers the customer has to deal with

Oxford Semiconductor is a Microsoft® Windows® Embedded Partner and has developed peripheral controller drivers for Windows CE 5.0. Similar software support is also available for Linux® 2.6.x.

For customers using a real time operating system (RTOS) such as VxWorks®, ThreadX®, Nucleus®, OSE, LynxOS® and AMX™ among others, Oxford Semiconductor offers its USBLink peripheral software solution.

The USBLink Product Suite is a modularized approach to providing USB connectivity for a wide variety of embedded products. Due to its flexible architecture and broad based support for USB host, peripheral and OTG applications, Oxford Semiconductor can tailor the USBLink software deliverables to meet each customer's USB requirements.

The USBLink solutions are configurable and can support systems with:

- Big or little endian processors
- DMA or non-DMA USB controllers
- A wide variety of USB controllers, including the TDUHC122
- A broad range of operating systems

Oxford Semiconductor has over eight years of experience developing embedded USB technology. Its USBLink software has been ported to over twenty different operating systems and a wide variety of embedded architectures. USBLink is shipping in many millions of units.

Sample Applications

- Set-top boxes
- Personal Digital Assistants (PDA)
- Cell phones
- Digital cameras
- Bluetooth USB HCI physical buses

Electrical Characteristics

Table 1 to Table 7 detail the required operating conditions for the device and the DC and AC electrical characteristics.

Table 1 Absolute Maximum Device Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{DD}	DC supply voltage		-0.3	3.6	V
V_I	DC input voltage		-0.3	V_{DD}+0.5	V
V_O	DC output voltage		-0.3	V_{DD}+0.5	V
T_O	Operating temperature		-40	+85	°C
T_S	Storage temperature		-65	+150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the normal operating conditions specified in the following section. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
V_{DD}	3.3 V supply voltage		3.0	3.6	V
I_{DDO}	Operational state current	V_{DD} = 3.3V, no devices		16	mA
I_{DDF}	Full USB traffic current	V_{DD} = 3.3V, one full-speed device		~20	mA
I_{DDS}	Suspend state current	V_{DD} = 3.3V, no devices		11	mA
I_{DDPS}	Power save state current	V_{DD} = 3.3V	100	~200	µA

D.C. Characteristics

Table 3 DC Characteristics, USB I/O Signals: D_P and D_M Only

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	Input level high (driven)		2.0		V
V_{IHZ}	Input level high (floating)		2.7		V
V_{IL}	Input level low			0.8	V
V_{DI}	Diff. input sensitivity	DP_n and DM_n	0.2		V
V_{CM}	Diff. comm. mode range		0.8	2.5	V
V_{OL}	Static output low	R_L of 1.5 kΩ to V_{DD}		0.3	V
V_{OH}	Static output high	R_L of 15 kΩ to V_{SS}	2.8	V_{DD}	V
V_{CRS}	Output signal crossover		1.3	2.0	V
C_{IN}	Input capacitance			20	pF

Table 4 DC Characteristics, Logic Signals

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Low level output voltage	V_{DD} = 3V, I_{OL} = 0.3 mA		V_{SS} + 0.1	V
V_{OH}	High level output voltage	V_{DD} = 3V, I_{OH} = 0.3 mA	V_{DD} - 0.1		V
C_{OUT}	Output capacitance	1 MHz		10	pF
V_{IL}	Low level input voltage	V_{DD} = 3.0 – 3.6 V	-0.3	$0.3 \cdot V_{DD}$	V
V_{IH}	High level input voltage	V_{DD} = 3.0 – 3.6 V	$0.7 \cdot V_{DD}$	V_{DD}	V
C_{IN}	Input capacitance	1 MHz		10	pF

Note: The capacitances listed above do not include pad capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance of about 0.5 pF and the package capacitance, which is about 0.86 pF max for LQFP.

Table 5 DC Characteristics, Oscillator Circuits OSC_1 and OSC_2

Symbol	Parameter	Condition	Min	Max	Unit
V_{LH}	OSC1 switching level		0.47	1.20	V
V_{HL}	OSC1 switching level		0.67	1.44	V
CX_1	Input capacitance, OSC_1			17	pF
CX_2	Output capacitance, OSC_2			17	pF
C_{12}	$OSC_{1/2}$ capacitance			1	pF
t_{SU}	Start-up time	6 MHz, fundamental		2	ms
DL	Drive level	V_{DD} = 3.3V, 6 MHz crystal, 100 Ω equiv series resistor		150	µW

A.C. Characteristics

Unless otherwise specified. Measurements are under the following conditions:

- V_{DD} = 3.3V
- Ambient temperature = 25 °C
- Clock edge switching time (from V_{SS} to V_{DD} or from V_{DD} to V_{SS}) = 1.0 ns.

Table 6 AC Characteristics, DP_n and DM_n Driver Characteristics (Full Speed)

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise time	C_L = 50 pF	4	20	ns
t_F	Fall time	C_L = 50 pF	4	20	ns
t_{RFM}	T_R/T_F matching		90	110	%
Z_{DRV}	Driver output resistance *	Steady state drive	28	44	W

- With external 22 Ω series resistor.

Table 7 AC Characteristics, DP_n and DM_n Driver Characteristics (Low Speed)

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise time	C_L = 200 - 600 pF	75	300	ns
t_F	Fall time	C_L = 200 - 600 pF	75	300	ns
T_{RFM}	T_R/T_F matching		80	125	%

Pin Layout

The TDUHC122 is supplied as a 64-pin LQFP package. Figure 2 shows the pin layout of the TDUHC122 package.

Figure 2 TDUHC122 64-Pin LQFP Package (Top View)

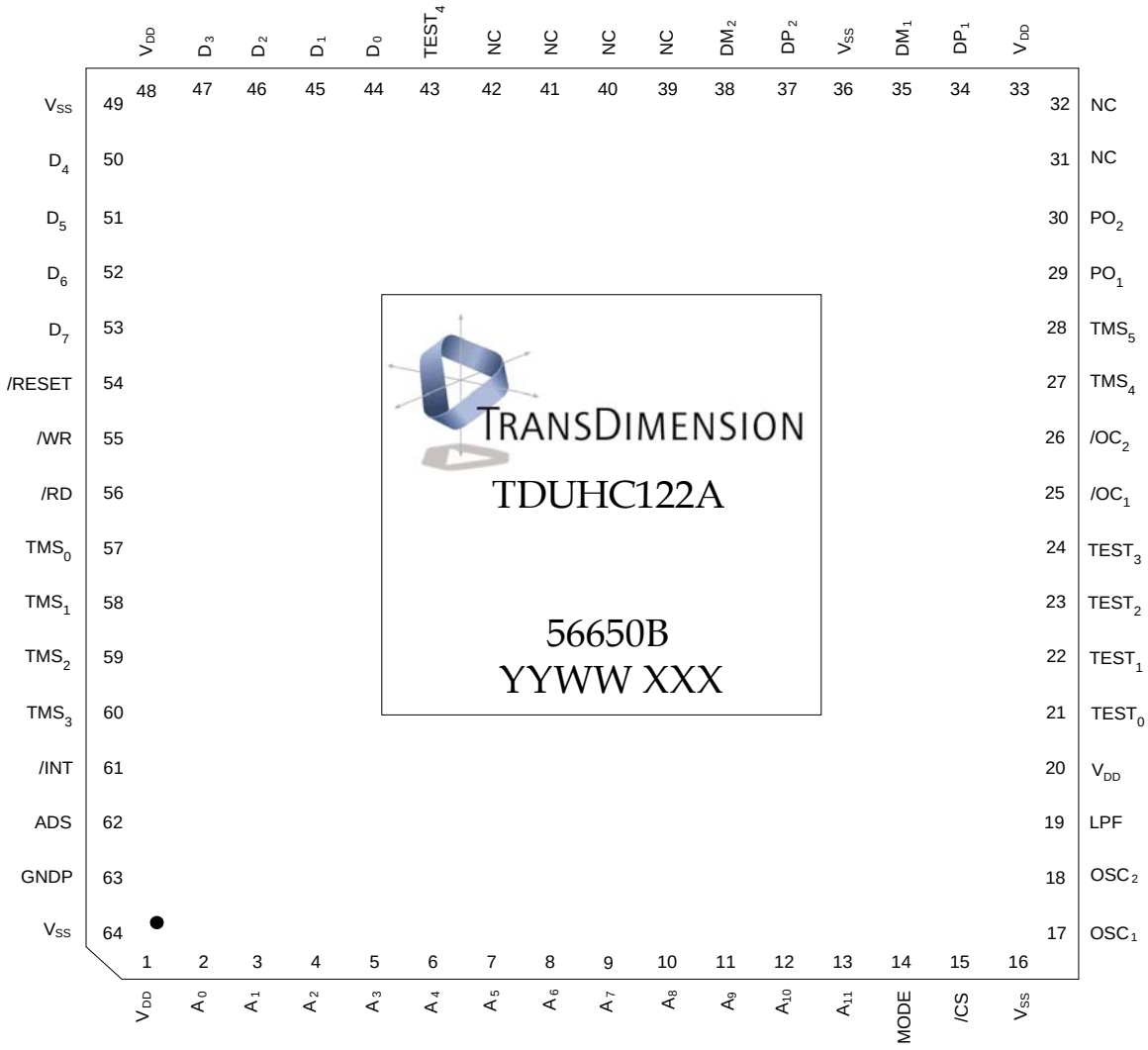


Table 8 lists the LQFP pin allocations.

Table 8 TDUHC122 ***64-Pin LQFP*** *Pin Allocations (Sheet 1 of 2)*

Pin	No. Bits	Type	Name	Description
Processor Interface (28 pins)				
44, 45, 46, 47, 50, 51, 52, 53	8	B	D_0 - D_7	Data Bus. D_7 is the most significant bit
2, 3, 4, 5, 6, 7, 8, 9 10, 11, 12, 13	12	I	A_0 - A_{11}	Address Bus. A_{11} (pin13) selects CM or DM
55	1	I	/WR	Memory Write Strobe. Active low
56	1	I	/RD	Memory Read Strobe. Active low
15	1	I	/CS	Chip Select. Active low
14	1	I	MODE	Memory Access Mode. MODE = 1: Non-multiplexed memory access. D_7:D_0 are connected to the MCU's data bus, A_{11}:A_0 to its address bus; MODE = 0: Multiplexed memory access with auto-incremented address. When accessing a block of TDUHC122 memory, the 12-bit starting address is first latched into the chip by writing the least significant 8-bits of the address into D_7:D_0 while holding ADS high, and placing the most significant 4-bits of the address on A_{11}:A_8. Data is then retrieved out of, or stored into TDUHC122 memory with successive read or write operations through D_7:D_0, while pin ADS is pulled low. The memory address is automatically incremented internally for each subsequent memory access. A_7:A_0 are not used under this mode
62	1	I	ADS	Address/Data Select. See discussion on signal MODE; When MODE = 1, this pin has no effect, and it should be tied to V_{SS} for noise immunity
61	1	O	/INT	Interrupt to the MCU. This pin can be software configured as a driven output or open drain. Open drain is the default
54	1	I	/RESET	Master Reset. Resets entire USB system; active low
63	1	I	GNDP	Voltage Reference. For built-in power on reset (POR), connect to V_{SS} (ground) for normal operation
Oscillator and PLL (3 pins)				
17	1	I	OSC_1	Oscillator Input. Input to the inverting oscillator amplifier
18	1	O	OSC_2	Oscillator Output. Output of the inverting oscillator amplifier
19	1	I	LPF	PLL Filter. Connecting to a passive RC network; see Section 9 on proper usage of this pin

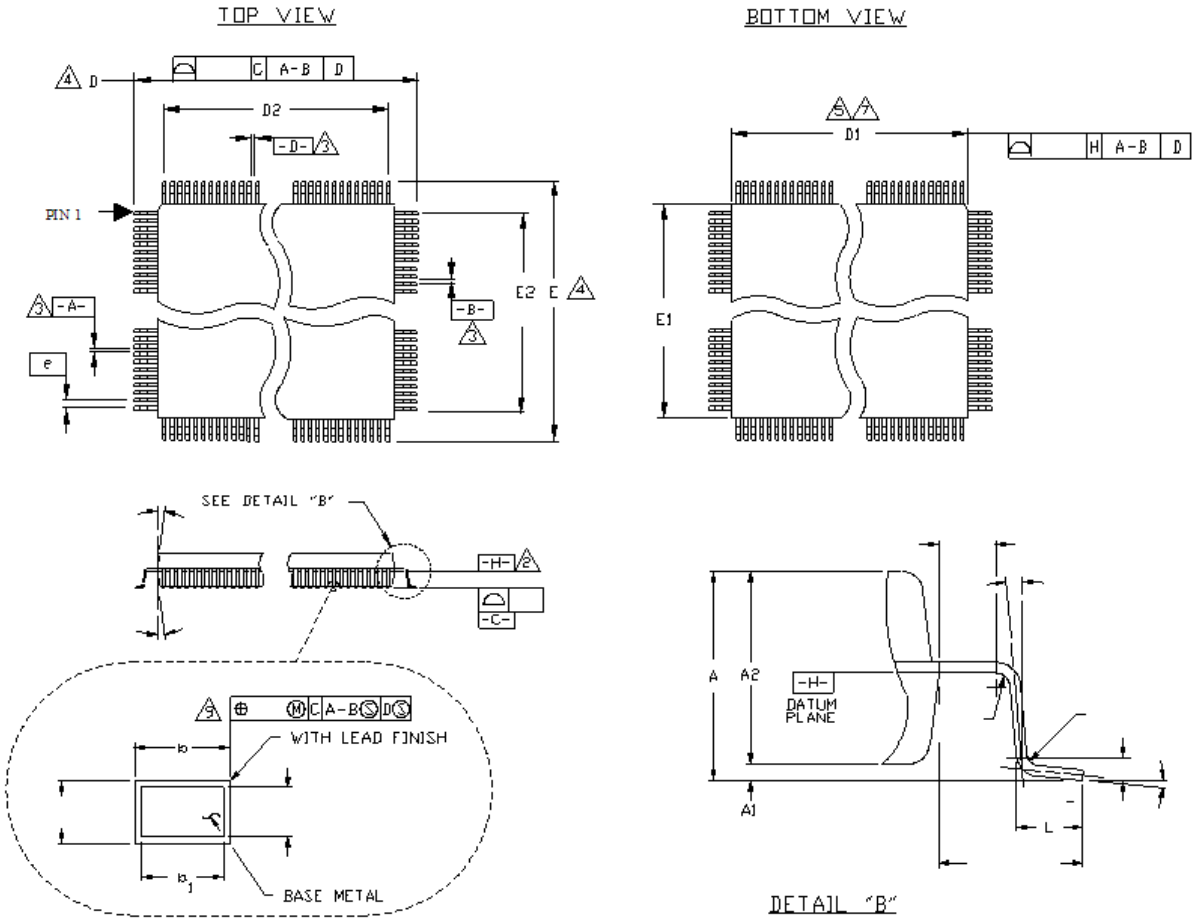
Table 8 TDUHC122 ***64-Pin LQFP*** *Pin Allocations (Sheet 2 of 2)*

Pin	No. Bits	Type	Name	Description
USB Interface (8 pins)				
34, 35, 37, 38	4	B	DP_1, DM_1, DP_2, DM_2	Port Data for USB I/O DP_1:DP_2 and DM_1:DM_2 are the differential signal pairs to connect downstream USB devices [7.1:107]
25, 26	2	I	$/OC_1$, $/OC_2$	Over Current Indicator. Input signal to indicate to the root hub that over current is detected at the port; active low. If $/OC_n$ is asserted, the root hub will de-assert $/PO_n$, and report the status in the root hub's port status register
29, 30	2	O	$/PO_1$, $/PO_2$	Power On Switch. Output signal to turn on the external voltage supplying power to a port; active low. $/PO_n$ is de-asserted when a power supply problem is detected at $/OC_n$, where n is 1 or 2
Power & Ground (8 pins)				
1, 20, 33, 48,	4	V	V_{DD}	3.3 V Power Supply. All four pins must be connected
16, 36, 49, 64	4	V	V_{SS}	Ground. All four pins must be connected
Test (11 pins)				
28, 27, 60, 59, 58, 57	6	I	TMS_0, TMS_1, TMS_2, TMS_3, TMS_4, TMS_5	Test Mode Select. Used only for factory testing. Must connect to V_{SS} for normal operation
21, 22, 23, 24, 43	5	B	$TEST_0$, $TEST_1$, $TEST_2$, $TEST_3$, $TEST_4$	Test Signal I/O. Used only for factory testing; working in output mode during normal operation, they must be left floating
Miscellaneous (6 pins)				
42, 41, 40, 39, 32, 31	6	-	NC	These signals should be left floating. Do not connect them to either V_{SS} or V_{DD}

Package Layout

Figure 3 shows the package layout for the 64-pin LQFP package.

Figure 3 64-Pin LQFP



Package Dimensions

Table 9 list the package dimensions. All units are in mm unless otherwise specified.

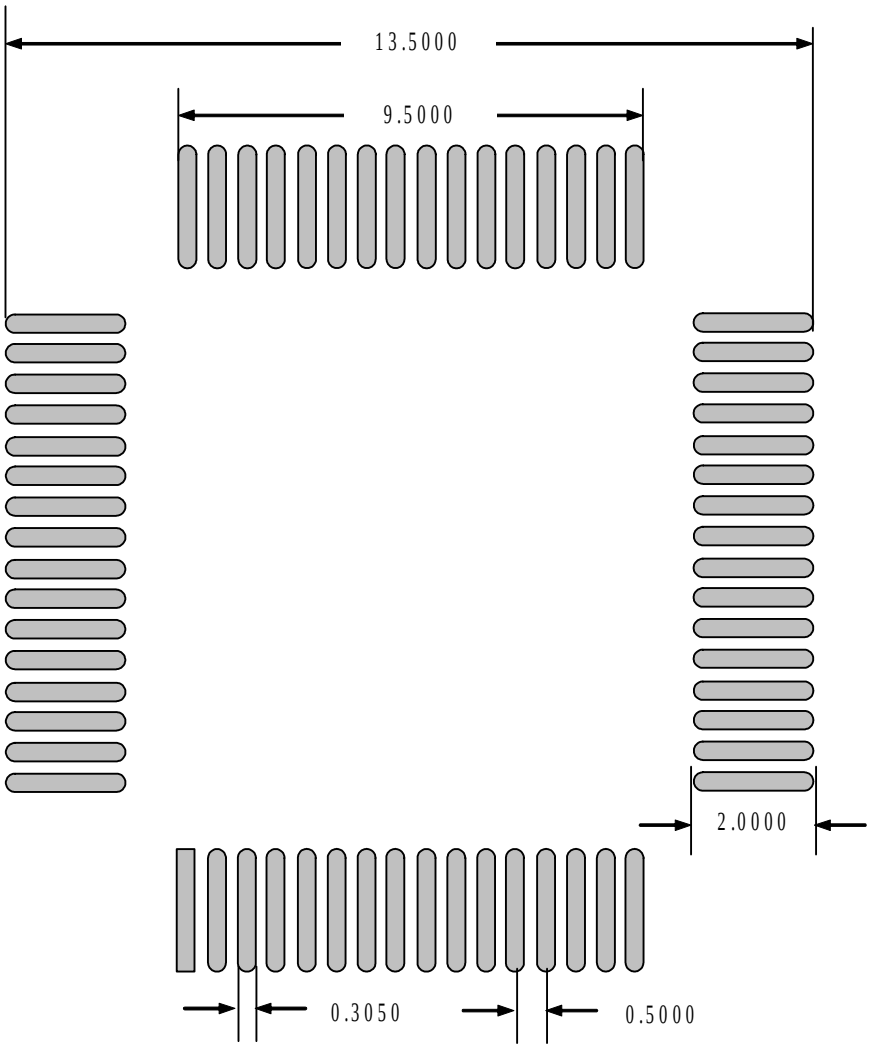
Table 9 TDUHC122 Package Dimensions

Symbol	Min	Nom	Unit
c	0.09		0.02
c1	0.09	50	0.16
L	0.45		0.75
L1		1.00 REF	
R2	0.08		0.20
R1	0.08		
S	0.2		
θ	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
A			1.60
B	0.17	0.22	0.27
b1	0.17	0.20	0.23
D		12.0 BSC	
E		12.0 BSC	
D1		10.0 BSC	
E1		10.0 BSC	
D2		7.5 BSC	
E2		7.5 BSC	
e		0.50 BSC	
A1	0.05		0.15
A2	1.35	140	1.45
Tolerances of Form and Position			
aaa		0.20	
bbb		0.20	
ccc		0.10	
ddd		0.08	

Landing Pattern

Figure 4 illustrates the recommended landing pattern. All units are in mm.

Figure 4 TDUHC122 Recommended Landing Pattern



Soldering Profile

Figure 10 lists the recommended soldering profile from J-STD-20.

Table 10 Recommended Soldering Profile

Parameters	Convection or IR/ Convection	VPR (Vapor Phase)
Average ramp-up rate (183°C to Peak)	3° C /s max.	10° C /s
Preheat temperature 125 ±25 °C	120s max.	
Temperature maintained above 183°C	60-150s	
Time within 5°C of actual peak temperature	10-20s	60s
Peak temperature range	235 +5/-0° C	235 +5/-0° C
Ramp-down rate	6° C /s	10° C /s
Time 25°C to peak temperature	6min max.	

A maximum of three reflow passes is allowed per component.

Storage Conditions

Dry packed products must not be stored for more than 1 year at 40°C and 90% RH.

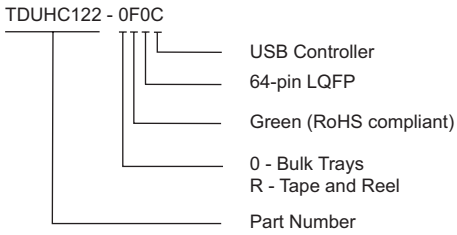
A longer storage period is allowed taking into account the following conditions: 5 years max. at 25°C ±5°C, 50% RH.

From opening the packs, the product must be assembled within 168 hours (the worst in process storage condition assumed: 30°C, 60% RH).

If the product cannot be soldered within this time period, then the product must be dried at 125°C for 24 hours. Only one drying is allowed.

Ordering Information

The following conventions are used to identify Oxford Semiconductor products.



Contacting Oxford Semiconductor

See the Oxford Semiconductor website (http://www.oxsemi.com) for further detail about Oxford Semiconductor devices, or email sales@oxsemi.com.

Revision Information

Table 11 documents the revisions of this guide.

Table 11 Revision Information

Revision	Modification
Mar 07	First publication

USBLink is a trademark of Oxford Semiconductor, Inc.
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