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EV-TD122-UHC124-PCI and EV-TD122-UHC124 Evaluation Board User Guide

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Contents

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Preface

This manual documents the EV-TD122-UHC124-PCI Evaluation Board hardware.

Revision Information

Table I documents the revisions of this manual

Table I Revision Information

Revision	Modification
Nov 2006	First publication

Typographic Conventions

In this manual, the conventions listed in Table II apply.

Table II Typographic Conventions

Convention	Meaning
Italic Letters With Initial Capital Letters	A cross-reference to another publication
`Courier Font`	Software code, or text typed in via a keyboard
1, 2, 3	A numbered list where the order of list items is significant
■	A list where the order of items is not significant
"Title"	Cross-refers to another section within the document
	Significant additional information

Ordering Information

The following boards are available:

- EV-TD122-UHC124-PCI Evaluation Board with the TD122 (EV-TD122-UHC124-PCI-110)
- EV-TD122-UHC124 Evaluation Board with the TD122 (EV-TF122-UHC124-110)
- EV-TD122-UHC124-PCI Evaluation Board with the UHC124 (EV-TD122-UHC124-PCI-210)
- EV-TD122-UHC124 Evaluation Board with the UHC124 (EV-TF122-UHC124-210)
- PCI104 Bridge Board (TDPCI104-1000-01)

Contacting Oxford Semiconductor

See the Oxford Semiconductor website (http://www.oxsemi.com) for further details about Oxford Semiconductor devices, or email sales@oxsemi.com.

Chapter 1

EV-TD122-UHC124-PCI

Overview

The EV-TD122-UHC124-PCI Evaluation Board is a system for TD122 and UHC124 customer evaluations and internal software development in the PC environment. The EV-TD122-UHC124-PCI Evaluation Board allows the user to install and use the TD122 or UHC124 in any PCI-based computer. Application software running on the system has access to the TD122 or UHC124 via the PCI memory space.The EV-TD122-UHC124 board can be used without the PCI Bridge Board, the PCI104.

The EV-TD122-UHC124-PCI allows customers to:

- Evaluate the Oxford Semiconductor TD122 and UHC124 USB host controller
- Run TD122 and UHC124 demonstrations
- Develop user software for TD122-UHC124-based applications

While the EV-TD122-UHC124-PCI can be used to evaluate the TD122-UHC124, it will not result in optimal performance due to the long access times of the PCI bus. For optimal performance evaluation, the TD122-UHC124 should be placed directly on the system bus using the EV-TD122-UHC124 board as described in Chapter 2 .

The EV-TD122-UHC124-PCI Evaluation Board is a two-board combination of the following:

- An EV-TD122-UHC124 Evaluation Board with 2 or 4 USB host ports
- A 33 MHz, 32-bit PCI Bridge Board, the PCI104

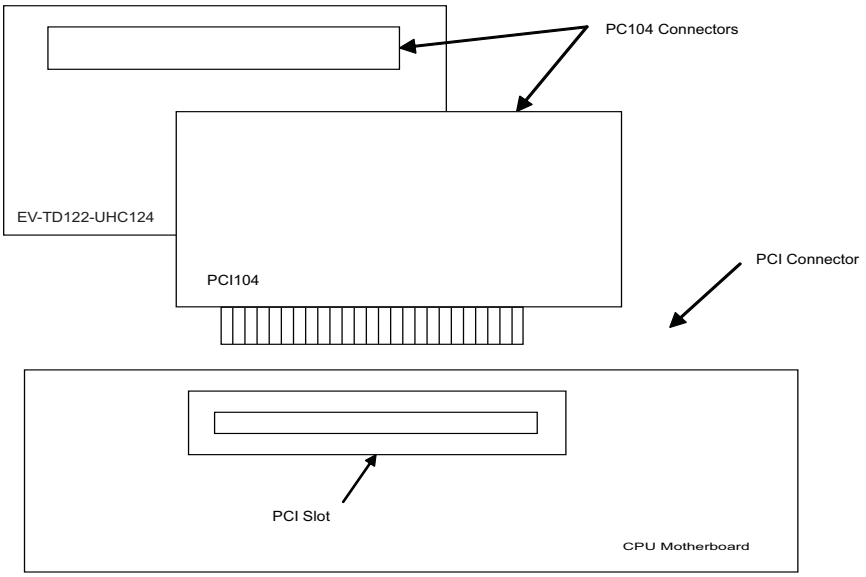
The EV-TD122-UHC124 Evaluation Board contains the TD122 or the UHC124 and all the USB-specific hardware.

The PCI104 Bridge Board contains the PCI9030 PCI bridge chip that bridges the PCI bus to the TD122 or UHC124. Power and control signals to the PCI bus are maintained by the PCI bridge chip, while initialization and configuration of the PCI bridge chip is maintained by the on-board serial EEPROM.

Figure 1-1 illustrates the orientation of the two boards. The combined boards are approximately one inch thick and require space for two PCI devices, but only one PCI slot. The two or four host USB connectors are easily accessible through the openings in the computer case.

Chapter 2 describes the EV-TD122-UHC124 Evaluation Board. Chapter 3 describes the PCI104 Bridge Board. For complete information about the TD122 device, see the *TD122 USB Host Controller Technical Manual*. For complete information about the UHC124 device, see the *UHC124 USB Host Controller Data Sheet*.

Figure 1-1 EV-TD122-UHC124-PCI System Board Orientation



PCI Operation

Every PCI implementation has a PCI configuration space, where the PCI configuration registers are found. PCI configuration registers are accessed with reads/writes to the configuration space, which is separate from memory and I/O space. Table 1-1 lists the standard PCI configuration register space for all PCI functions on the PCI bus.

Table 1-1 Standard PCI Configuration Register Space

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID		Vendor ID		00h
Status Register		Command Register		04h
Class Code			Revision ID	08h

Table 1-1 Standard PCI Configuration Register Space

Byte 3	Byte 2	Byte 1	Byte 0	Offset
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Register 0 (BAR 0)				10h
Base Address Register 1 (BAR 1)				14h
Base Address Register 2 (BAR 2)				18h
Base Address Register 3 (BAR 3)				1Ch
Base Address Register 4 (BAR 4)				20h
Base Address Register 5 (BAR 5)				24h
CardBus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capabilities Pointer	34h
Reserved				38h
Max Latency	Min Grant	Interrupt Pin	Interrupt Line	3Ch

The PCI104 can be identified on the PCI bus during enumeration by the following PCI configuration registers:

Table 1-2 PCI Configuration Registers

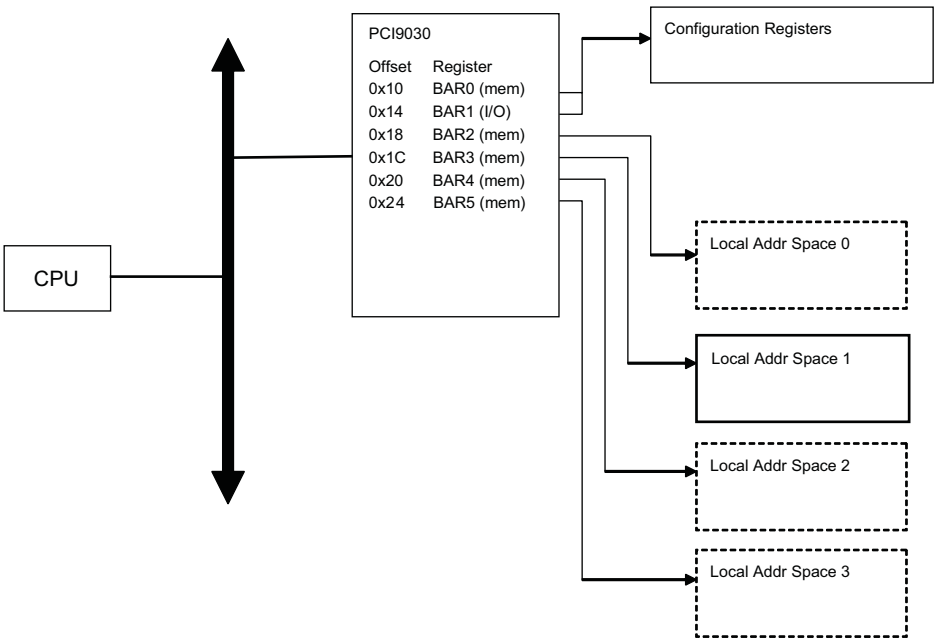
Register	Power-On Value
Vendor ID	192Eh
Device ID	012Fh
Revision	0001h
Class Code	0680h
Subsystem ID	012Fh
Subsystem Vendor ID	192Eh

Most operating systems provide functions for finding devices on the PCI bus. These functions typically key off the Vendor and Device IDs, or the Class Code. Because the Class Code for the PCI104 appears as a PCI Bridge with sub class code “other”, the search should be keyed to the Vendor and Device IDs.

Configuration

The EV-TD122-UHC124-PCI has two memory mapped register spaces and one I/O mapped register space. The address locations of the various spaces are determined by the Base Address Registers of the PCI configuration registers. Base Address Register 0 (BAR0) of the PCI configuration registers contains the address of the memory mapped PCI bridge controller registers. BAR1 contains the I/O address for the same PCI bridge controller registers. The PCI bridge controller registers are mapped into both memory and I/O space, so that these registers can be accessed via memory accesses or I/O addressing. BAR3 contains the address of the memory mapped TD122 or UHC124 registers. Figure 1-2 illustrates the register mappings within a PCI system.

Figure 1-2 PCI104 Register Mappings



The Base Address Registers are typically initialized by the system BIOS or by the operating system. Software generally does not have to set the addresses of the mapped locations, however, this is system dependent. If these registers are not initialized, the three spaces should be manually mapped into system memory and I/O space accordingly. Care must be taken to ensure no conflicts exist between the mapped regions and other devices on the PCI bus.

Serial EEPROM Registers

The PCI9030 PCI bridge chip provides an interface to program the attached serial EEPROM. The serial EEPROM is pre-programmed with the default values in Table 1-3. The table is for informational purposes only. If the default values are modified, the behavior of the PCI104 will change.

Table 1-3 Serial EEPROM Registers

Serial EEPROM Offset	Description	Default
00h	PCI Device ID	012Fh
02h	PCI Vendor ID	192Eh
04h	PCI Status Register	0290h
06h	PCI Command Register	0003h
08h	PCI Class Code	0680h
0Ah	PCI Class Code / Revision Number	0001h
0Ch	PCI Subsystem ID	016Bh
0Eh	PCI Subsystem Vendor ID	192Eh
10h	MSB New Capability Pointer	0000h
12h	LSB New Capability Pointer	0040h
14h	(Maximum Latency and Minimum Grant are not loadable)	0000h
16h	Interrupt Pin (Interrupt Line Routing is not loadable)	0100h
18h	MSW of Power Management Capabilities	4801h
1Ah	LSW of Power Management Next Capability Pointer / Power Management Capability ID	4801h
1Ch	MSW of Power Management Data /PMCSR Bridge Support Extension	0000h
1Eh	LSW of Power Management Control/Status	0000h
20h	MSW of Hot Swap Control/Status	0000h
22h	LSW of Hot Swap Next Capability Pointer / Hot Swap Control	4C06h
24h	PCI Vital Product Data Address	0000h
26h	PCI Vital Product Data Next Capability Pointer / PCI Vital Protocol Data Control	0003h
28h	MSW of Local Address Space 0 Range	0000h
2Ah	LSW of Local Address Space 0 Range	0000h
2Ch	MSW of Local Address Space 1 Range	FFFFh
2Eh	LSW of Local Address Space 1 Range	F000h
30h	MSW of Local Address Space 2 Range	0000h
32h	LSW of Local Address Space 2 Range	0000h
34h	MSW of Local Address Space 3 Range	0000h
36h	LSW of Local Address Space 3 Range	0000h
38h	MSW of Expansion ROM Range	0000h
3Ah	LSW of Expansion ROM Range	0000h
3Ch	MSW of Local Address Space 0 Local Base Address (Remap)	0000h
3Eh	LSW of Local Address Space 0 Local Base Address (Remap)	0000h
40h	MSW of Local Address Space 1 Local Base Address (Remap)	0000h
42h	LSW of Local Address Space 1 Local Base Address (Remap)	0001h
44h	MSW of Local Address Space 2 Local Base Address (Remap)	0000h
46h	LSW of Local Address Space 2 Local Base Address (Remap)	0000h
48h	MSW of Local Address Space 3 Local Base Address (Remap)	0000h
4Ah	LSW of Local Address Space 3 Local Base Address (Remap)	0000h

Table 1-3 Serial EEPROM Registers

Serial EEPROM Offset	Description	Default
4Ch	MSW of Expansion ROM Local Base Address (Remap)	0010h
4Eh	LSW of Expansion ROM Local Base Address (Remap)	0000h
50h	MSW of Local Address Space 0 Bus Region Descriptor	0080h
52h	LSW of Local Address Space 0 Bus Region Descriptor	0000h
54h	MSW of Local Address Space 1 Bus Region Descriptor	4013h
56h	LSW of Local Address Space 1 Bus Region Descriptor	F940h
58h	MSW of Local Address Space 2 Bus Region Descriptor	0000h
5Ah	LSW of Local Address Space 2 Bus Region Descriptor	0000h
5Ch	MSW of Local Address Space 3 Bus Region Descriptor	0080h
5Eh	LSW of Local Address Space 3 Bus Region Descriptor	0000h
60h	MSW of Expansion ROM Bus Region Descriptor	0000h
62h	LSW of Expansion ROM Bus Region Descriptor	0000h
64h	MSW of Chip Select 0 Base Address	0BFFh
66h	LSW of Chip Select 0 Base Address	FFC1h
68h	MSW of Chip Select 1 Base Address	0000h
6Ah	LSW of Chip Select 1 Base Address	4001h
6Ch	MSW of Chip Select 2 Base Address	0000h
6Eh	LSW of Chip Select 2 Base Address	0000h
70h	MSW of Chip Select 3 Base Address	0000h
72h	LSW of Chip Select 3 Base Address	0000h
74h	Serial EEPROM Write-Protected Address Boundary	0030h
76h	LSW of Interrupt Control/Status	0041h
78h	MSW of Target Response, Serial EEPROM, and initialization Control	0870h
7Ah	LSW of Target Response, Serial EEPROM, and initialization Control	0000h
7Ch	MSW of General Purpose I/O Control	0024h
7Eh	LSW of General Purpose I/O Control	9864h
80h	MSW of Hidden 1 Power Management Data Select	0000h
82h	LSW of Hidden 1 Power Management Data Select	0000h
84h	MSW of Hidden 2 Power Management Data Select	0000h
86h	LSW of Hidden 2 Power Management Data Select	0000h

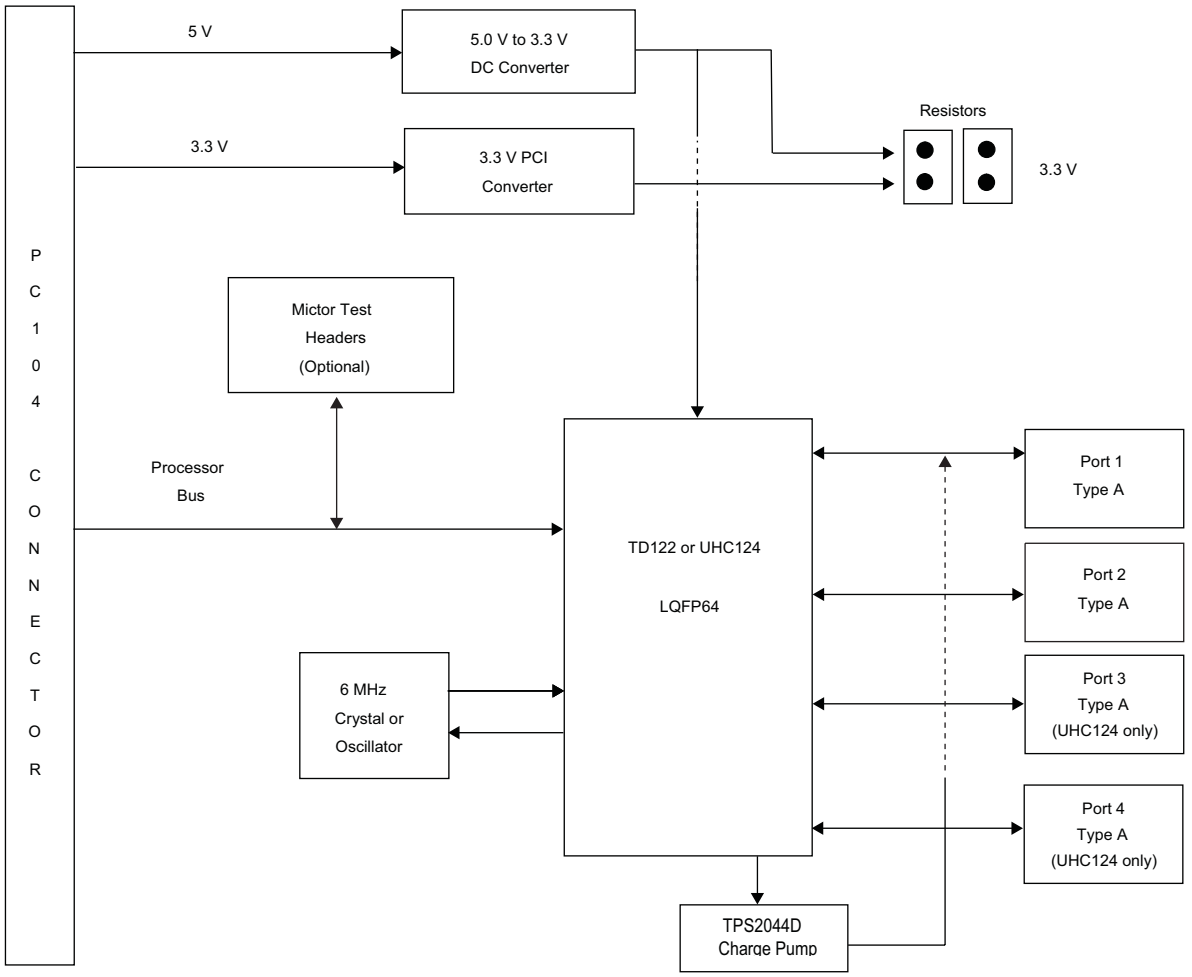
Chapter 2

EV-TD122-UHC124 Evaluation Board

Overview

This chapter describes the hardware operation and configuration options available for the EV-TD122-UHC124 in stand-alone mode. These options allow customers to directly connect the TD122 or the UHC124 to their embedded processor or CPU without going through a PCI bus. The use of this board without the PCI bridge card increases performance and allows driver development in real-world applications of the product. Figure 2-1 shows the EV-TD122-UHC124 block diagram.

Figure 2-1 EV-TD122-UHC124 Block Diagram



Board Operation Require-ments

When used with the PCI104 board, the EV-TD122-UHC124 board is powered by the PCI bus.

If the EV-TD122-UHC124 board is not used with the PCI104, the EV-TD122-UHC124 requires a DC power source capable of supplying 5 V ± 10% at 1.0 A through a power switch.

Default Configurations

The following factory default settings support the development of the TD122 USB host for Port 1 and Port 2:

- R54, R55 (0_1206 Ω) populated to route 5 V from the PCI104 connectors
- R49 (0_1206 Ω) populated for 3.3 V from the voltage regulator
- R23, R29, R31, R33 (0 Ω) populated for non-multiplex mode (MODE = 1)
- R26 (4.7 kΩ) populated for non-multiplex mode (MODE = 1)
- R38 (0 Ω) populated for /ADS signal inversion
- R5, R9 (4.7 kΩ) populated when the TD122 is installed
- R35, R52, R14, R41 (4.7 kΩ) populated for control signals pull-ups
- U1, U3, U5, U7 (with an STF201-30) populated for ESD protection, series resistance, and pull-downs to match impedance

Optional Configurations

If the UHC124 is installed in U10, R6 and R8 (4.7 kΩ) are installed as pull-ups. This allows all four standard-A ports to be used.

To use the EV-TD122-UHC124 in multiplex mode (MODE = 0):

1. Install a 0 Ω resistor in R24, R28, R32, R34.
2. Remove the 0 Ω resistor from R23, R29, R31, R33.
3. Install R27 (4.7 kΩ) and remove R26.

If the ADS input signal is already active high and does not need to be inverted, install R36 (0 Ω) and remove R38.

To use 3.3 V from the PCI connector, install R47 (0_1206 Ω) and remove R49.

To use a different ESD protection part, USBDF01W5, install U2, U4, U6, U8 (USBDF01W5) and remove U1, U3, U5, U7 (STF210-30). Semtech STF201-30 has $D_P/D_M/V_{BUS}$ ESD protection with 30 Ω series resistance and 15 kΩ pull-down. ST Micro USBDF01W5 has D_P/D_M ESD protection with 33 Ω series resistance and 15 kΩ pull-down.

Power Distribution

5 V Power Supply

The EV-TD122-UHC124 5 V power is supplied by one of two sources. The source is resistor selectable:

1. From the PC104 connector, by installing R54 and R55 (0 Ω) near the PC104 connector (default setting).
2. From an external power supply connected to JP9.3. Protection circuitry is not provided (remove R54 and R55).

3.3 V Power Supply

The EV-TD122-UHC124 3.3 V power is supplied by one of three sources:

1. From U12, a 5 V-to-3.3 V DC converter (default setting).
2. From the PC104 connector. Install R47 (0_1206 Ω) and remove R49.
3. From an external power supply connected to the test pin on JP7.3. Protection circuitry is not provided (remove R47 and R49).

Reset

The /RESET pin of the TD122 or UHC124 is connected to the PC104 connector. Users can control /RESET through a CPU GPIO.

D_P/D_M Signals

- Each of the D_P/D_M pairs has a 2-pin, 0.1 inch spacing, connector to support attachment of a differential probe (JP1-JP4)
- These traces are impedance controlled to 90 Ω ± 10%

LEDs

The EV-TD122-UHC124 has the following LEDs to enable monitoring of the normal operation of the board:

- D1-D4: Type A VBUS Power Indicator
- D5: 3.3 V Power Rail Indicator
- D6: 5 V Power Rail Indicator

Oscillator Input

Use of a 6 MHz crystal, instead of a crystal oscillator, is recommended to lower EMI. The only footprint provided in the EV-TD122-UHC124 board uses a 6 MHz crystal located at Y1 (Ecliptek Corp., E2SAA18-6.000M, 18 pF internal load).

Mounting Holes

The EV-TD122-UHC124 board has four un-plated standoff holes, one near each corner of the board. Each hole is 0.146 inch in diameter. The placement matches the PCI104 PCI board which together make the EV-TD122-UHC124-PCI.

Test Points

The following test points are furnished on the EV-TD122-UHC124:

- Ground Test Points JP5, JP6, JP8, and JP10
- Power Test Points TP1-TP4, TP5

Chapter 3

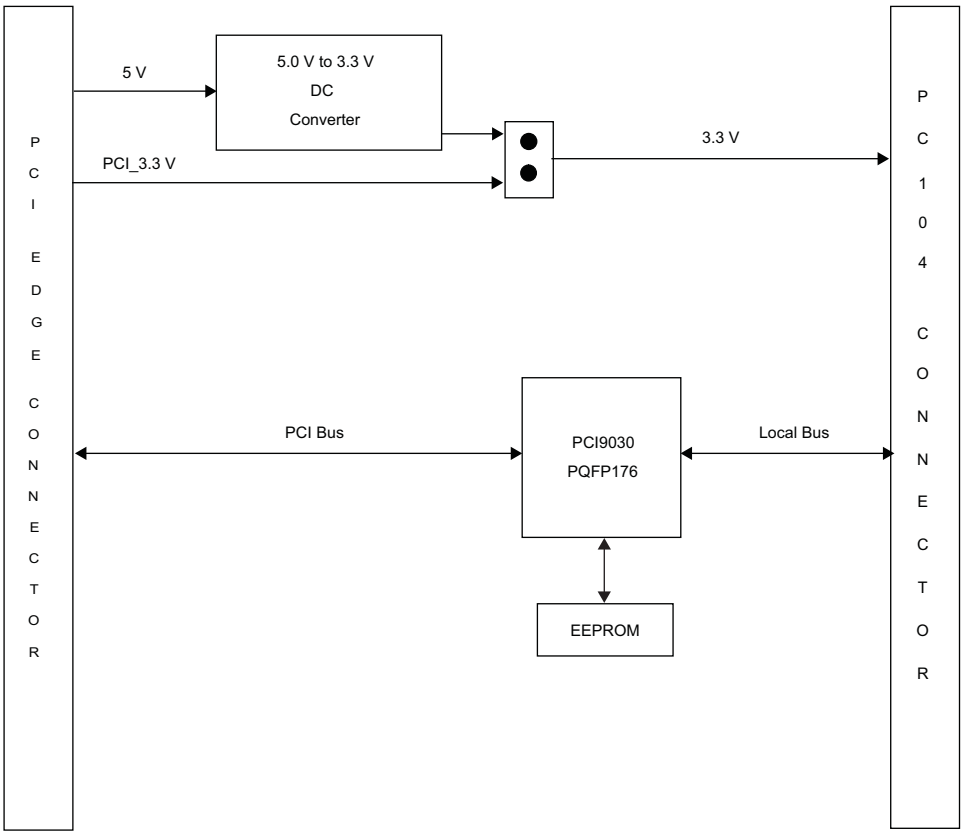
PCI104 Bridge Board

Overview

The PCI104 contains a PLX Technology PCI9030 bridge chip, an Atmel AT93C66A-10PI-2.7, a ROM socket, and three connectors.

The PCI104 board bridges between the PCI bus and the TD122-UHC124 local bus. The local bus is routed out to the standard PC104 connectors (J1 and J2). The EV-TD122-UHC124 interfaces to the PCI104 Bridge Card via these three female connectors. Another proprietary, non-PC104 connector (J3) was added to support a 32-bit interface and additional signals not included in the PC104 signal definition. Figure 3-1 shows the PCI104 block diagram.

Figure 3-1 PCI104 Bridge Board



The PCI104 board uses the PCI9030 bridge device. The PCI configuration registers are stored in an on-board EEPROM.

Power Distribution

The PCI104 board gets its 5 V power from the standard PCI bus edge connector (U2 – eight 5 V pins). The 5 V supply is routed directly to the EV-TD122 via the PC104 connectors (J1.D16, J2.B3, J2.B29).

The PCI104 board 3.3 V power is supplied by one of two sources:

1. 5.0 V-to-3.3 V DC regulator (U1). Install jumper on JP2 pin 1-2, 3-4 (default setting)
2. The standard PCI bus edge connector (U2 – twelve 3.3 V pins). Install jumper on JP2 pin 5-6, 7-8

Local Bus Configuration

The PCI9030 local bus is connected directly to the EV-TD122-UHC124 board via the PC104 connectors. Refer to the *PCI9030 Data Book* for a detailed explanation of its operation.

PCI9030 CS1L chip select is routed to the EV-TD122-UHC124. Register Space 1 of the PCI9030 controls CS1L. The number values programmed into Space 1 registers of the EEPROM are shown below. Changing values in the EEPROM requires an application from PLX operating across the PCI bus. Space 1 has 8-bit local and PCI space and contains 4 Kb memory space size. There is no prefetch on space 1.

- Space 1 Range 0xFFFF_F000
- Space 1 Remap 0x0000_0001
- Space 1 Descriptor 0x4013_F940
- Space 1 Base Address 0x0000_0801
- Space 1 Initialization Control 0x0030_0041

The local timing is five WAIT states for READs (address-to-data) and seven for WRITEs (address-to-data) to make the PCI104 backwards compatible with previous Oxford Semiconductor chips. The other WAIT states are: three RD (data-to-data), three RD/WR (data-to-address), one WR (data-to-data), and one WR cycle hold. An optimum bus access will not create a significant increase in performance in the EV-TD122-UHC124-PCI system. For better performance evaluation, the TD122 and UHC124 should be embedded directly on the system bus using the EV-TD122-UHC124 board.

Local Bus Speed

LCLK, the local bus clock, operates at frequencies up to 60 MHz and is asynchronous to the PCI bus clock, BCLK. BCLK is routed back into LCLK, setting the default local bus speed at 33 MHz.

An oscillator up to 60 MHz can be soldered at the U4/U5 dual-footprint by the customer to increase the local bus speed. R10 (33 Ω) must be installed and R11 removed in this configuration. More WAIT states may have to be added to meet the TD122-UHC124 interface timing when increasing the local bus frequency.

LEDs

The PCI104 has two LEDs to enable verification of the normal operation of the board.

- D1: 3.3 V Power Rail Indicator
- D2: 5.0 V Power Rail Indicator

Mounting Holes

The PCI104 board has four un-plated standoff holes, one near each corner of the board. Each hole is 0.146″ in diameter. The placement matches the EV-TD122-UHC124 evaluation board which togther make the EV-TD122-UHC124-PCI.

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Schematics

Overview

This chapter provides the EV-TD122-UHC124 and PCI104 schematics. The term “EVB12X” refers to the EC-TD122-UHC124 board. U10 is shown as a “TD12X”, which refers to either the TD122 or UHC124 USB chip, depending on the installation.

Figure 4-1 EV-TD122-UHC124 Top-Level Schematic

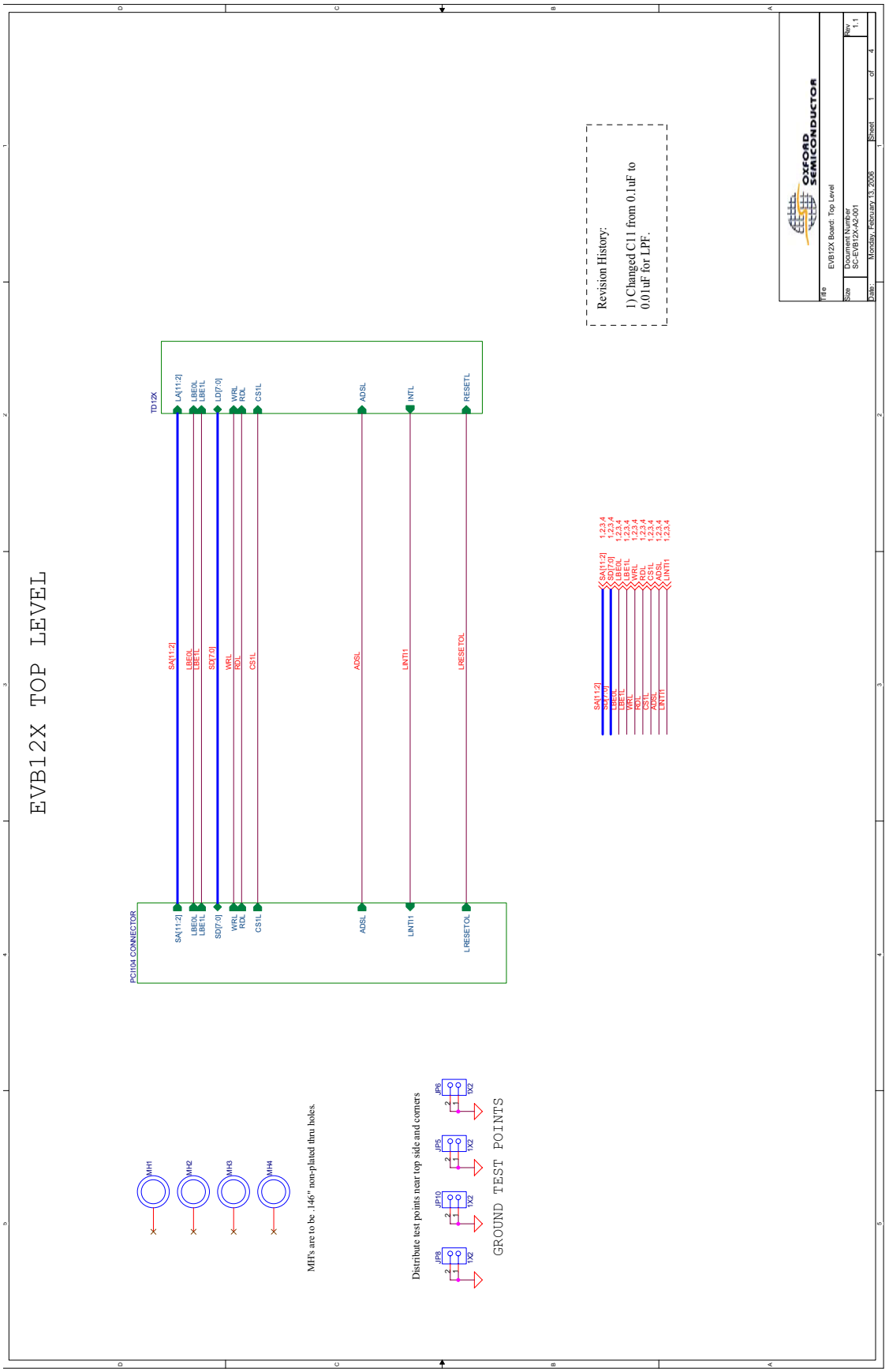

Figure 4-2 EV-TD122-UHC124 Test Headers

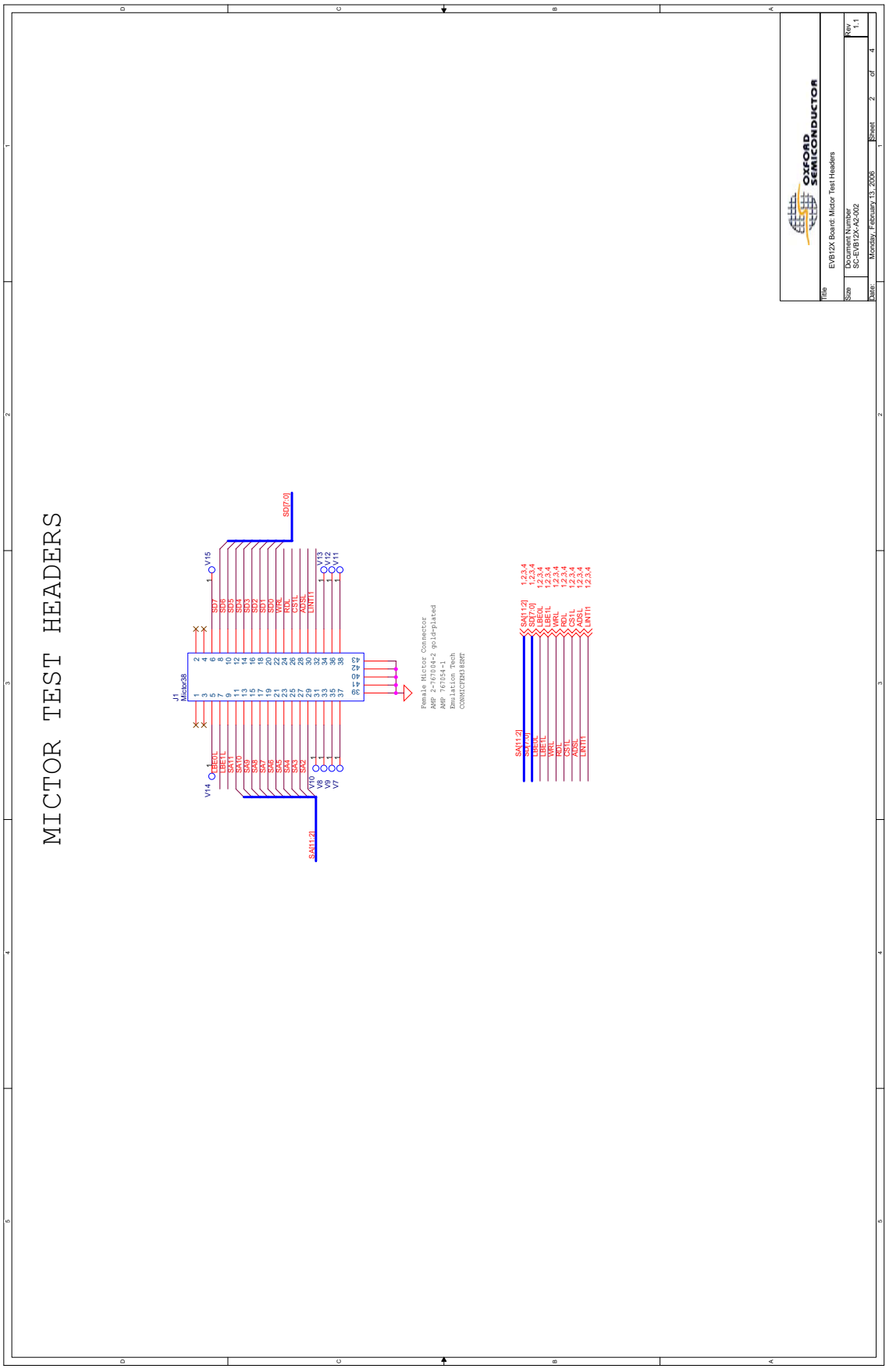

Figure 4-3 EV-TD122-UHC124 PC104 Connector

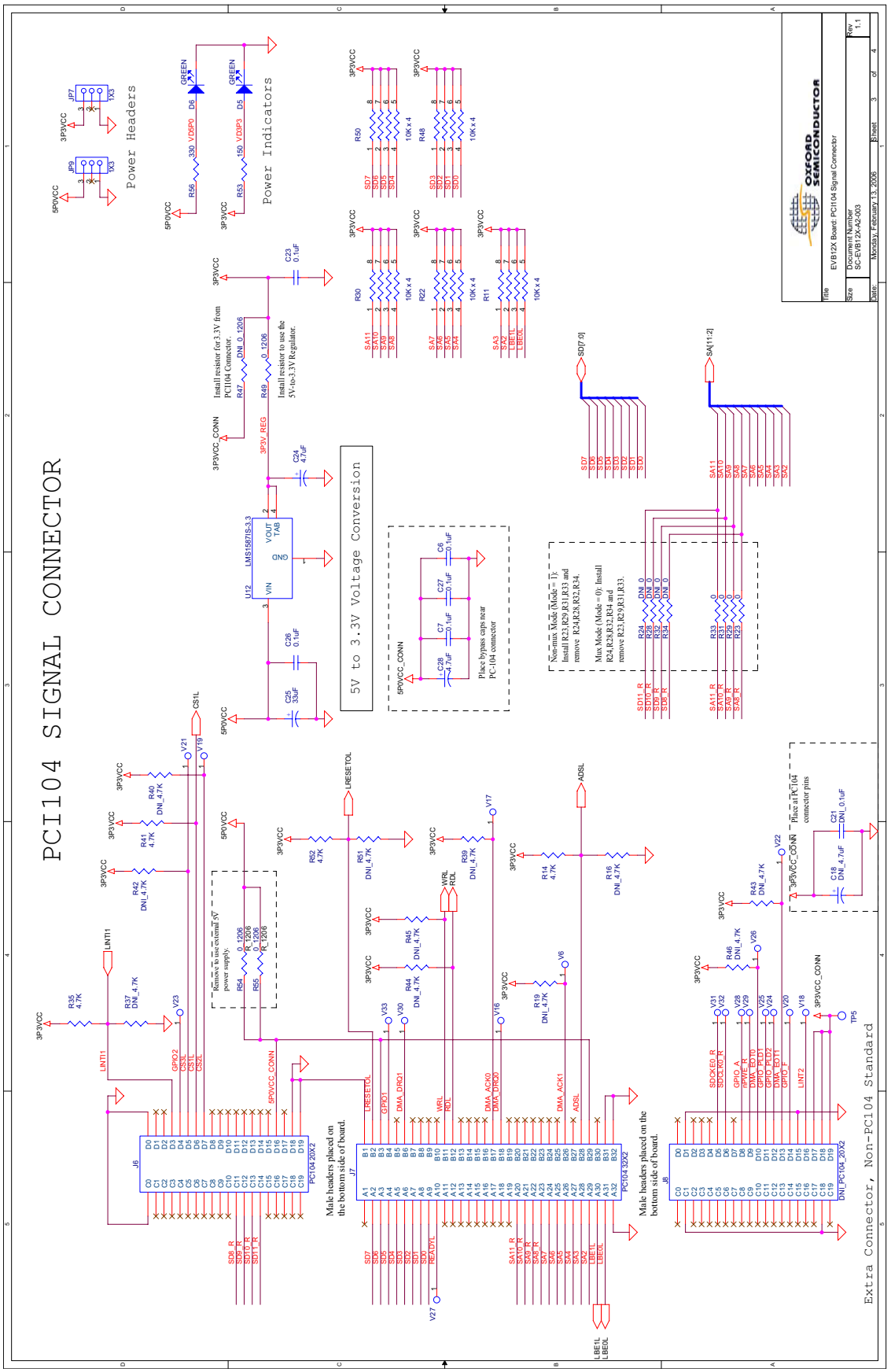

Figure 4-4 EV-TD122-UHC124 - TD12X and USB Ports Schematic

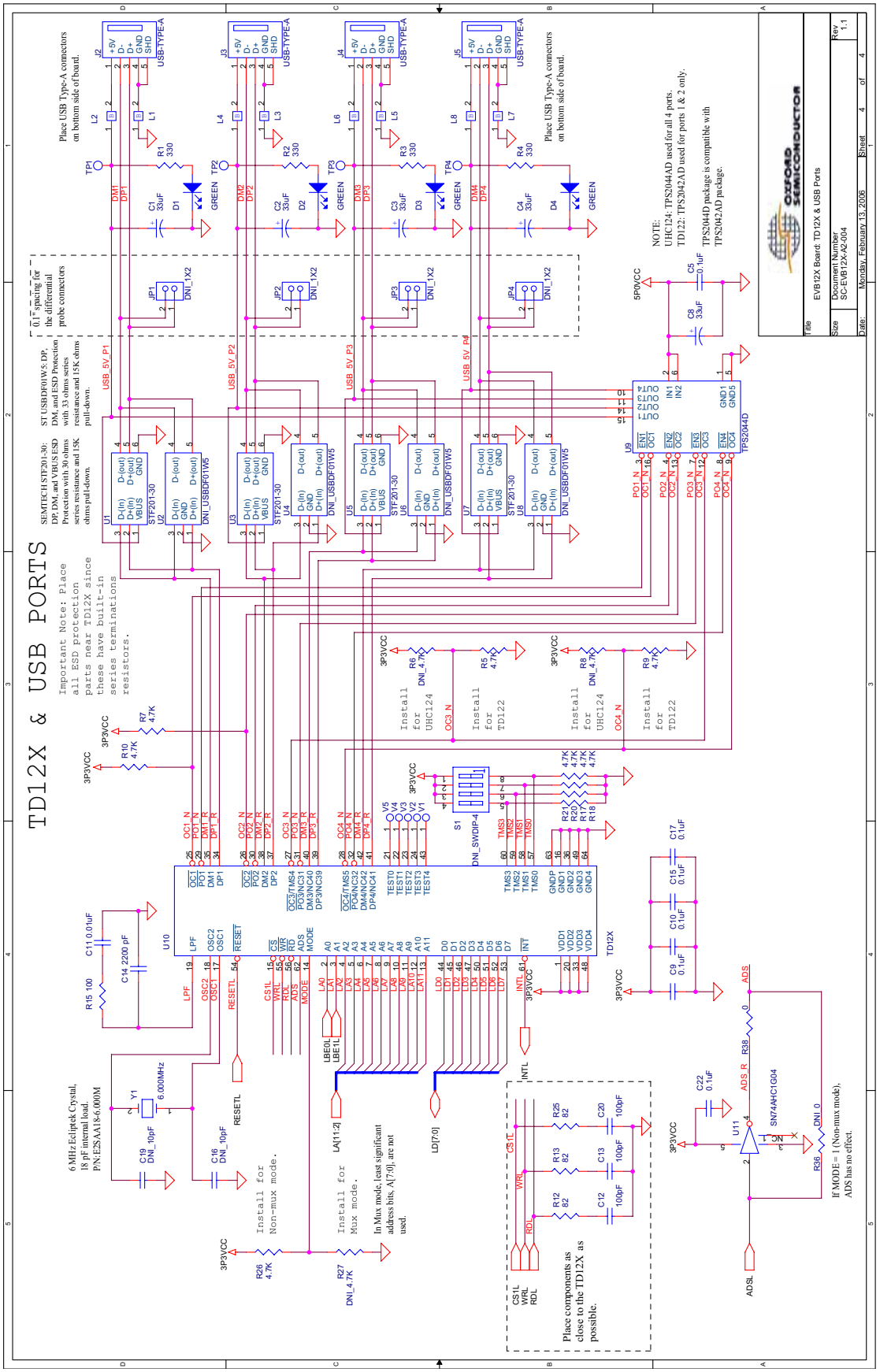

Figure 4-5 PCI104 Top-Level Schematic

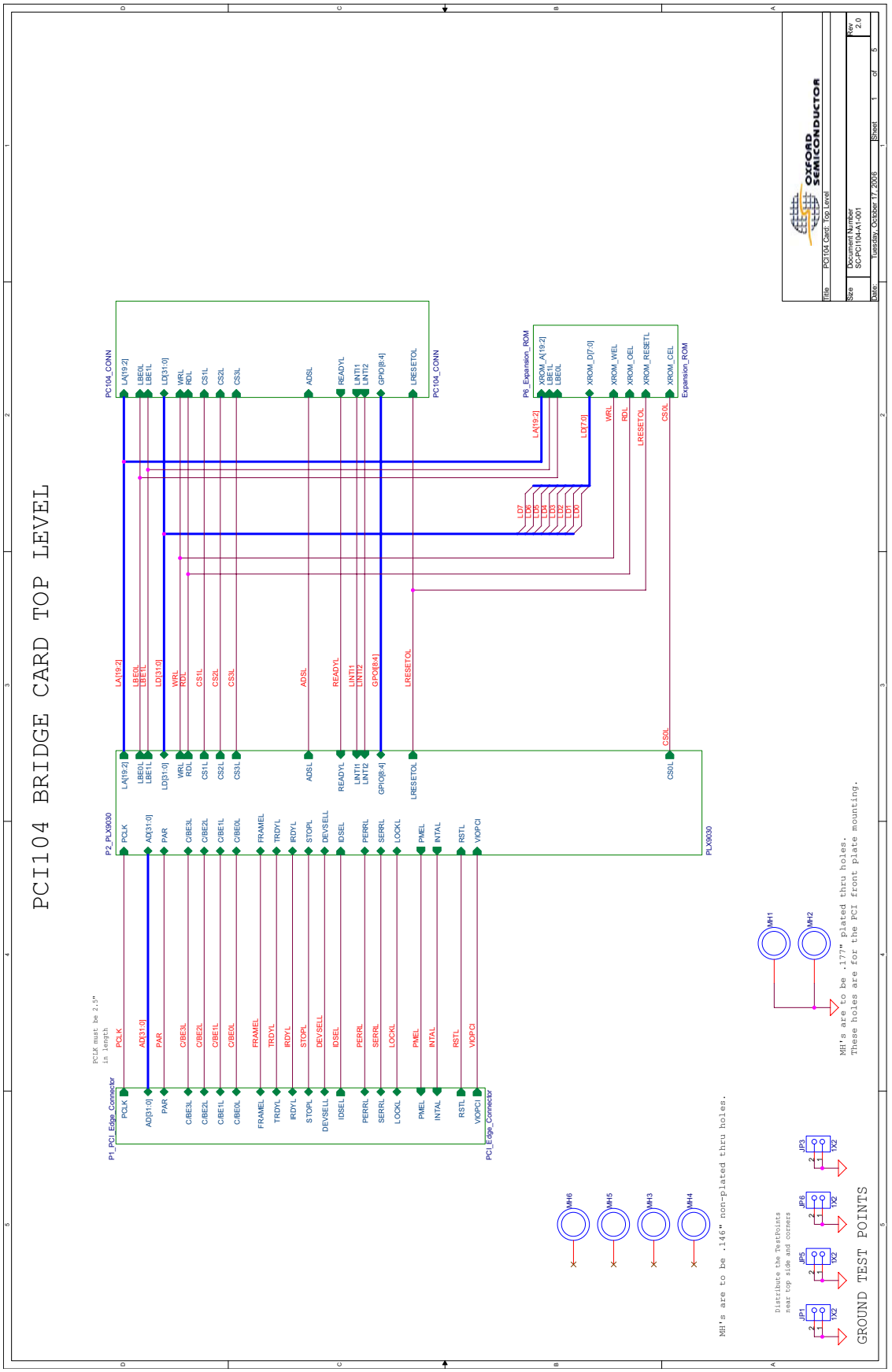

Figure 4-6 PCI104 PCI Connector

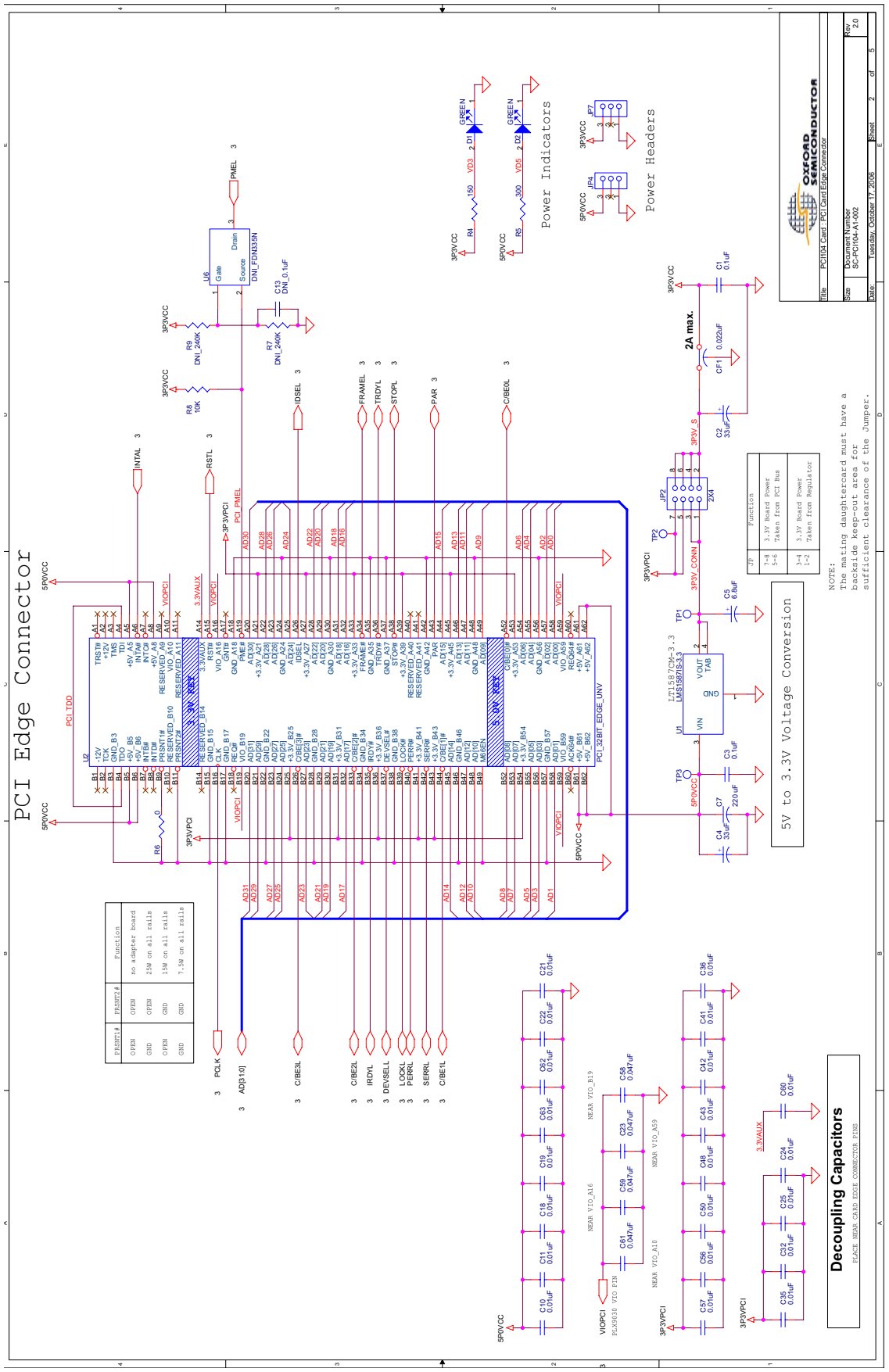

Figure 4-7 PCI9030 Bridge Chip

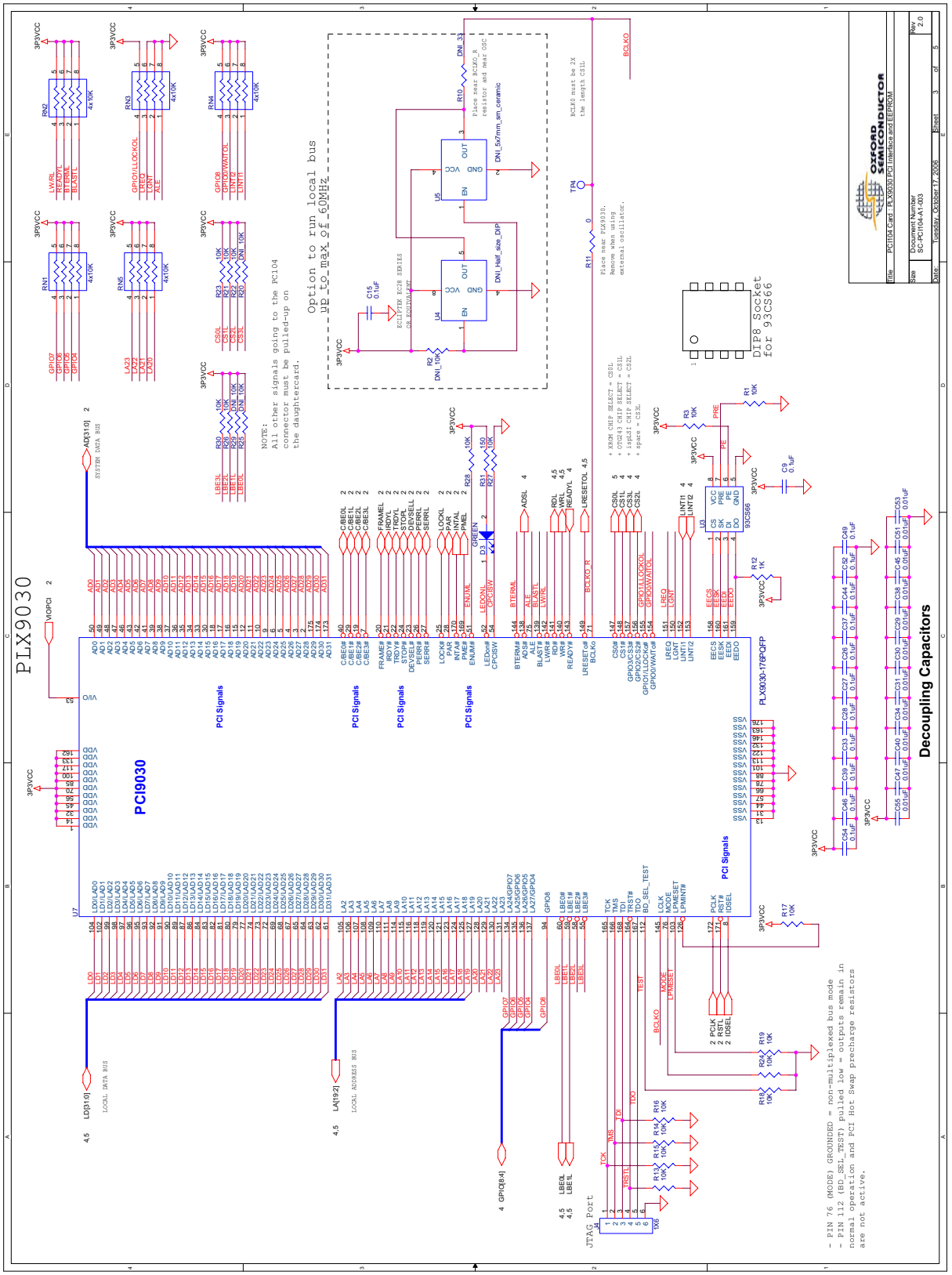

Figure 4-8 PC104 Connectors

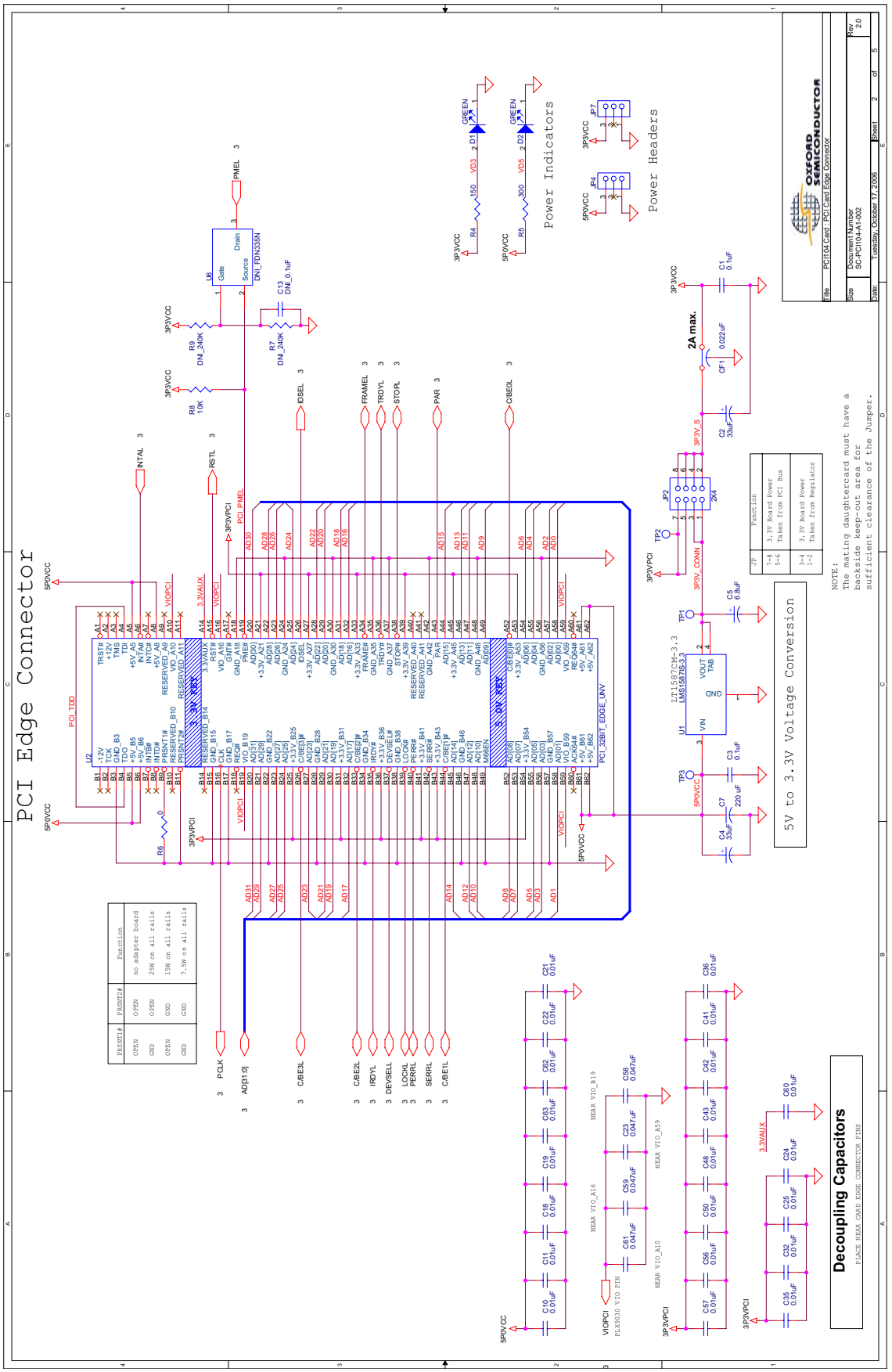

Figure 4-9 PC104 Expansion ROM