## SiHK155N60E

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Vishay Siliconix

### **E Series Power MOSFET**

#### PowerPAK® 10 x 12 TAB TAB TAB PowerPAK® 10 x 12 TAB TAB PowerPAK® 10 x 12 TAB PowerPAK® 10 x

PRODUCT SUMMARY					
V <sub>DS</sub> (V) at T <sub>J</sub> max.	650				
R <sub>DS(on)</sub> typ. (Ω) at 25 °C	$V_{GS} = 10 V$	0.135			
Q <sub>g</sub> max. (nC)	36				
Q <sub>gs</sub> (nC)	10				
Q <sub>gd</sub> (nC)	6				
Configuration	Single				

### FEATURES

- 4<sup>th</sup> generation E series technology
- Low figure-of-merit (FOM) Ron x Qg
- Low effective capacitance (Co(er))
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

#### **APPLICATIONS**

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Solar (PV inverters)

ORDERING INFORMATION	
Package	PowerPAK <sup>®</sup> 10 x 12
Lead (Pb)-free and halogen-free	SiHK155N60E-T1-GE3

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25$ °C, unless otherwise noted)							
PARAMETER			SYMBOL	LIMIT	UNIT		
Drain-source voltage			V <sub>DS</sub>	600	- V		
Gate-source voltage			V <sub>GS</sub>	± 30	v		
Continuous drain current (T <sub>J</sub> = 150 °C)	Vac at 10 V	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	19			
	VGS AL TO V	$V_{GS}$ at 10 V $T_{C} = 100 \text{ °C}$		12	А		
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	43			
Linear derating factor				1.04	W/°C		
Single pulse avalanche energy <sup>b</sup>			E <sub>AS</sub>	179	mJ		
Maximum power dissipation			PD	156	W		
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C		
Drain-source voltage slope $T_J = 125 \text{ °C}$		du (dt	100	V/ns			
Reverse diode dv/dt <sup>d</sup>			dv/dt	5	v/ns		

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature

- b.  $V_{DD}$  = 120 V, starting T<sub>J</sub> = 25 °C, L = 28.2 mH, R<sub>g</sub> = 25  $\Omega$ , I<sub>AS</sub> = 2.8 A
- c.  $I_{SD} \leq I_D, \, di/dt$  = 100 A/µs, starting  $T_J$  = 25  $^\circ C$





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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R <sub>thJA</sub>	-	50 <sup>a</sup>	°C/W	
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	0.96	0/10	

Note

a. When mounted on 1" x 1" FR4 board

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static				•		•	
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> =	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		-	-	V
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I <sub>D</sub> = 1 mA	-	0.62	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> =	: V <sub>GS</sub> , I <sub>D</sub> = 250 μΑ	3.0	-	5.0	V
	I <sub>GSS</sub>	$V_{GS} = \pm 20 V$		-	-	± 100	nA
Gate-source leakage			V <sub>GS</sub> = ± 30 V	-	-	± 1	μA
		V <sub>DS</sub> =	: 600 V, V <sub>GS</sub> = 0 V	-	-	1	
Zero gate voltage drain current	IDSS	V <sub>DS</sub> = 480 V	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 \text{ °C}$		-	10	μA
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A	-	0.135	0.155	Ω
Forward transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 10 \text{ A}$		-	5.1	-	S
Dynamic							<u>.                                    </u>
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V,		-	1514	-	pF
Output capacitance	C <sub>oss</sub>	- ,	$V_{GS} = 0 V,$ $V_{DS} = 100 V,$		60	-	
Reverse transfer capacitance	C <sub>rss</sub>	f = 100 KHz		-	2	-	
Effective output capacitance, energy related	C <sub>o(er)</sub>	$V_{DS}$ = 0 V to 400 V, $V_{GS}$ = 0 V		-	58	-	
Effective output capacitance, time related	C <sub>o(tr)</sub>			-	322	-	
Total gate charge	Qg			-	24	36	
Gate-source charge	Q <sub>gs</sub>	$V_{GS} = 10 V$	$V_{GS} = 10 \text{ V}$ $I_D = 10 \text{ A}, V_{DS} = 480 \text{ V}$		10	-	nC
Gate-drain charge	Q <sub>gd</sub>	1 [		-	6	-	
Turn-on delay time	t <sub>d(on)</sub>	$V_{DD} = 480 \text{ V}, \text{ I}_{D} = 10 \text{ A},$ $V_{GS} = 10 \text{ V}, \text{ R}_{g} = 9.1 \Omega$		-	20	40	- ns
Rise time	t <sub>r</sub>			-	27	54	
Turn-off delay time	t <sub>d(off)</sub>			-	28	56	
Fall time	t <sub>f</sub>			-	17	34	
Gate input resistance	Rg	f = 1 MHz, open drain		0.4	0.9	1.8	Ω
Drain-Source Body Diode Characteristic	S	•		•	•	•	
Continuous source-drain diode current	I <sub>S</sub>	showing the	MOSFET symbol showing the		-	22	
Pulsed diode forward current	I <sub>SM</sub>	p - n junction diode		-	-	43	- A
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	$T_{J} = 25 \text{ °C}, I_{F} = I_{S} = 10 \text{ A},$ di/dt = 100 A/µs, V <sub>R</sub> = 25 V		-	291	582	ns
Reverse recovery charge	Q <sub>rr</sub>			-	3.5	7.0	μC
Reverse recovery current	I <sub>BBM</sub>			-	21	-	A

#### Notes

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ 

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### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

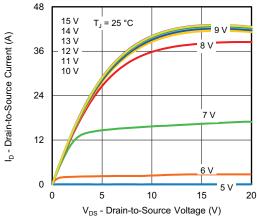


Fig. 1 - Typical Output Characteristics

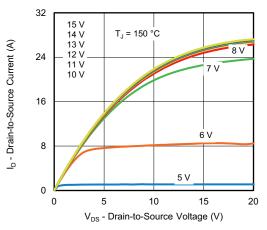


Fig. 2 - Typical Output Characteristics

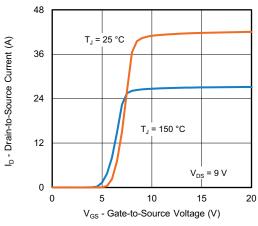


Fig. 3 - Typical Transfer Characteristics

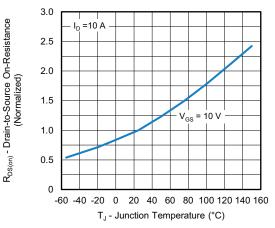


Fig. 4 - Normalized On-Resistance vs. Temperature

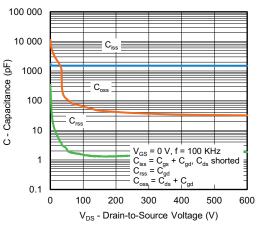


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

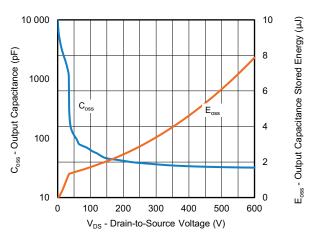


Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$ 

S22-1060-Rev. A, 26-Dec-2022

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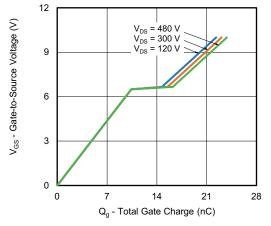


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

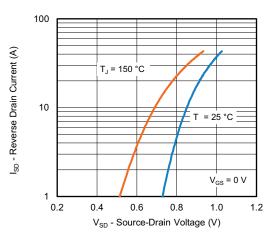


Fig. 8 - Typical Source-Drain Diode Forward Voltage

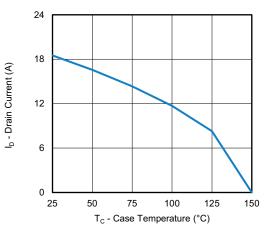


Fig. 9 - Maximum Drain Current vs. Case Temperature

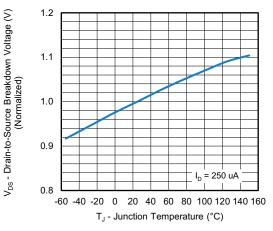


Fig. 10 - Temperature vs. Drain-to-Source Voltage

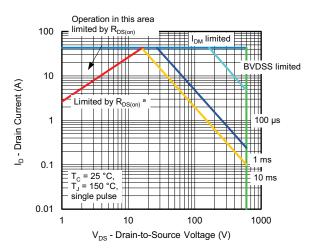


Fig. 11 - Maximum Safe Operating Area

#### Note

c.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

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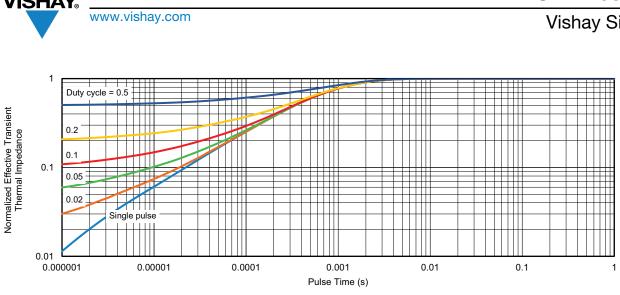


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

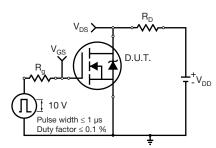


Fig. 13 - Switching Time Test Circuit

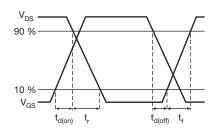


Fig. 14 - Switching Time Waveforms

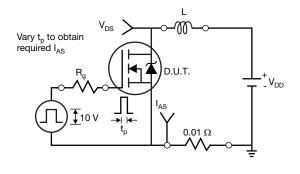


Fig. 15 - Unclamped Inductive Test Circuit

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V<sub>DD</sub>  $V_{DS}$ I<sub>AS</sub>

DS

Fig. 16 - Unclamped Inductive Waveforms

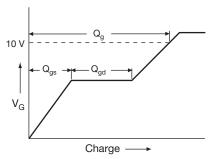
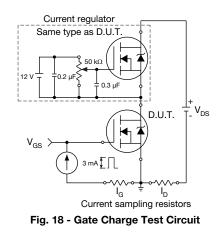
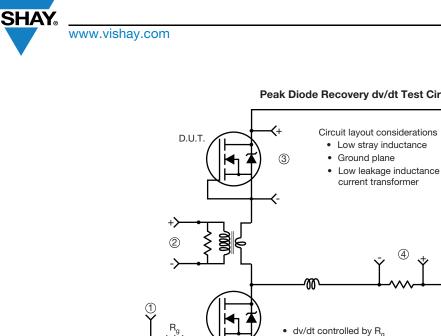


Fig. 17 - Basic Gate Charge Waveform



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#### Peak Diode Recovery dv/dt Test Circuit

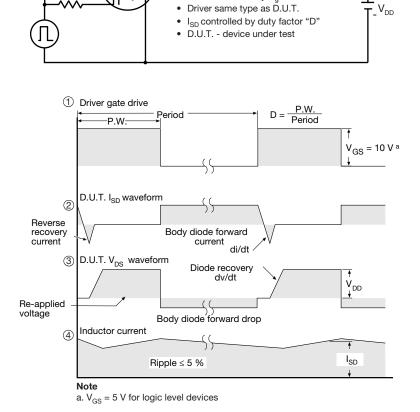


Fig. 19 - For N-Channel

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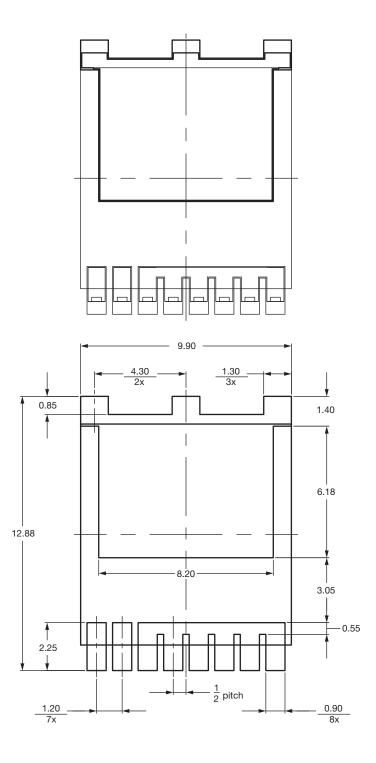
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### **PAD** Pattern



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# Recommended Land Pattern PowerPAK<sup>®</sup> 10 x 12 (TOLL) (High Voltage)



#### Note

• Dimensions in mm

ECN: S22-1061-Rev. C, 26-Dec-2022 DWG: 3013

Revision: 26-Dec-2022

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