



Product Change Notification / ALAN-22WDFU453

Date:

16-Mar-2023

Product Category:

Switching Regulators

PCN Type:

Manufacturing Change

Notification Subject:

CCB 4386.002 Final Notice: Qualification of Microchip Technology Tempe - Fab 2 (TMGR) as new fabrication site for Die#2 and Die#3 for selected MIC2851xx device families in 32L VQFN (6x6x0.9mm) package.

Affected CPNs:

[ALAN-22WDFU453_Affected_CPN_03162023.pdf](#)

[ALAN-22WDFU453_Affected_CPN_03162023.csv](#)

Notification Text:

PCN Status:Final Notification

PCN Type:Manufacturing Change

Microchip Parts Affected:Please open one of the files found in the Affected CPNs section.

Note: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

Description of Change:Qualification of Microchip Technology Tempe - Fab 2 (TMGR) as new fabrication site for Die#2 and Die#3 for selected MIC2851xx device families in 32L VQFN (6x6x0.9mm) package.

Pre and Post Change Summary:

	Pre Change	Post Change
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Fabrication Location	Die # 1	Microchip Technology Colorado (MCSO)	Microchip Technology Colorado (MCSO)
	Die # 2	MaxPower Semiconductor (MAPW)	Microchip Technology Tempe - Fab 2 (TMGR)
	Die # 3	MaxPower Semiconductor (MAPW)	Microchip Technology Tempe - Fab 2 (TMGR)
Wafer Size	Die # 1	6 inches	6 inches
	Die # 2 and Die # 3	8 inches	8 inches

Impacts to Data Sheet:None

Change Impact:None

Reason for Change:To improve manufacturability and on-time delivery performance by qualifying TMGR as new fabrication site for Die#2 and Die#3.

Change Implementation Status:In Progress

Estimated First Ship Date:March 31, 2023 (date code: 2313)

Note: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Time Table Summary:

	September 2022					>	March 2023				
Workweek	3 6	3 7	3 8	3 9	4 0		0 9	1 0	1 1	1 2	1 3
Initial PCN Issue Date			x								
Qual Report Availability									x		
Final PCN Issue Date									x		
Estimated Implementation Date											x

Method to Identify Change:Traceability code

Qualification Report:Please open the attachments included with this PCN labeled as PCN_#_Qual_Report.

Revision History:

September 13, 2021: Issued initial notification.

March 16, 2023: Issued final notification. Attached the Qualification Report. Provided estimated first ship date to be on March 31, 2023.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

[PCN_ALAN-22WDFU453_Qual_Report.pdf](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

MIC28516T-E/PHA

MIC28516T-E/PHAVAO

MIC28517T-E/PHA

MIC28517T-E/PHAVAO



QUALIFICATION REPORT SUMMARY

PCN #: ALAN-22WDFU453

Date:

March 02, 2023

**Qualification of Microchip Technology Tempe - Fab 2 (TMGR)
as new fabrication site for Die#2 and Die#3 for selected
MIC2851xx device families in 32L VQFN (6x6x0.9mm)
package.**

Purpose: Qualification of Microchip Technology Tempe - Fab 2 (TMGR) as new fabrication site for Die#2 and Die#3 for selected MIC2851xx device families in 32L VQFN (6x6x0.9mm) package.

Summary:

In keeping with guidelines established in Microchip specification QCI-39000, three lots were used for qualification testing this MASK. The mask ID was changed from Q1008 to Q8G01 to differentiate between mask voltage options. This memo summarizes the activities and results.

Conclusion:

Based on the results, mask Q8G01 REV A0 (Q1008 or MCP1008-EH7C) complies with the reliability guidelines implemented in the CCB 4386 qualification plan. Therefore, the mask can be released to production.

Device Description:

Device	MCP1008-E/H7C
Mask	Q8G01 rev A0
CCB#	4386 and 4386.002
Document Control Number	ML022023007K
Document Revision	A

Qualification Material:

Test Lot	Lot 1	Lot 2	Lot 3	Lot 4
WAFER LOT	TMPE222088074.100	TMPE222088074.210	TMPE222088074.310	TMPE222088074.100
ASSEMBLY LOT	ASEM223400116.100	ASEM223400100.000	ASEM223400117.000	ASEM223400116.100
TRACE CODE	2146P1M	2146ES5	2146P2G	n/a
PACKAGE	8L VDFN56	8L VDFN56	8L VDFN56	8L VDFN56 (TO-220 SNAP-OUT)
REL STRESS TESTS	IOL, HTRB, HTGB, TC, UIS, uHAST,HAST	IOL, HTRB, HTGB, TC, UIS, uHAST,HAST	IOL, HTRB, HTGB, TC, UIS, uHAST,HAST	HBM, CDM

Qualification Results:

Intermittent Operating Life (IOL)

Test Method/Condition	JEDEC J-STD-020D and JESD22-A11, MSL Level 3 soak, 260°C peak 3x Reflow Temperature
Lot #	Results (Fail/Pass)
Lot 1: ASEM223400116.000	0/80
Lot 2: ASEM223400100.000	0/80
Lot 3: ASEM223400117.000	0/80
Test Method	AEC Q101: MIL-STD-750 Method 1037
Test Condition	Cycle Read points- 0, 5k, 10k, 15k cycles Each Cycle Time- 243 sec
Sample Size = 80	(Fail/Pass)
Lot 1, 2, 3	0 / 240

Pre & Post Testing was done @ +25°C

High Temperature Reverse Bias (HTRB)

Test Method	AEC Q101: MIL-STD-750-1
Test Condition	125°C / 1000 hours with Bias Voltage of 80Vds Cycle Read points- 0hr, 24hrs, 500hrs, 1000hrs
Sample Size = 80	(Fail/Pass)
Lot 1, 2, 3	0 / 240

Pre & Post Testing was done @ +25°C

High Temperature Gate Bias (HTGB)

Test Method	AEC Q101: JESD22-A-108
Test Condition	125°C / 1000 hours with Bias Voltage of 10Vgs Cycle Read points- 0hr, 24hrs, 500hrs, 1000hrs
Sample Size = 80	(Fail/Pass)
Lot 1, 2, and 3	0 / 240

Pre & Post Testing was done @ +25°C

ESD HBM, CDM, Unclamped Inductive Switching (UIS)

Test	Reference Method	Sample Size	Highest Passing Voltage
ESD – HBM	AEC Q101-001A: JS-001-2017	30 / Lot	+/- 2000V (Drain wrt Source, Gate)
ESD – HBM	AEC Q101-001A: JS-001-2017	30 / Lot	+/- 1000V (all possible pin-pair combinations)
ESD – CDM	AEC Q101-005A	60 / Lot	+/- 2000V
UIS	AEC Q101-004 Section 2	5 / Lot 4 5 / Lot 4 5 / Lot 4	Tested at 1mH

Pre & Post Testing done @ +25°C.

Package Qualification Data:**Package Pre-conditioning**

Test Method/Condition	JEDEC J-STD-020D and JESD22-A11, MSL Level 3 soak, 260°C peak 3x Reflow Temperature
Lot #	Results (Fail/Pass)
Lot 1: ASEM223400116.000	0/160
Lot 2: ASEM223400100.000	0/160
Lot 3: ASEM223400117.000	0/160

Pre and post testing was conducted at +25°C.

HAST (Highly Accelerated Temperature and Humidity Stress Test)

Test Method/Condition	JESD22-A110, Vin = +42V, Ta = +130°C/85%RH	
Lot #	96HR Results (Fail/Pass)	
Lot 1: ASEM223400116.000	0/80	
Lot 2: ASEM223400100.000	0/80	
Lot 3: ASEM223400117.000	0/80	

Pre and Post testing was conducted at +25°C.

Unbiased HAST

Test Method/Condition	JESD22-A118, Ta = +130°C/85% RH	
Lot #	96HR Results (Fail/Pass)	
Lot 1: ASEM223400116.000	0/80	
Lot 2: ASEM223400100.000	0/80	
Lot 3: ASEM223400117.000	0/80	

Pre and Post testing was conducted at +25°C.

Package Pre-conditioning

Test Method/Condition	JEDEC J-STD-020D and JESD22-A113F, MSL Level 1 soak 260°C peak 3x Reflow Temperature	
Lot #	Results (Fail/Pass)	
Lot 1: ASEM223400116.000	0/32	
Lot 2: ASEM223400100.000	0/32	
Lot 3: ASEM223400117.000	0/32	

Pre and Post testing was conducted at +25°C.

Temperature Cycling (TC)

Test Method	AEC Q101: JESD22-A-104 Appendix 6	
Test Condition	Temp Range- -65°C to 150°C, Cycle Read points- 0, 500, 1000 cycles	
Sample Size (30 min)	(Fail/Pass)	
Lot 1: ASEM223400116.000	0 / 32	
Lot 2: ASEM223400100.000	0 / 32	
Lot 3: ASEM223400117.000	0 / 32	

Pre and Post testing was conducted at +25°C.