

2.7 V to 5.5 V Input, 600 mA Single Synchronous Buck DC/DC Converter for Automotive

BD9S012NUX-C

General Description

BD9S012NUX-C is a synchronous buck DC/DC Converter with built-in low On Resistance power MOSFETs. It is capable of providing current up to 600 mA. Small inductor is applicable due to high switching frequency of 2.2 MHz. It is a current mode control DC/DC Converter and features high-speed transient response. It has an integrated feedback resistor that sets the output voltage to 1.1 V and a built-in phase compensation circuit. Applications can be created with a few external components.

Features

- AEC-Q100 Qualified^(Note 1)
- Single Synchronous Buck DC/DC Converter
- Adjustable Soft Start Function
- Output Discharge Function
- Power Good Output
- Input Under Voltage Lockout Protection (UVLO)
- Short Circuit Protection (SCP)
- Output Over Voltage Protection (OVP)
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)

(Note 1) Grade 1

Applications

- Automotive Equipment
- Other Electronic Equipment

Key Specifications

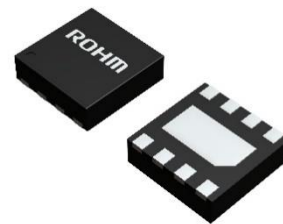
■ Input Voltage:	2.7 V to 5.5 V
■ Output Voltage:	1.1 V(Typ)
■ Output Current:	600 mA(Max)
■ Switching Frequency:	2.2 MHz(Typ)
■ High Side FET ON Resistance:	270 mΩ(Typ)
■ Low Side FET ON Resistance:	180 mΩ(Typ)
■ Shutdown Circuit Current:	0 μA(Typ)
■ Operating Temperature:	-40 °C to +125 °C

Package

VSON008X2020

W(Typ) x D(Typ) x H(Max)

2.00 mm x 2.00 mm x 0.60 mm



Typical Application Circuit

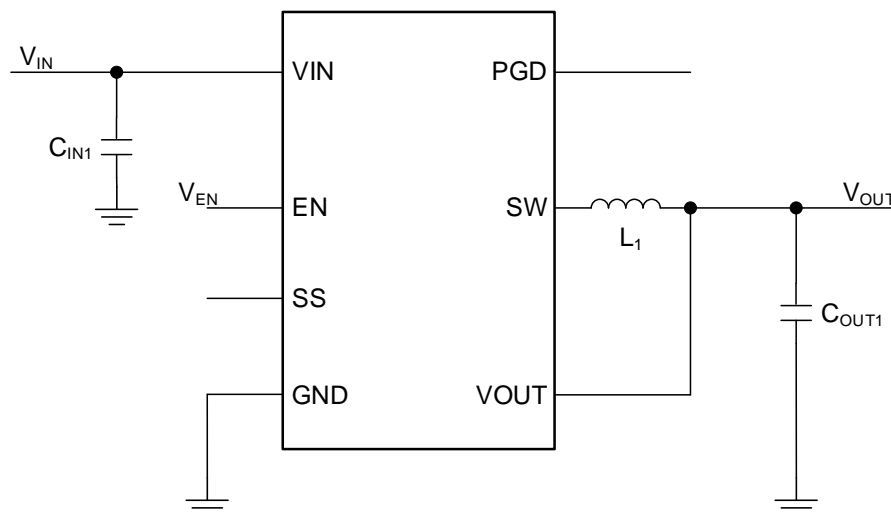
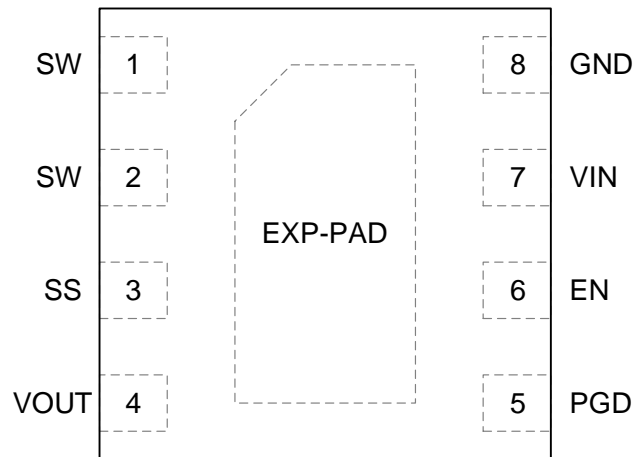


Figure 1. Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration



(TOP VIEW)

Pin Descriptions

Pin No.	Pin Name	Function
1, 2	SW	Switch pin. These pins are connected to the drain of the High Side FET and the Low Side FET.
3	SS	Pin for setting the soft start time. The rise time of the output voltage can be specified by connecting a capacitor to this pin. See page 17 for how to calculate the capacitance..
4	VOUT	V_{OUT} feedback pin. Connect to output voltage sense point.
5	PGD	Power Good pin, an open drain output. It is need to be pulled up to the power supply with the resistor. See page 11 for setting the resistance.
6	EN	Pin for controlling the device. Turning this pin Low forces the device to enter the shutdown mode. Turning this pin High makes the device to start up.
7	VIN	Power supply pin. Connecting a 10 μ F(Typ) ceramic capacitor is recommended. The detail of a selection is described in page 15 .
8	GND	Ground pin.
-	EXP-PAD	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using via provides excellent heat dissipation characteristics.

Block Diagram

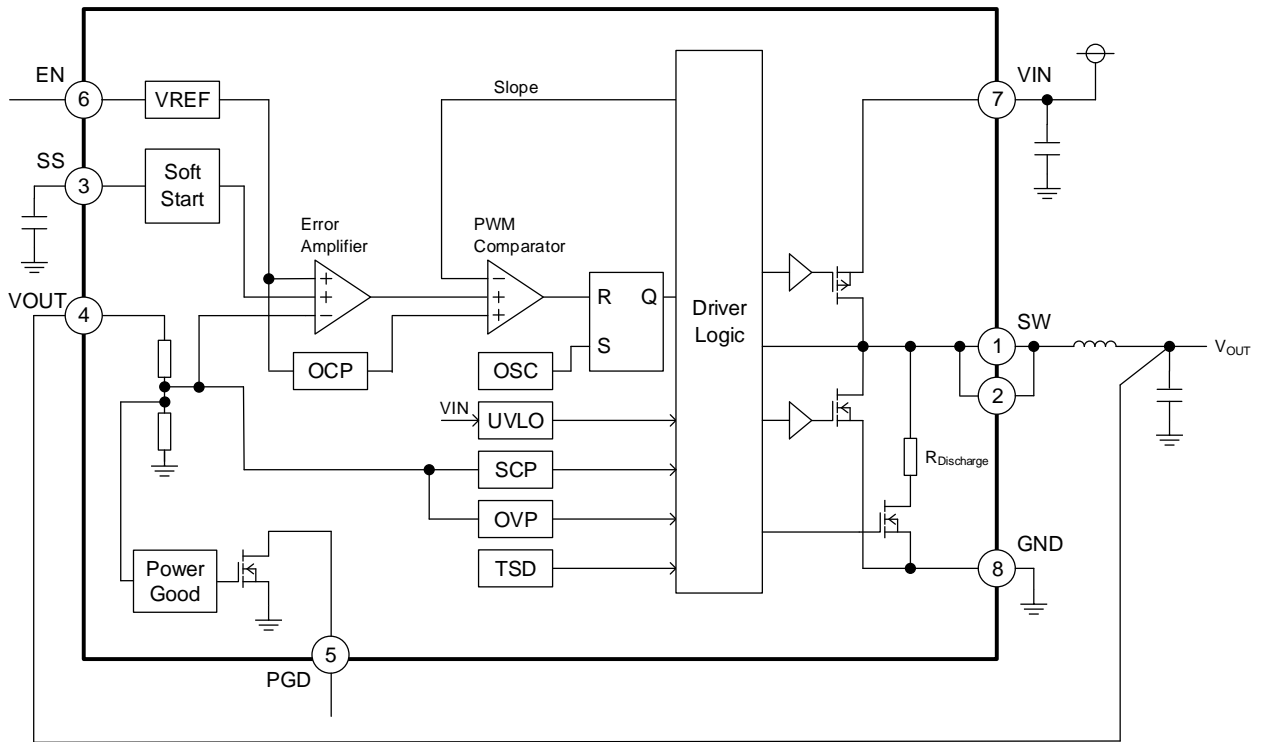


Figure 2. Block Diagram

Description of Blocks

1. VREF
The VREF block generates the internal reference voltage.
2. UVLO (Under Voltage Lockout)
The UVLO block is for under voltage lockout protection. It will shutdown the device when the V_{IN} falls to 2.45 V(Typ) or lower. The threshold voltage has a hysteresis of 100 mV(Typ).
3. SCP (Short Circuit Protection)
This is the short circuit protection circuit. After soft start is judged to be completed, if the VOUT pin voltage falls to 70 % (Typ) of the voltage setting or less and remain in that state for 1 ms(Typ), output MOSFET will turn OFF for 14 ms(Typ) and then restart the operation.
4. OVP (Over Voltage Protection)
This is the output over voltage protection circuit. When the VOUT pin voltage becomes +15 % (Typ) of the voltage setting or more, it turns the output MOSFET OFF. After output voltage falls +10 % (Typ) of the voltage setting or less, the output MOSFET returns to normal operation.
5. TSD (Thermal Shutdown)
This is the thermal shutdown circuit. It will shutdown the device when the junction temperature (T_j) reaches to 175 °C(Typ) or more. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation with hysteresis of 25 °C(Typ).
6. OCP (Over Current Protection)
The Over Current Protection function operates by limiting the current that flows through High Side FET at each cycle of the switching frequency.
7. Soft Start
The Soft Start circuit slows down the rise of output voltage during startup, which allows the prevention of output voltage overshoot. The soft start time of the output voltage can be specified by connecting a capacitor to the SS pin. See [page 17](#) for how to calculate the capacitance. A built-in soft start function is provided and a soft start is initiated in 1 ms(Typ) when the SS pin is open.
8. Error Amplifier
The Error Amplifier block is an error amplifier and its inputs are the reference voltage and the VOUT pin voltage.
9. PWM Comparator
The PWM Comparator block compares the output voltage of the Error Amplifier and the Slope signal to determine the output switching pulse duty.
10. OSC (Oscillator)
This block generates the oscillating frequency.
11. Driver Logic
This block controls switching operation and various protection functions.
12. Power Good
When the VOUT pin voltage reaches within ± 10 % (Typ) of the setting voltage, the built-in Nch MOSFET turns OFF and the PGD output turns high. In addition, the PGD output turns low when the VOUT pin voltage reaches outside ± 15 % (Typ) of the voltage setting.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	-0.3 to +7	V
EN Voltage	V_{EN}	-0.3 to V_{IN}	V
PGD Voltage	V_{PGD}	-0.3 to +7	V
VOUT, SS Voltage	V_{OUT}, V_{SS}	-0.3 to V_{IN}	V
Maximum Junction Temperature	T_{jmax}	150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
VSON008X2020				
Junction to Ambient	θ_{JA}	309.5	77.1	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	53	12	°C/W

(Note 1) Based on JESD51-2A(Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μ m

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ 0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μ m	74.2 mm x 74.2 mm	35 μ m	74.2 mm x 74.2 mm	70 μ m

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	2.7	5.5	V
Operating Temperature	T_a	-40	+125	°C
Output Current	I_{OUT}	-	600	mA

Electrical Characteristics (Unless otherwise specified Ta = Tj = -40 °C to +125 °C, V_{IN} = 5 V, V_{EN} = 5 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VIN						
Shutdown Circuit Current	I _{SDN}	-	0	10	μA	V _{EN} = 0 V, Ta = 25 °C
Circuit Current	I _{CC}	250	400	550	μA	I _{OUT} = 0 mA Non-switching, Ta = 25 °C
UVLO Detection Voltage	V _{UVLO1}	2.30	2.45	2.60	V	V _{IN} Falling
UVLO Release Voltage	V _{UVLO2}	2.40	2.55	2.70	V	V _{IN} Rising
UVLO Hysteresis Voltage	V _{UVLO-HYS}	50	100	125	mV	
ENABLE						
EN Threshold Voltage High	V _{ENH}	1.0	-	V _{IN}	V	
EN Threshold Voltage Low	V _{ENL}	GND	-	0.4	V	
EN Input Current	I _{EN}	2	5	8	μA	V _{EN} = 5.0 V, Ta = 25 °C
Output Voltage						
Output Voltage	V _{OUT}	1.0835	1.1000	1.1165	V	V _{IN} = 2.7 V to 5.5 V
V _{OUT} Input Current 1	I _{OUT1}	8.0	12.5	20	μA	V _{OUT} = 1.1 V
V _{OUT} Input Current 2	I _{OUT2}	9.0	12.5	16	μA	V _{OUT} = 1.1 V, Ta = 25 °C
Soft Start						
Soft Start Time	t _{SS}	0.5	1.0	2.0	ms	V _{IN} = 5.0 V, The SS Pin OPEN
		0.6	1.2	2.4	ms	V _{IN} = 3.3 V, The SS Pin OPEN
SS Charge Current	I _{SS}	-1.4	-1.0	-0.6	μA	
Switching Frequency						
Switching Frequency	f _{SW}	2.0	2.2	2.4	MHz	
Power Good						
PGD Falling (Fault) Voltage	V _{PGDTH_FF}	V _{OUT} x 0.80	V _{OUT} x 0.85	V _{OUT} x 0.90	V	V _{OUT} Falling
PGD Rising (Good) Voltage	V _{PGDTH_RG}	V _{OUT} x 0.85	V _{OUT} x 0.90	V _{OUT} x 0.95	V	V _{OUT} Rising
PGD Rising (Fault) Voltage	V _{PGDTH_RF}	V _{OUT} x 1.10	V _{OUT} x 1.15	V _{OUT} x 1.20	V	V _{OUT} Rising
PGD Falling (Good) Voltage	V _{PGDTH_FG}	V _{OUT} x 1.05	V _{FB} x 1.10	V _{OUT} x 1.15	V	V _{OUT} Falling
PGD Output Leakage Current	I _{LEAKPGD}	-	0	2	μA	V _{PGD} = 5.0 V, Ta = 25 °C
PGD FET ON Resistance	R _{PGD}	30	60	120	Ω	
PGD Output Low Level Voltage	V _{PGDL}	0.03	0.06	0.12	V	I _{PGD} = 1 mA
Switch MOSFET						
High Side FET ON Resistance	R _{ONH}	120	270	470	mΩ	V _{IN} = 5.0 V
		150	330	550	mΩ	V _{IN} = 3.3 V
Low Side FET ON Resistance	R _{ONL}	80	180	300	mΩ	V _{IN} = 5.0 V
		100	210	350	mΩ	V _{IN} = 3.3 V
High Side FET Leakage Current	I _{LEAKSWH}	-	0	5	μA	V _{IN} = 5.5 V, V _{SW} = 0 V, Ta = 25 °C
Low Side FET Leakage Current	I _{LEAKSWL}	-	0	5	μA	V _{IN} = 5.5 V, V _{SW} = 5.5 V, Ta = 25 °C
SW Current of Over Current Protection ^(Note 1)	I _{OCP}	0.8	1.2	1.6	A	
SW Discharge Resistance	R _{DIS}	450	650	850	Ω	
SCP, OVP						
Short Circuit Protection Detection Voltage	V _{SCP}	V _{OUT} x 0.6	V _{OUT} x 0.7	V _{OUT} x 0.8	V	
Output Over Voltage Protection Detection Voltage	V _{OVP}	V _{OUT} x 1.10	V _{OUT} x 1.15	V _{OUT} x 1.20	V	

(Note 1) This is design value. Not production tested.

Typical Performance Curves

Unless otherwise specified $V_{IN} = V_{EN}$

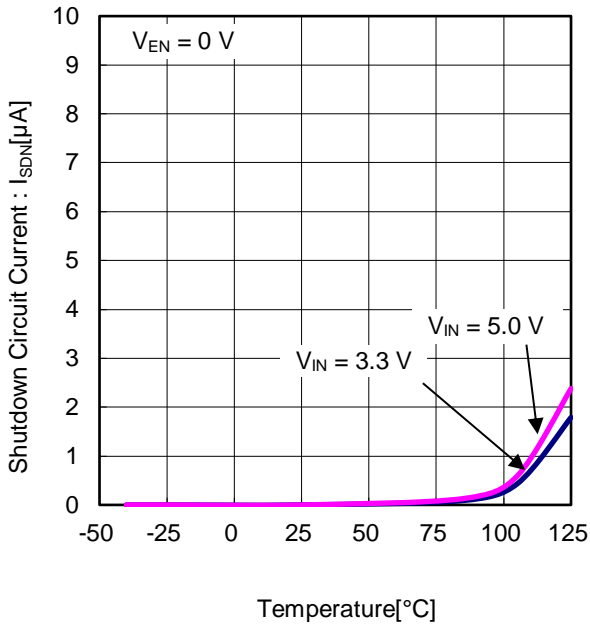


Figure 3. Shutdown Circuit Current vs Temperature

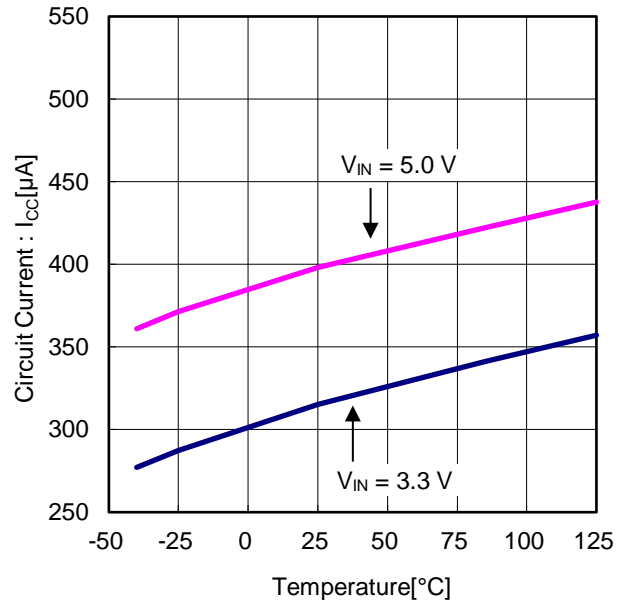


Figure 4. Circuit Current vs Temperature

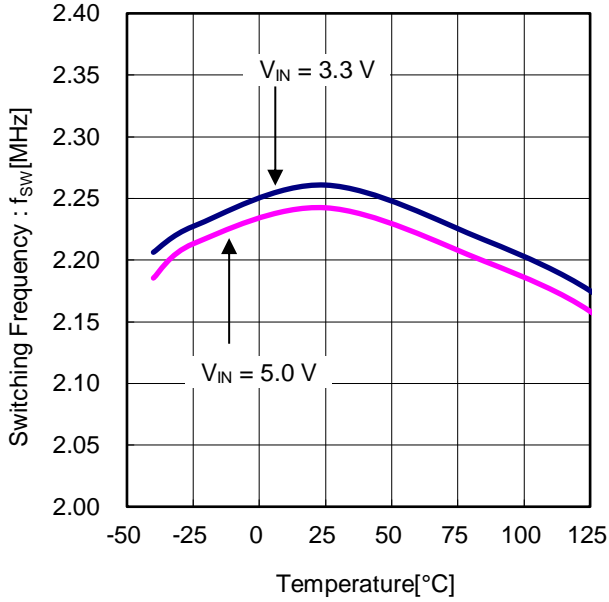


Figure 5. Switching Frequency vs Temperature

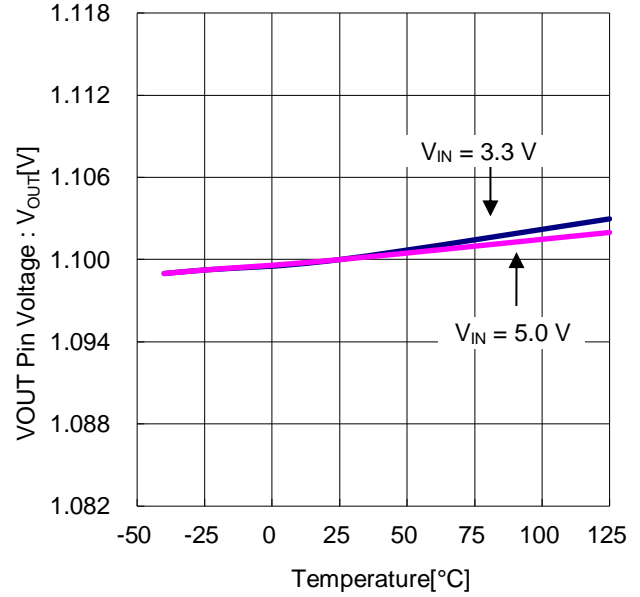


Figure 6. V_OUT Pin Voltage vs Temperature

Typical Performance Curves – continued

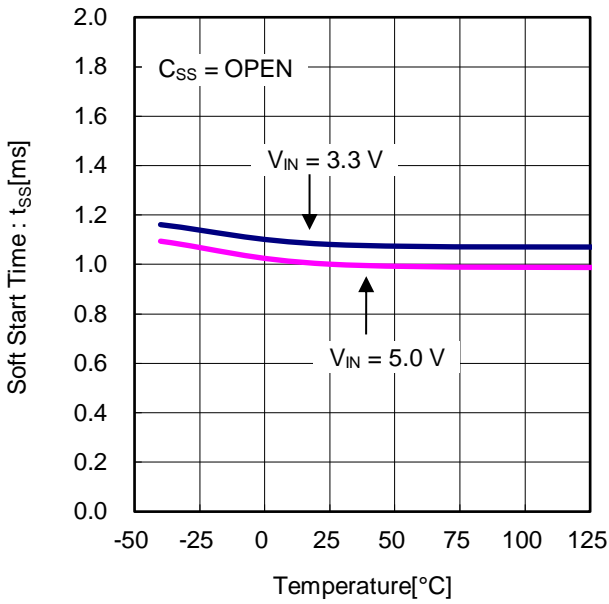


Figure 7. Soft Start Time vs Temperature

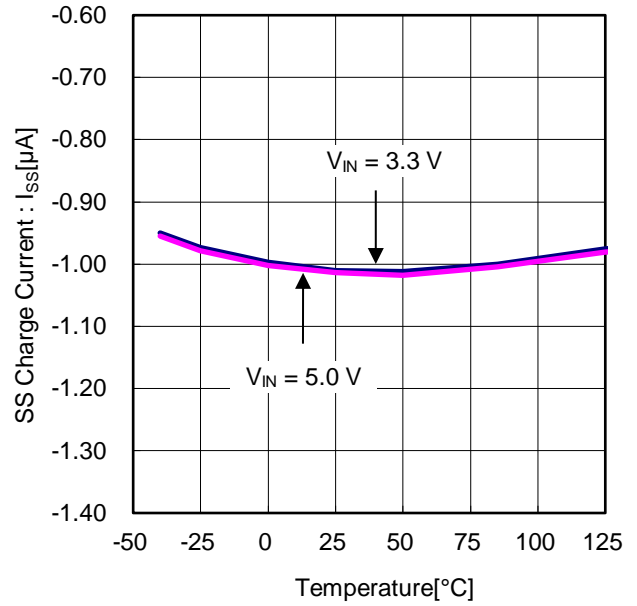


Figure 8. SS Charge Current vs Temperature

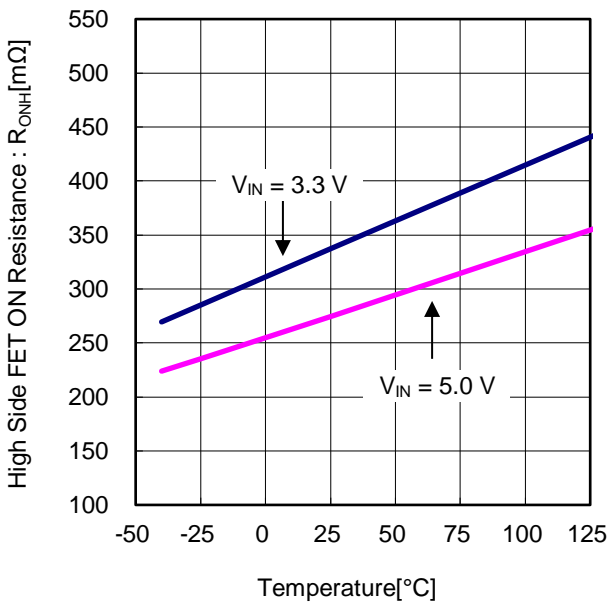


Figure 9. High Side FET ON Resistance vs Temperature

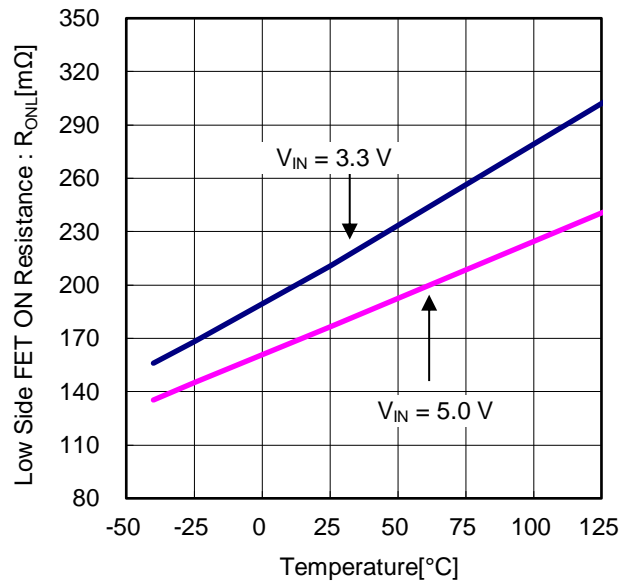


Figure 10. Low Side FET ON Resistance vs Temperature

Typical Performance Curves – continued

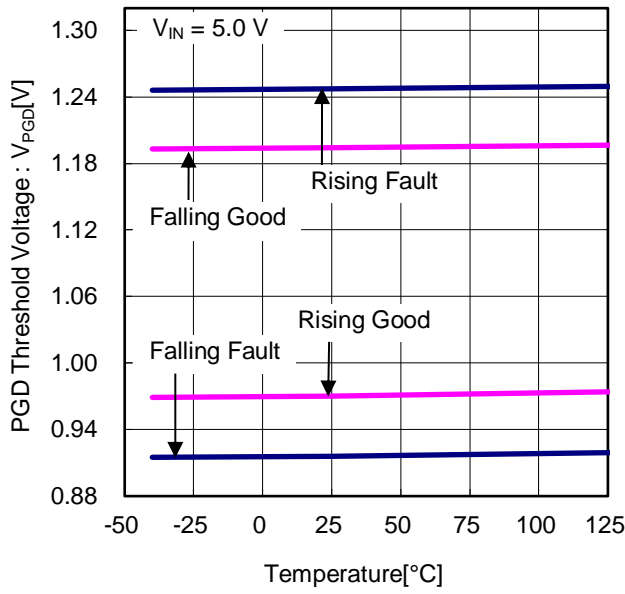


Figure 11. PGD Threshold Voltage vs Temperature

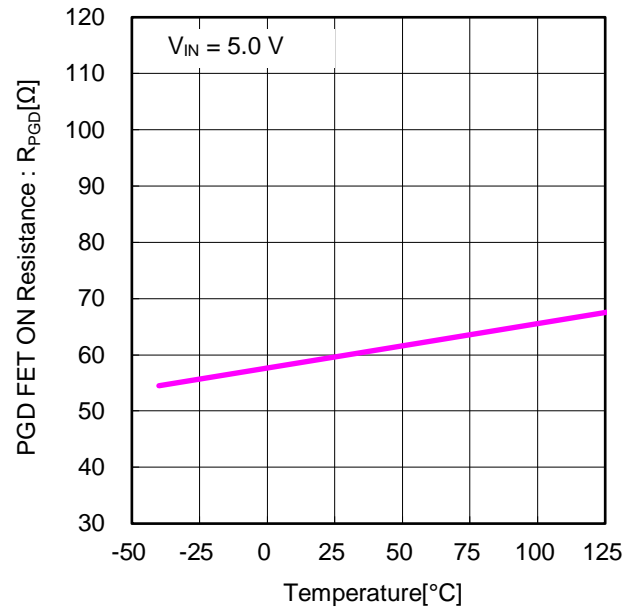


Figure 12. PGD FET ON Resistance vs Temperature

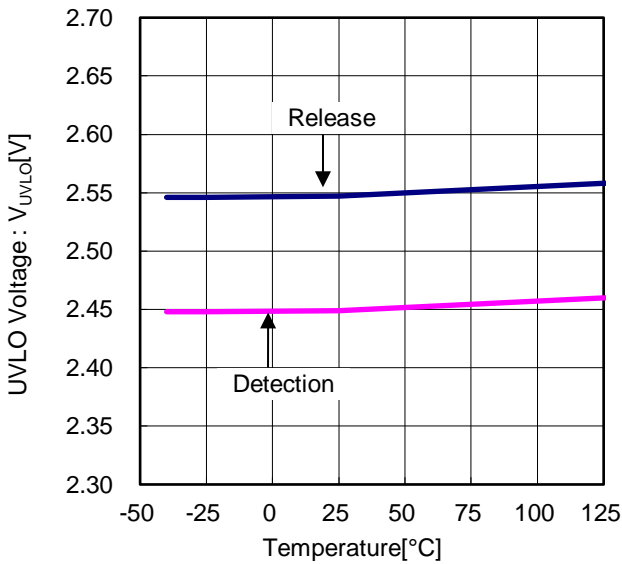


Figure 13. UVLO Voltage vs Temperature

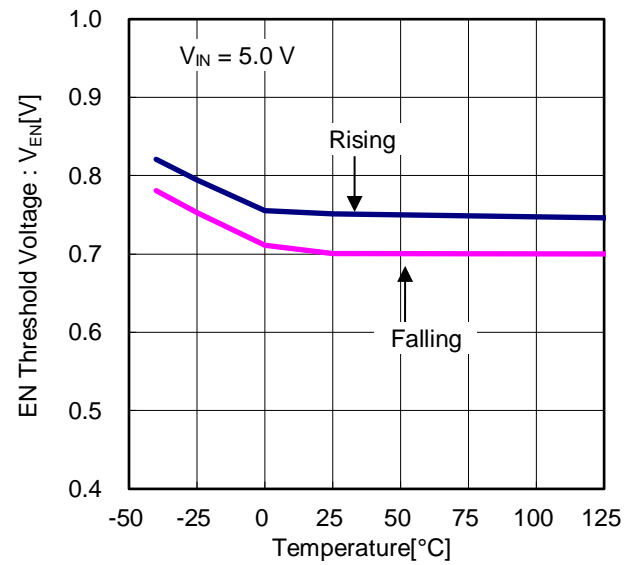


Figure 14. EN Threshold Voltage vs Temperature

Typical Performance Curves – continued

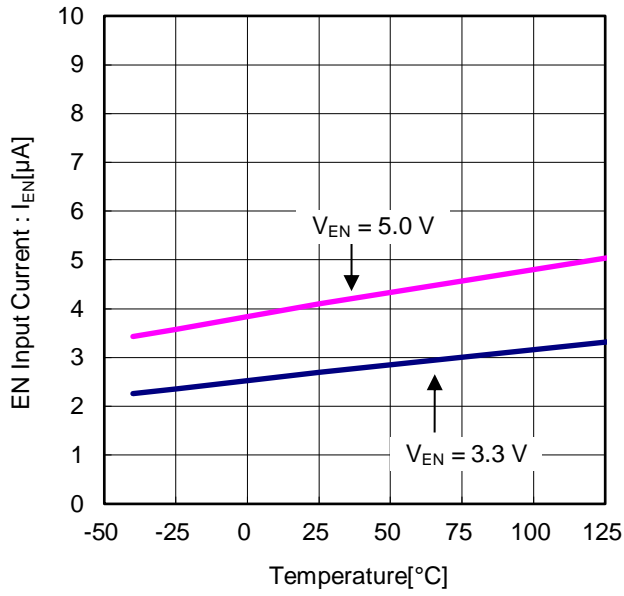


Figure 15. EN Input Current vs Temperature

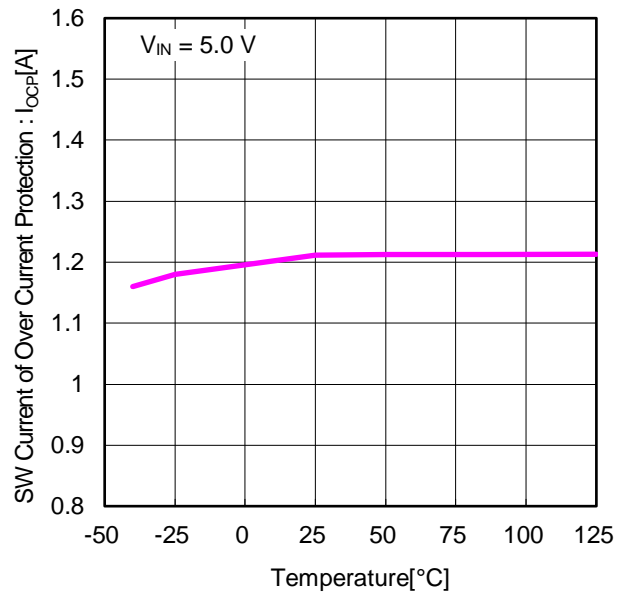


Figure 16. SW Current of Over Current Protection vs Temperature

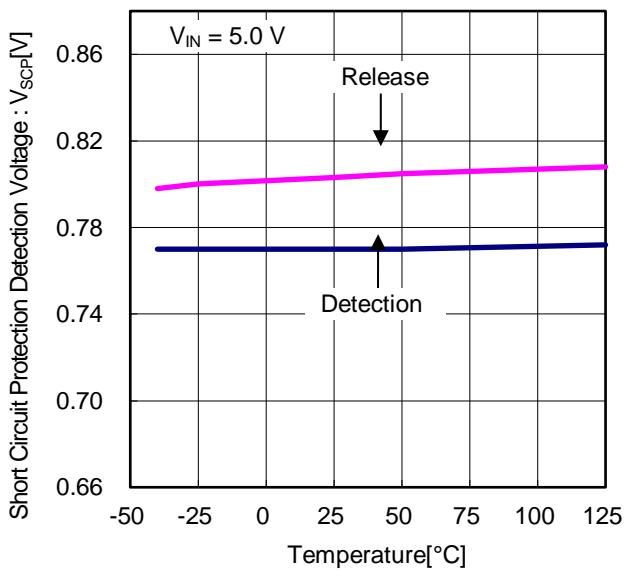


Figure 17. Short Circuit Protection Detection Voltage

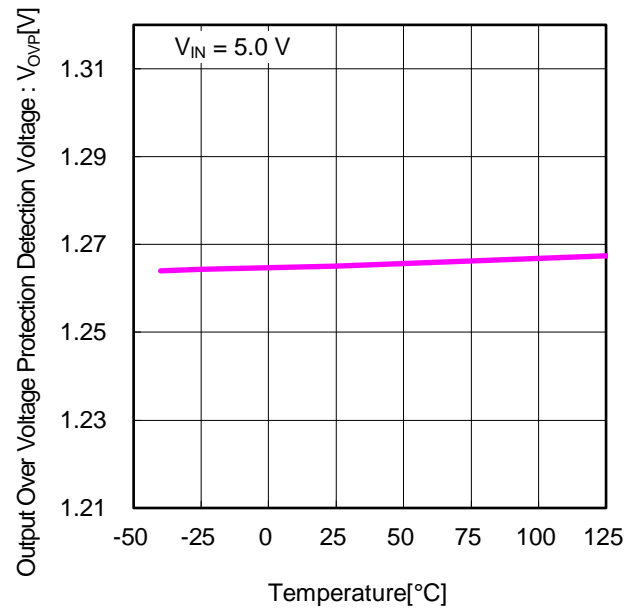


Figure 18. Output Over Voltage Protection Detection Voltage vs Temperature

Function Explanations

1. Enable Control

The device shutdown can be controlled by the voltage applied to the EN pin. When V_{EN} becomes 1.0 V or more, the internal circuit is activated and the device starts up with soft start. When V_{EN} becomes 0.4 V or less, the device will be shutdown.

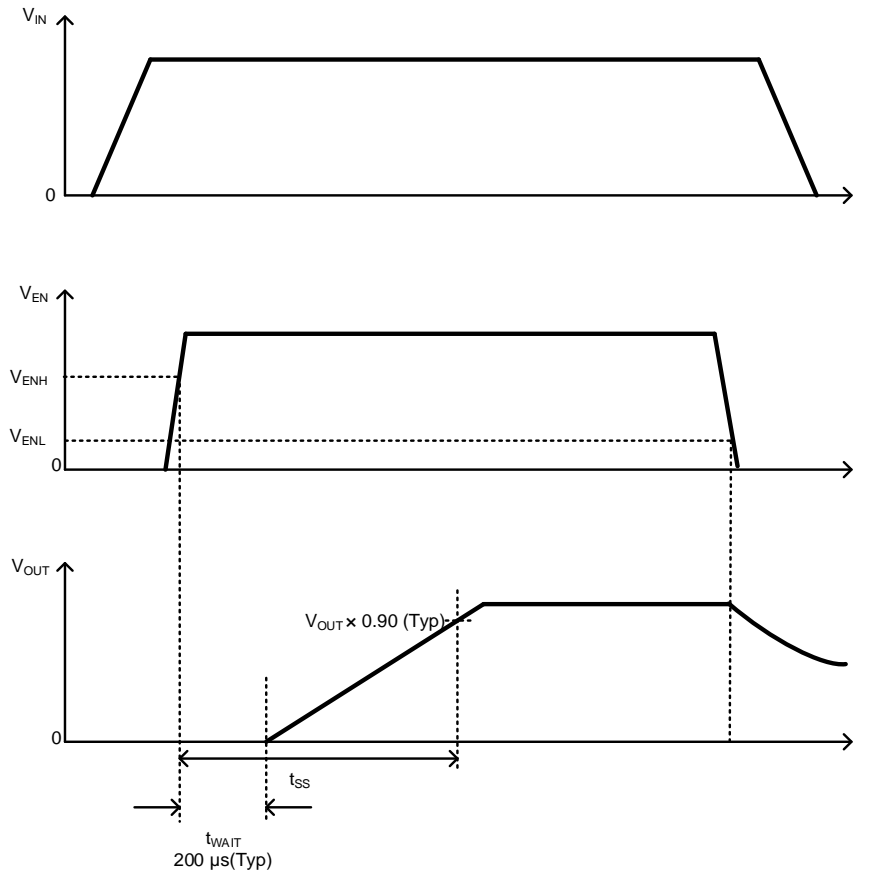


Figure 19. Enable ON/OFF Timing Chart

2. Power Good Function

When the VOUT pin voltage reaches within $\pm 10\%$ (Typ) of the voltage setting, the PGD pin open drain MOSFET turns OFF and the output turns high. In addition, when the VOUT pin voltage reaches outside $\pm 15\%$ (Typ) of the voltage setting, the PGD pin open drain MOSFET turns ON and the PGD pin is pulled down with impedance of $60\ \Omega$ (Typ). It is recommended to use a pull-up resistor of $2\ \text{k}\Omega$ to $100\ \text{k}\Omega$ for the power source

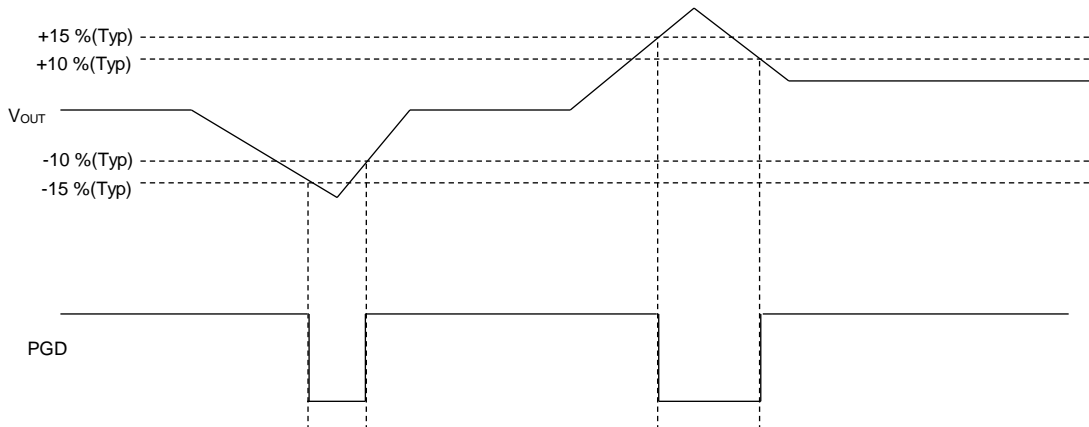


Figure 20. Power Good Timing Chart

Function Explanations – continued

3. Output Discharge Function

When even one of the following conditions is satisfied, output is discharged with $650\ \Omega$ (Typ) resistance through the SW pin.

- V_{EN} becomes $0.4\ \text{V}$ or less
- V_{IN} becomes $2.45\ \text{V(Typ)}$ or less(UVLO)
- V_{OUT} becomes $70\ \%$ (Typ) of the voltage setting or less and remains there for $1\ \text{ms(Typ)}$ (SCP)
- V_{OUT} becomes $+15\ \%$ (Typ) of the voltage setting or more(OVP)
- T_j becomes $175\ ^\circ\text{C(Typ)}$ or more(TSD)

When all of the above conditions are released, output discharge is stopped.

4. Pre-bias Function

The device can start up without to sink large current from the output even when the output is pre-biased. For example, if the device is turned ON/OFF by the EN pin, the output is discharged with the resistor of $650\ \Omega$ (Typ) during the EN OFF section and the delay section of $200\ \mu\text{s(Typ)}$, but both Output MOSFETs are turned off. After that, when the internal SS voltage reaches $40\ \text{mV(Typ)}$ higher than the internal FB voltage, the device starts switching and the output rises to the set voltage with soft start.

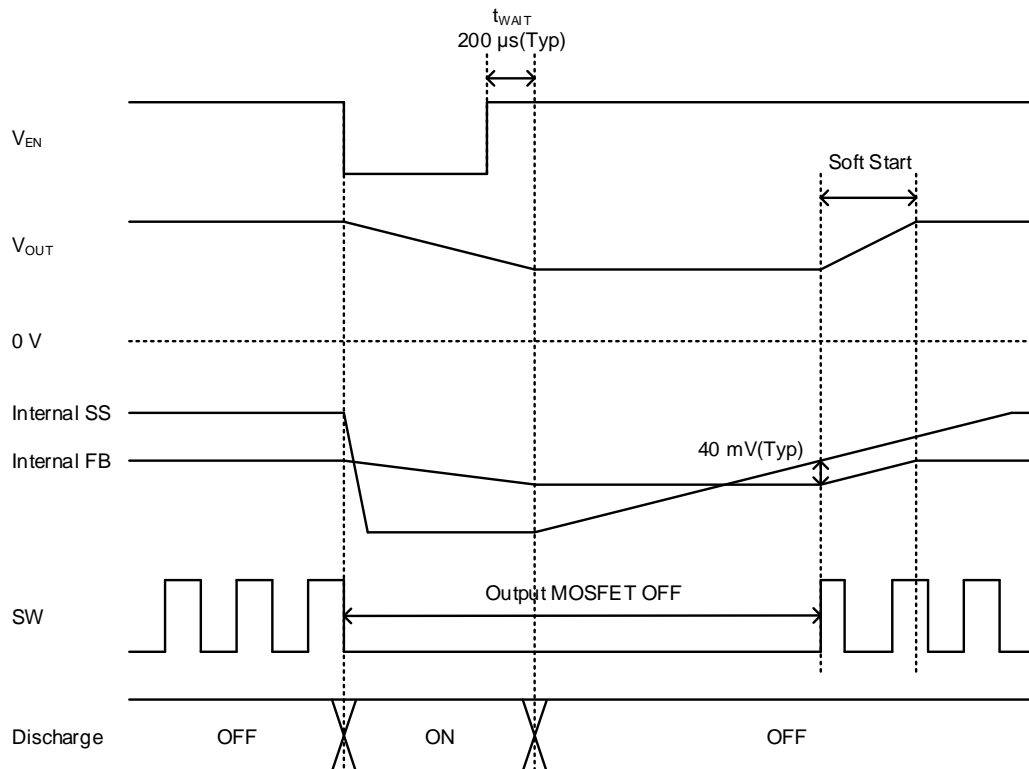


Figure 21. Pre-bias Timing Chart

Protection

1. Short Circuit Protection (SCP)

The Short Circuit Protection block compares the VOUT pin voltage with the internal reference voltage VREF. When the VOUT pin voltage has fallen to 70 % (Typ) of the voltage setting or less and remained there for 1 ms (Typ), SCP stops the operation for 14 ms (Typ) and subsequently initiates a restart. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the device should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected at all times).

The EN Pin	The VOUT Pin	Short Circuit Protection	Short Circuit Protection Operation
1.0 V or higher	$\leq V_{OUT} \times 0.7(\text{Typ})$	Enabled	ON
	$\geq V_{OUT} \times 0.75(\text{Typ})$		OFF
0.4 V or lower	-	Disabled	OFF

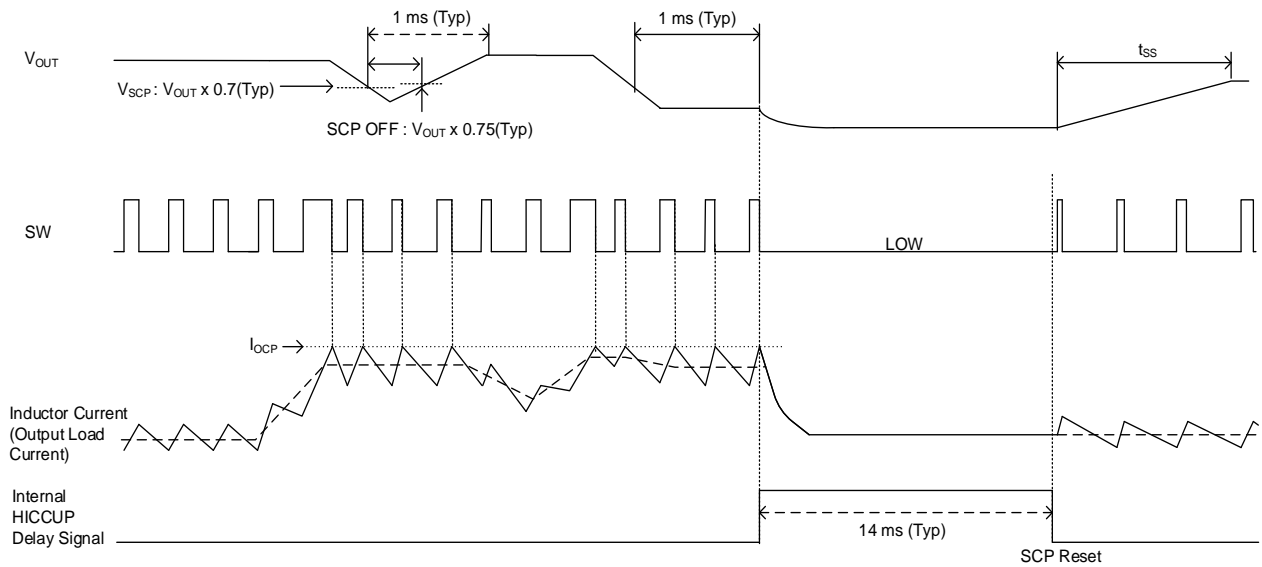


Figure 22. Short Circuit Protection (SCP) Timing Chart

2. Over Current Protection (OCP)

The Over Current Protection function operates by limiting the current that flows through High Side FET at each cycle of the switching frequency. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the device should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected at all times).

Protection – continued

3. Under Voltage Lockout Protection (UVLO)

It shuts down the device when the VIN pin falls to 2.45 V(Typ) or lower. The threshold voltage has a hysteresis of 100 mV(Typ).

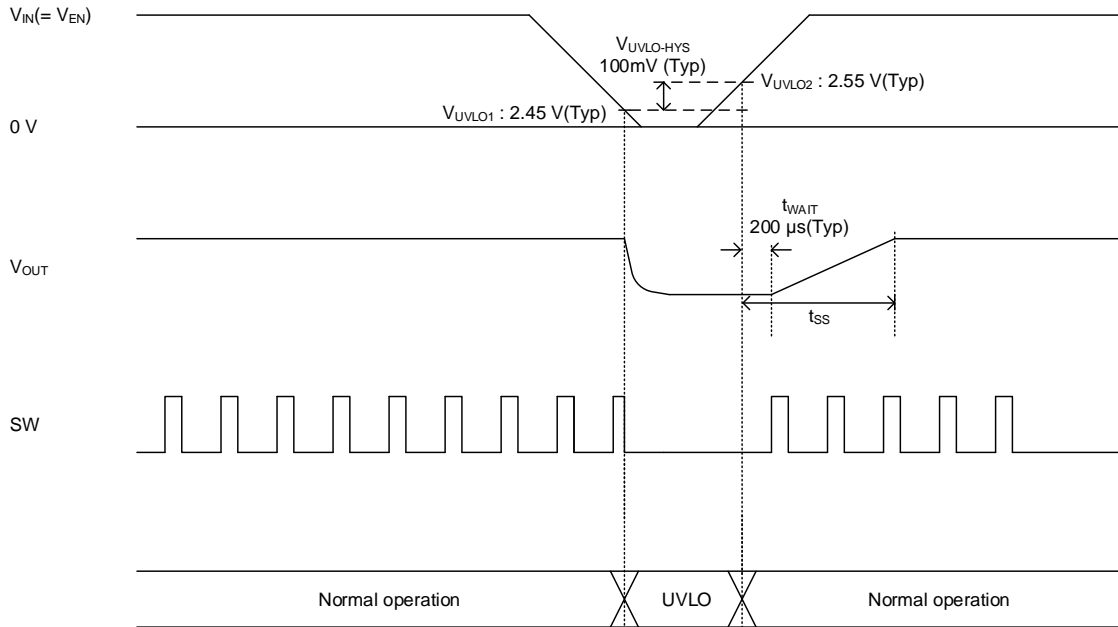


Figure 23. UVLO Timing Chart

4. Thermal Shutdown

This is the thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. However, if the rating is exceeded for a continued period and the junction temperature (T_j) rises to 175 °C(Typ), the TSD circuit activates and the output MOSFET turns OFF. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

5. Over Voltage Protection (OVP)

The device incorporates an over voltage protection circuit to minimize the output voltage overshoot when recovering from strong load transients or output fault conditions. If the VOUT pin voltage becomes over or equal to +15 % (Typ) of the voltage setting, which is Output Over Voltage Protection Detection Voltage, the MOSFET on the output stage is turned OFF to prevent the increase in the output voltage. After the detection, the switching operation resumes if the output decreases and the over voltage state is released. Output Over Voltage Protection Detection Voltage and release voltage have a hysteresis of 5 %.

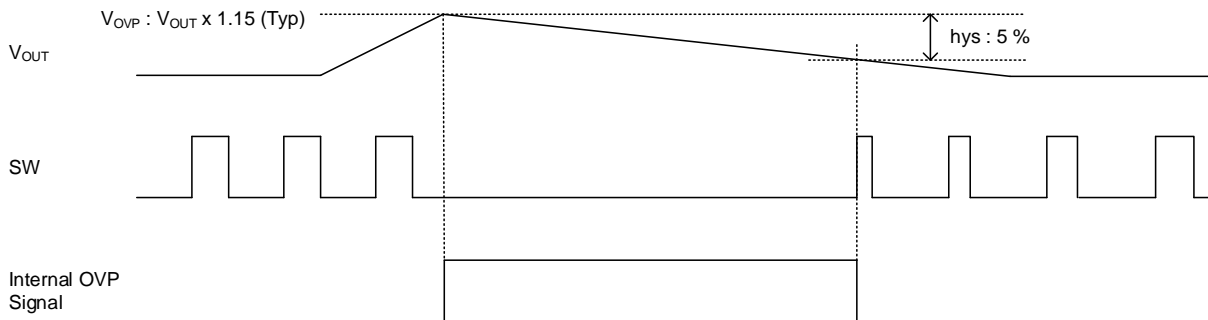


Figure 24. OVP Timing Chart

Selection of Components Externally Connected

Contact us if not use the recommended constant in this section.

Necessary parameters in designing the power supply are as follows:

Table 1. Application Specification

Parameter	Symbol	Example Value
Input Voltage	V_{IN}	5.0 V
Output Voltage	V_{OUT}	1.1 V(Typ)
Switching Frequency	f_{SW}	2.2 MHz(Typ)
Output Capacitor	C_{OUT}	10 μ F
Soft Start Time	t_{SS}	8.0 ms(Typ)
Maximum Output Current	I_{OUTMAX}	600 mA

Application Example

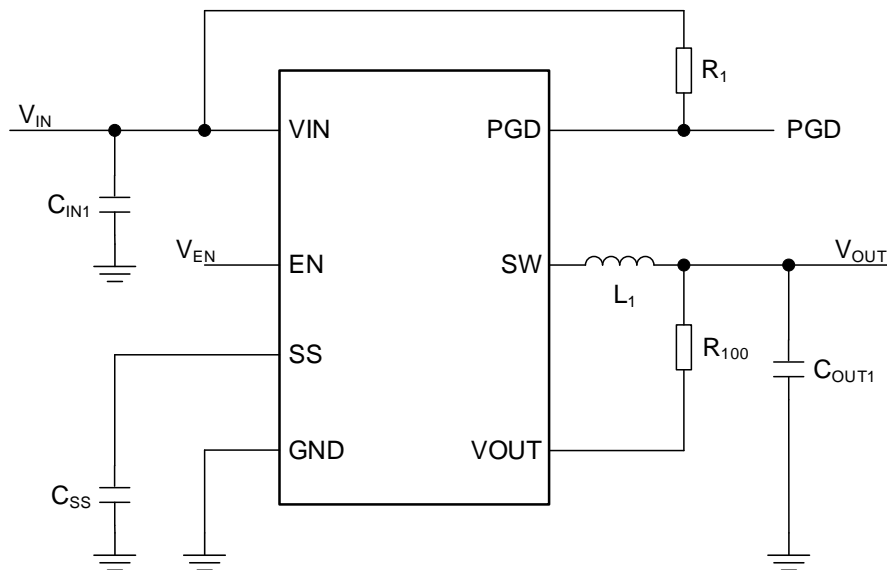


Figure 25. Typical Application

1. Switching Frequency

The switching frequency f_{SW} is fixed at 2.2 MHz(Typ) inside the IC.

2. Selection of Input Capacitor

Use ceramic type capacitor for the input capacitor C_{IN1} . C_{IN1} is used to suppress the input ripple noise and this capacitor is effective by being placed as close as possible to the VIN pin. Set the capacitor value for C_{IN1} so that it does not fall to 4.7 μ F considering the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, and etc. Use components which are comparatively same with the components used in [“Application Example” on page 18](#). Moreover, factors like the PCB layout and the position of the capacitor may lead to IC malfunction. Refer to [“PCB layout Design” on page 20 and 21](#).

In addition, the capacitor with value 0.1 μ F can be added to suppress the high frequency noise as an option.

Selection of Components Externally Connected – continued

3. Selection of Output LC Filter

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. Use the inductor with value 1.0 μH to 2.2 μH .

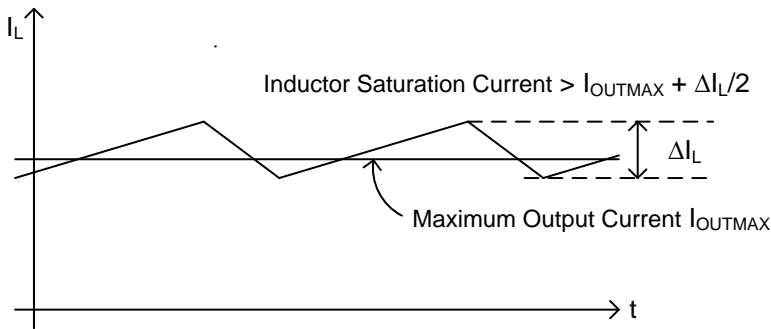


Figure 26. Waveform of Current through Inductor

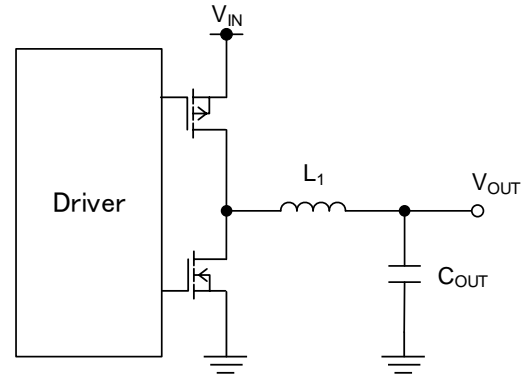


Figure 27. Output LC Filter Circuit

Inductor ripple current ΔI_L can be represented by the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L_1} = 260 \text{ [mA]}$$

where

- V_{IN} is the 5.0 V
- V_{OUT} is the 1.1 V
- L_1 is the 1.5 μH
- f_{SW} is the 2.2 MHz (Switching Frequency)

The rated current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔI_L .

Use ceramic type capacitor for the output capacitor C_{OUT} . The capacitance value of C_{OUT} is recommended in the range between 10 μF and 22 μF . C_{OUT} affects the output ripple voltage characteristics. C_{OUT} must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \text{ [V]}$$

Where

- R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor

The output ripple voltage ΔV_{RPL} can be represented by the following equation.

$$\Delta V_{RPL} = 0.260 \text{ A} \times \left(10 \text{ m}\Omega + \frac{1}{8 \times 10 \mu\text{F} \times 2.2 \text{ MHz}} \right) = 4.08 \text{ [mV]}$$

where

- C_{OUT} is the 10 μF
- R_{ESR} is the 10 m Ω

3. Selection of Output LC Filter – continued

In addition, for the total value of capacitance in the output line $C_{OUT(Max)}$, need to satisfy the value obtained by the following equation.

$$C_{OUT(Max)} < \frac{(t_{SS(Min)} - 200 \mu s) \times (I_{OCP(Min)} - I_{SWSTART})}{V_{OUT}} \text{ [F]}$$

where:

- $I_{SWSTART}$ is the maximum output current during startup
- $I_{OCP(Min)}$ is the minimum OCP operation SW current 0.8 A
- $t_{SS(Min)}$ is the minimum Soft Start Time
- V_{OUT} is the output voltage

Startup failure may happen if the limits from the above-mentioned are exceeded. Especially if the capacitance value is large, over current protection may be activated by the inrush current at startup and prevented to turn on the output. Please confirm this on the actual application.

Stable transient response and the loop is dependent to C_{OUT} . Actually, characteristics will vary depending on PCB layout, arrangement of wiring, kinds of parts used and use conditions(temperature, etc.). Please be sure to check stability and responsiveness with the actual application.

4. Selection of Soft Start Capacitor

Turning the EN pin signal high activates the soft start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time t_{SS_EXT} depends on the value of the capacitor connected to the SS pin. The capacitance value should be set in the range between 4700 pF and 0.1 μ F.

$$t_{SS_EXT} = \frac{(C_{SS} \times 0.8)}{I_{SS}} \text{ [s]}$$

$$t_{OFFSET} = \frac{(C_{SS} \times 0.04)}{I_{SS}} \text{ [s]}$$

where

- t_{SS_EXT} is the Soft Start Time
- t_{OFFSET} is the Internal Delay Time
- C_{SS} is the Capacitor connected to the SS pin
- I_{SS} is the SS Charge Current 1.0 μ A(Typ)

With $C_{SS} = 0.01 \mu$ F

$$t_{SS_EXT} = \frac{(0.01 \mu F \times 0.8)}{1.0 \mu A} = 8.0 \text{ [ms]}$$

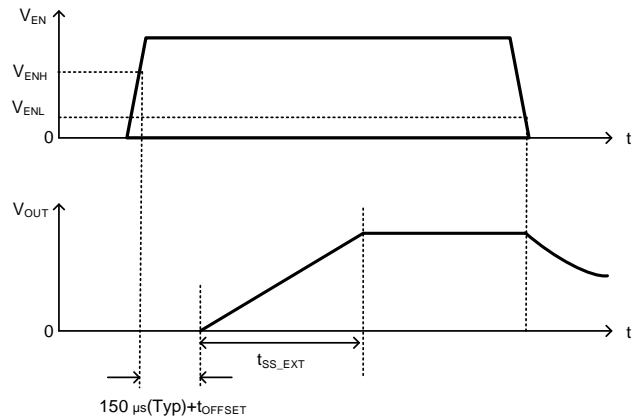


Figure 28. Soft Start Timing Chart

Turning the EN pin High without connecting capacitor to the SS pin and keeping the SS pin either OPEN condition or 10 k Ω to 100 k Ω pull up condition to power source, the output will rise in 1 ms(Typ).

Recommended Parts Manufacturer List

Shown below is the list of the recommended parts manufacturers for reference.

Table 2

Device	Type	Manufacturer	URL
C	Ceramic capacitors	Murata	www.murata.com
C	Ceramic capacitors	TDK	product.tdk.com
L	Inductors	Coilcraft	www.coilcraft.com
L	Inductors	Cyntec	www.cyntec.com
L	Inductors	Murata	www.murata.com
L	Inductors	Sumida	www.sumida.com
L	Inductors	TDK	product.tdk.com
R	Resistors	ROHM	www.rohm.com

Application Example

Table 3. Specification Example

Parameter	Symbol	Example Value
Product Name	IC	BD9S012NUX-C
Supply Voltage	V_{IN}	5.0 V, 3.3 V
Output Voltage	V_{OUT}	1.1 V(Typ)
Soft Start Time	t_{SS}	1.0 ms(Typ)
Maximum Output Current	I_{OUTMAX}	600 mA
Operation Temperature Range	T_a	-40 °C to +125 °C

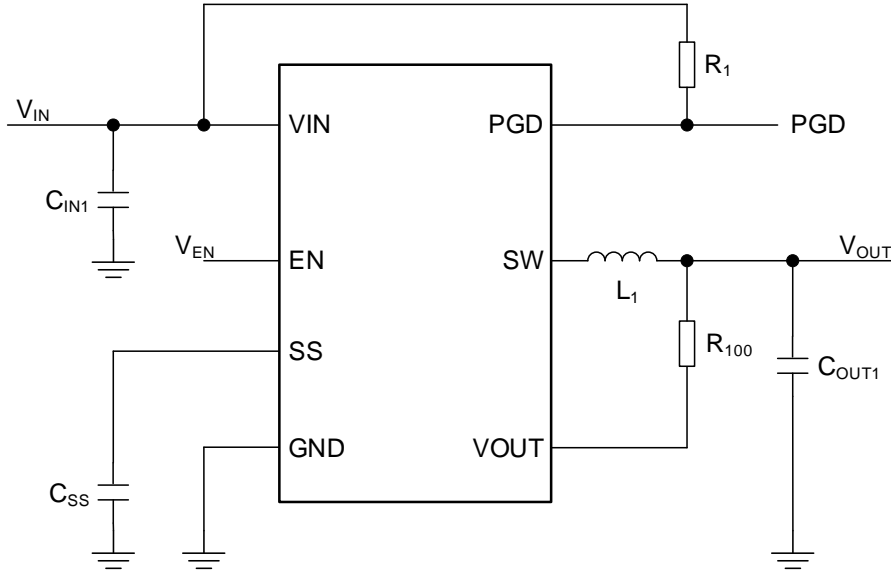


Figure 29. Reference Circuit

Table 4. Parts List

No	Package	Parameters	Part Name(Series)	Type	Manufacturer
L_1	2016	1.5 μ H	TFM201610ALMA1R5M	Inductor	TDK
C_{OUT1}	2012	10 μ F, X7R, 6.3 V	GCM21BR70J106K	Ceramic Capacitor	Murata
C_{IN1}	2012	10 μ F, X7R, 10 V	GCM21BR71A106K	Ceramic Capacitor	Murata
R_{100}	-	SHORT	-	-	-
R_1	1005	100 k Ω , 1 %, 1/16 W	MCR01MZPF1003	Chip Resistor	ROHM
C_{SS}	-	-	-	-	-

Characteristic Data (Application Examples)

$V_{IN} = V_{EN}$, $T_a = 25\text{ }^\circ\text{C}$

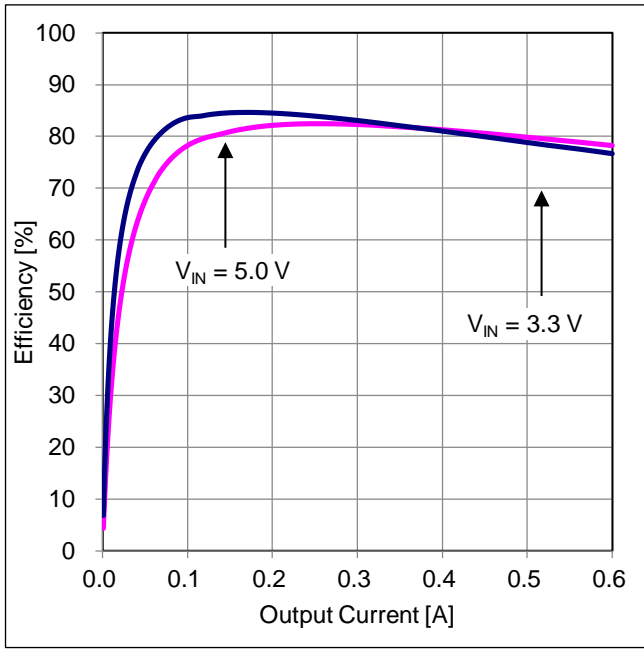


Figure 30. Efficiency vs Output Current

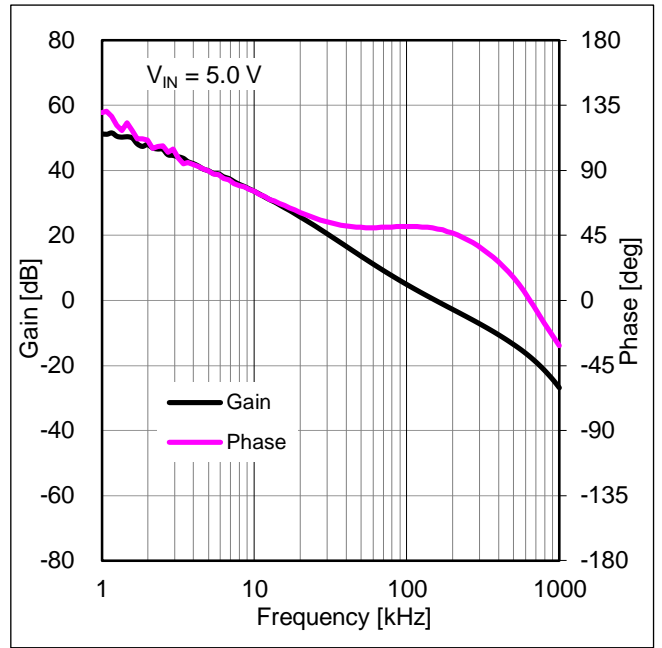


Figure 31. Frequency Characteristics ($I_{OUT} = 0.6\text{ A}$)

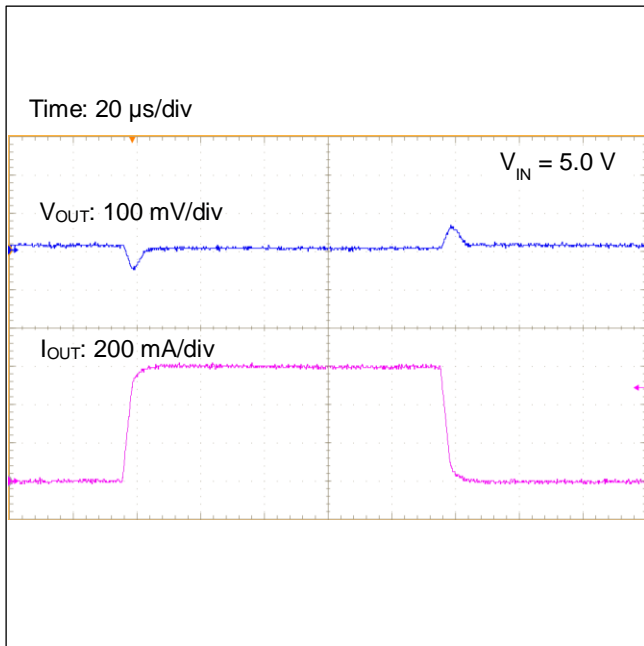


Figure 32. Load Transient Response ($I_{OUT} = 0\text{ A} \leftrightarrow 0.6\text{ A}$)

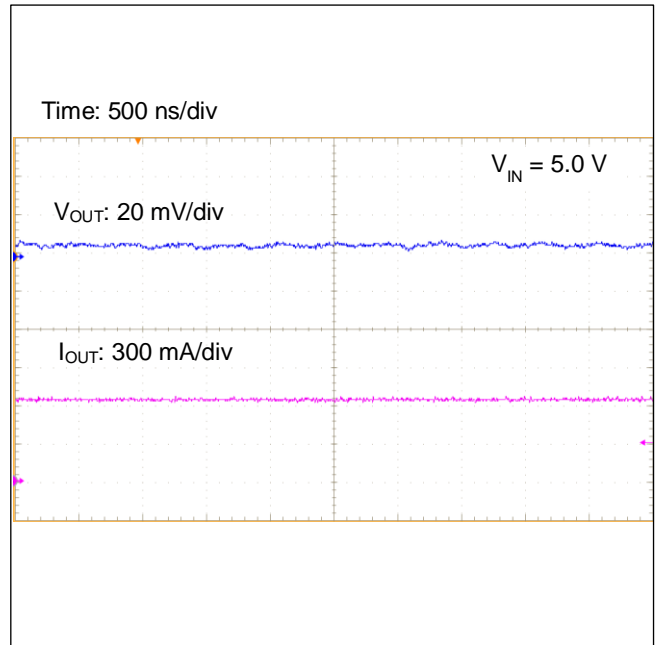


Figure 33. Output Ripple Voltage ($I_{OUT} = 0.6\text{ A}$)

PCB Layout Design

PCB layout design for DC/DC converter is very important. Appropriate layout can avoid various problems concerning power supply circuit. Figure 34-a to 34-c show the current path in a buck DC/DC converter circuit. The Loop 1 in Figure 34-a is a current path when H-side switch is ON and L-side switch is OFF, the Loop 2 in Figure 34-b is when H-side switch is OFF and L-side switch is ON. The thick line in Figure 34-c shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element H-side and L-side switch change from OFF to ON, and vice versa. These sharp changes induce a waveform with harmonics in this loop. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more details, refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

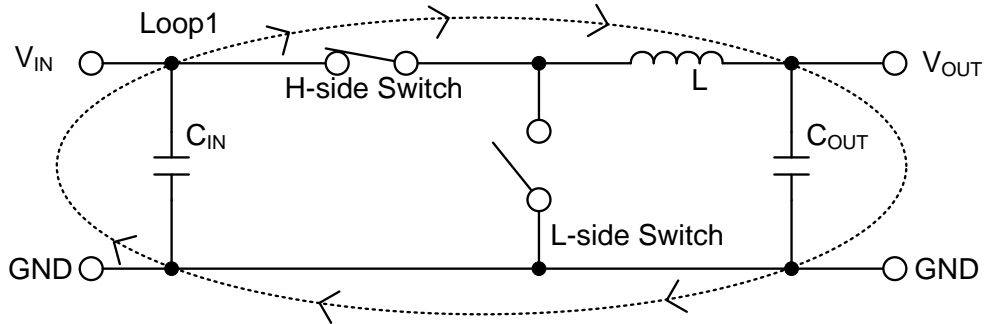


Figure 34-a. Current Path when H-side Switch = ON, L-side Switch = OFF

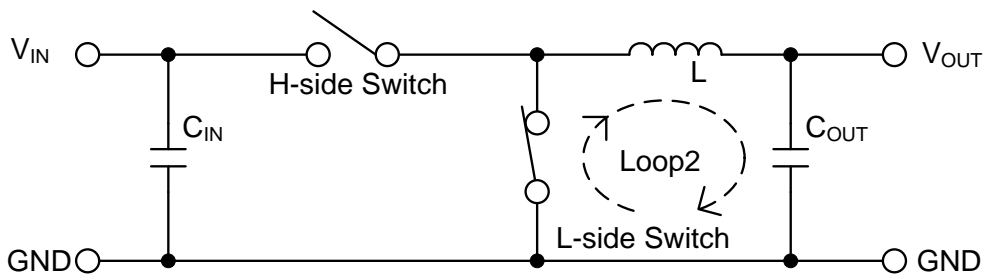


Figure 34-b. Current Path when H-side Switch = OFF, L-side Switch = ON

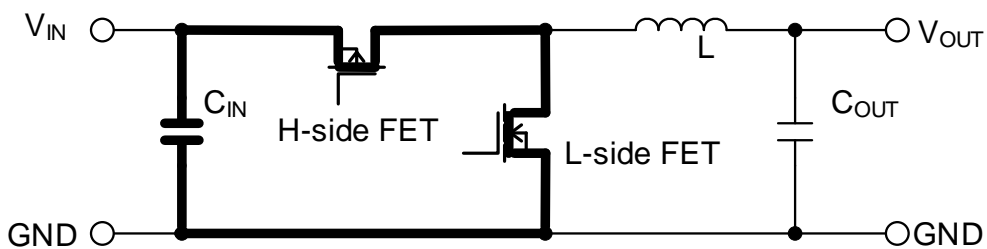
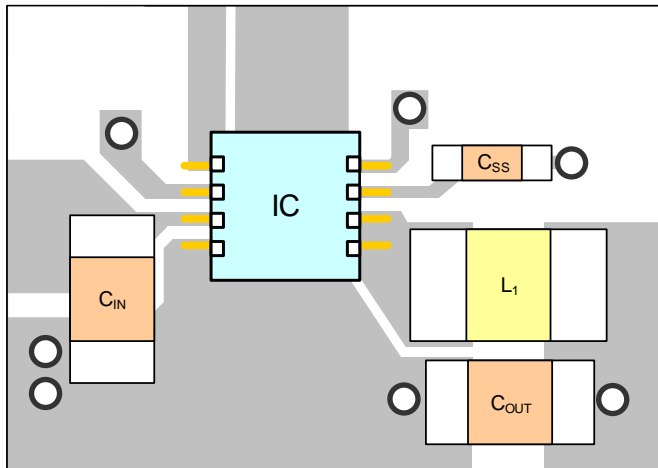


Figure 34-c. Difference of Current and Critical Area in Layout

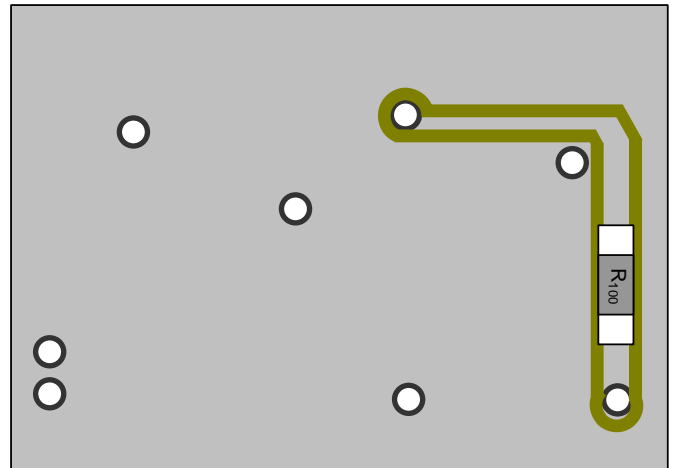
PCB Layout Design – continued

When designing the PCB layout, please pay extra attention to the following points:

- Connect the input capacitor C_{IN} as close as possible to the VIN pin and GND pin on the same plane as the IC.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the inductor pattern as thick and as short as possible.
- Feedback line connected to VOUT pin far from the SW nodes.
- R_{100} is provided for the measurement of feedback frequency characteristics (optional). By inserting a resistor into R_{100} , it is possible to measure the frequency characteristics of feedback (phase margin) using FRA etc. R_{100} is short-circuited for normal use.



Example of Evaluation Board Layout (Top View)



Example of Evaluation Board Layout (Bottom View)

Figure 35. Example of Evaluation Board Layout

Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
 (Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature T_a is to be 125 °C or less.
2. The chip junction temperature T_j is to be 150 °C or less.

The chip junction temperature T_j can be considered in the following two patterns:

1. To obtain T_j from the package surface center temperature T_t in actual use

$$T_j = T_t + \psi_{JT} \times W \text{ [}^\circ\text{C]}$$

2. To obtain T_j from the ambient temperature T_a

$$T_j = T_a + \theta_{JA} \times W \text{ [}^\circ\text{C]}$$

Where:

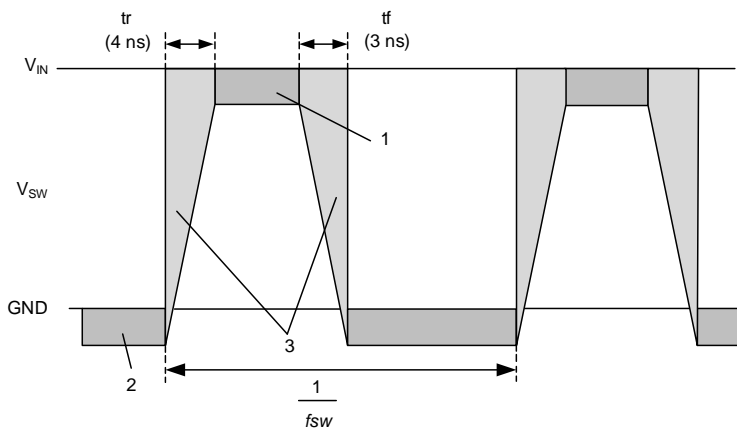
- ψ_{JT} is junction to top characterization parameter ([Refer to page 5](#))
- θ_{JA} is junction to ambient ([Refer to page 5](#))

The heat loss W of the IC can be obtained by the formula shown below:

$$W = R_{ONH} \times I_{OUT}^2 \times \frac{V_{OUT}}{V_{IN}} + R_{ONL} \times I_{OUT}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + V_{IN} \times I_{CC} + \frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW} \text{ [W]}$$

Where:

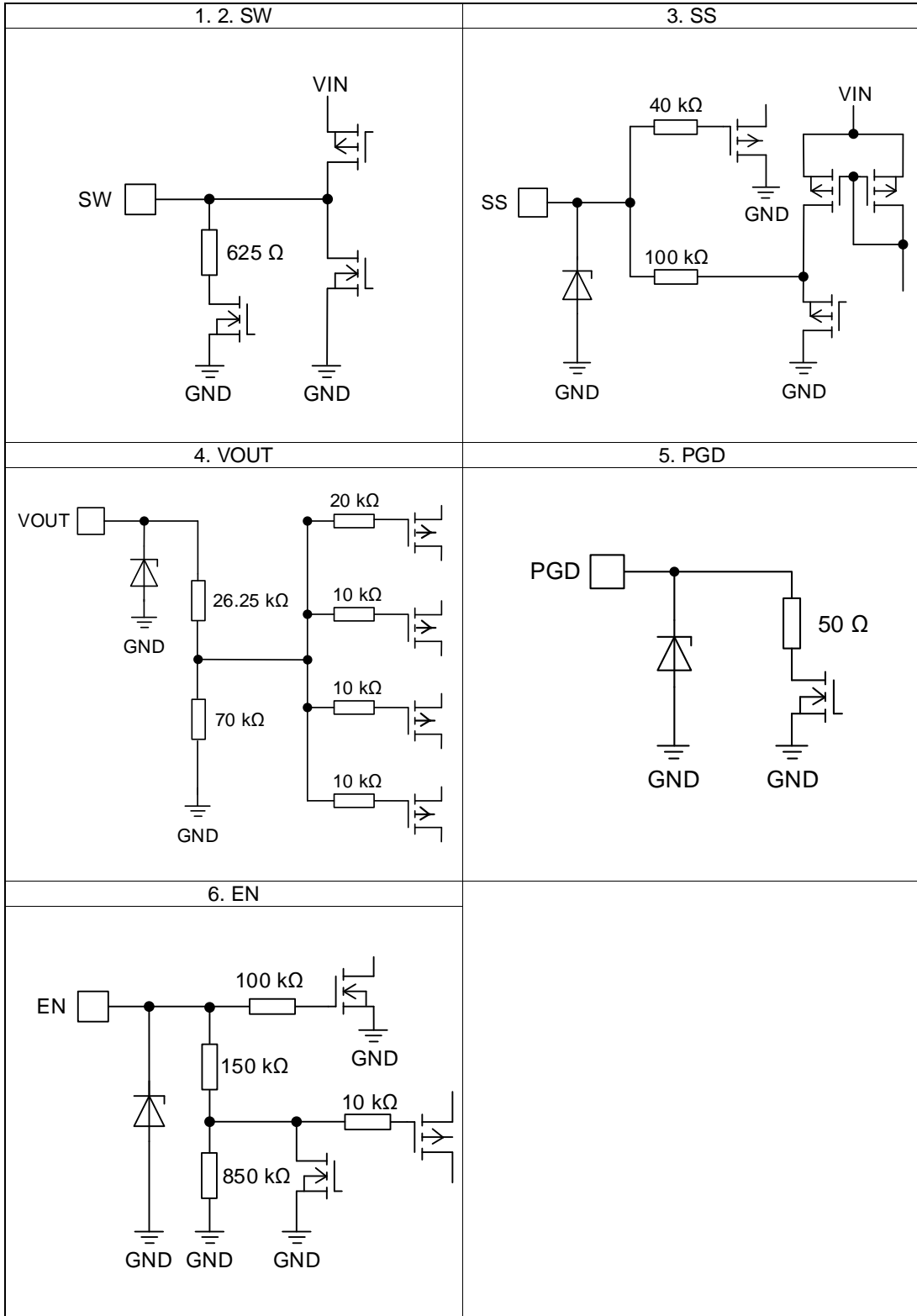
- R_{ONH} is the High Side FET ON Resistance ([Refer to page 6](#)) [Ω]
- R_{ONL} is the Low Side FET ON Resistance ([Refer to page 6](#)) [Ω]
- I_{OUT} is the Output Current [A]
- V_{OUT} is the Output Voltage [V]
- V_{IN} is the Input Voltage [V]
- I_{CC} is the Circuit Current ([Refer to page 6](#)) [A]
- tr is the Switching Rise Time [s] (Typ:4 ns)
- tf is the Switching Fall Time [s] (Typ:3 ns)
- f_{SW} is the Switching Frequency ([Refer to page 6](#)) [Hz]



1. $R_{ONH} \times I_{OUT}^2$
2. $R_{ONL} \times I_{OUT}^2$
3. $\frac{1}{2} \times (tr + tf) \times V_{IN} \times I_O \times f_{SW}$

Figure 36. SW Waveform

I/O Equivalence Circuits



(Note) Resistance value is Typical.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

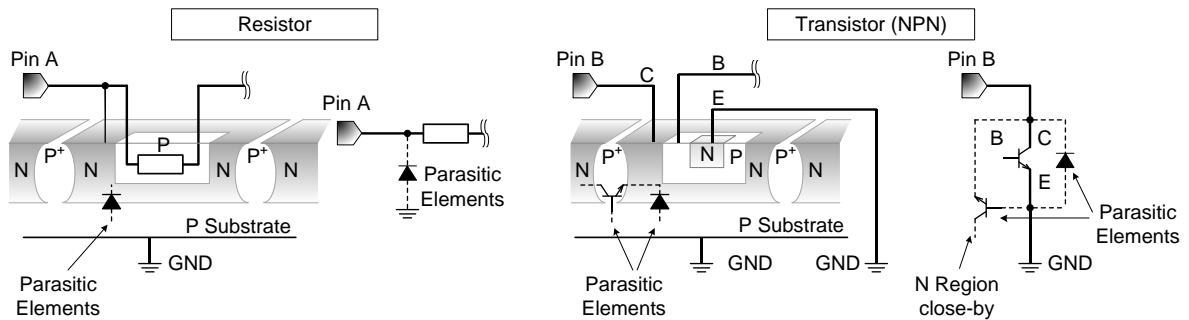


Figure 37. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

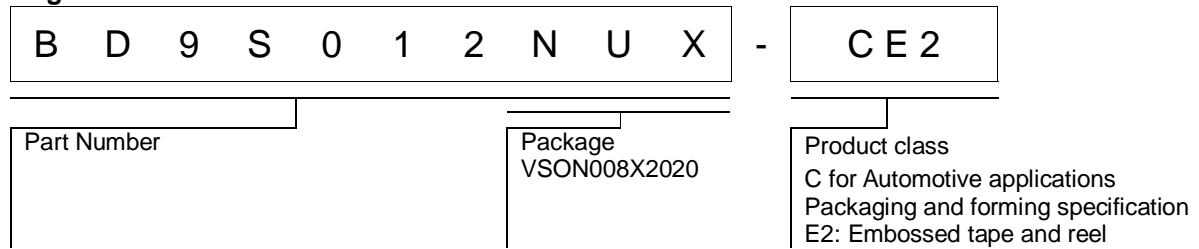
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

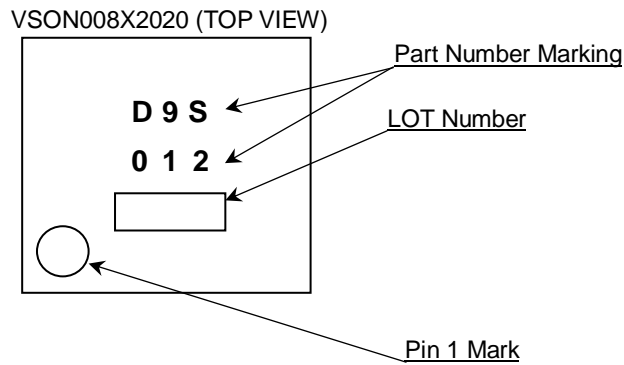
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

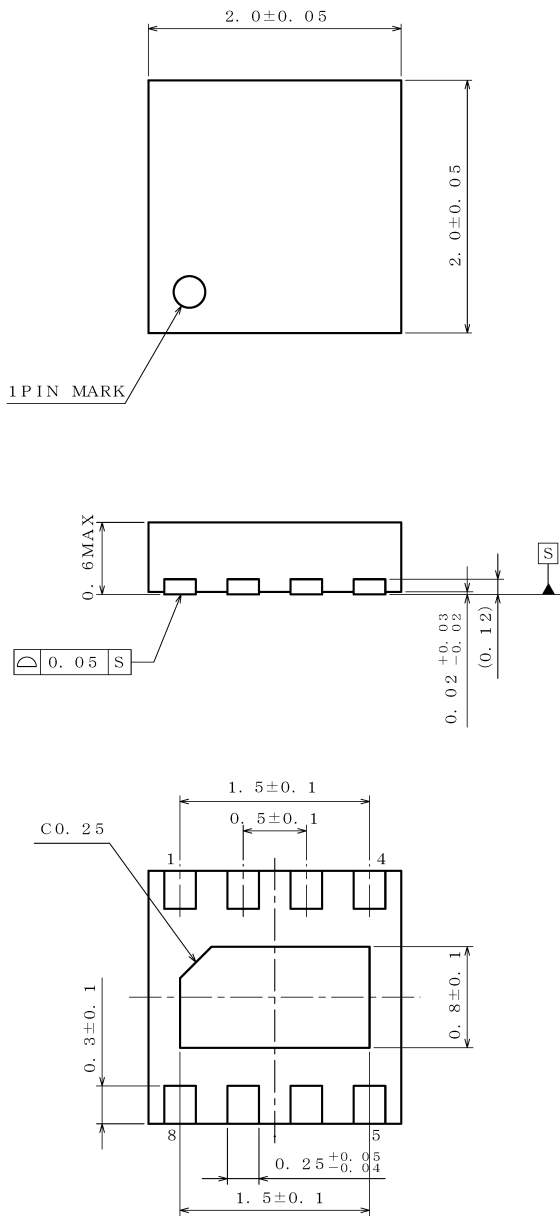


Marking Diagram



Physical Dimension and Packing Information

Package Name	VSON008X2020
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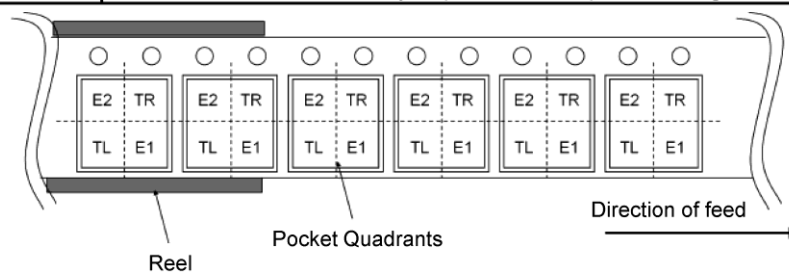


(UNIT : mm)

PKG : VSON008X2020
Drawing No. EX178-5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
21.Feb.2019	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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