Click here to ask an associate for production status of specific part numbers.

MAX17554, MAX17555

Integrated 60V, 50mA, Ultra-Small, High Efficiency, Synchronous Step-Down DC-DC Converters

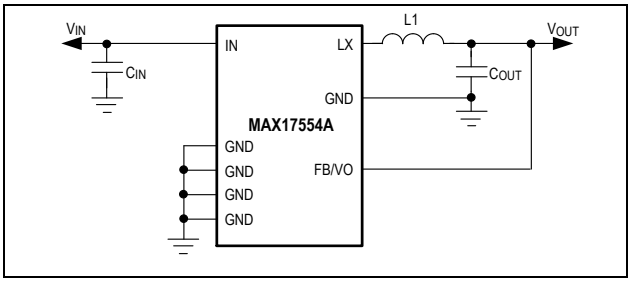
Product Highlights

- Reduces External Components and Total Cost
  - No Schottky–Synchronous Operation
  - Internal Control Loop Compensation
  - Internal Fixed Soft-Start
  - Fixed Turn ON/OFF Input Voltage (MAX17554)
  - All-Ceramic Capacitors, Ultra-Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4V to 60V Input Voltage (MAX17555)
  - Wide 10V to 60V Input Voltage (MAX17554)
  - Fixed 3.3V (MAX17554A, MAX17555A) and 5V (MAX17554B, MAX17555B) Output Voltage Options
  - Adjustable Output Range from 0.8V up to 90% of V_{IN} (MAX17554C, MAX17555C)
  - Deliver up to 50mA of Load Current
- Reduced Power Dissipation
  - Higher Light-Load Efficiency with Discontinuous-Conduction Mode (DCM) Operation
  - Power Loss Reduction with External Boot-Strap Input (FB/VO) for Internal Circuitry (Fixed Output Part Options)
  - Fixed 70kHz Switching Frequency
  - 3.8µA Shutdown Current (MAX17555)
- Flexible Design
  - Programmable EN/UV and HYST Threshold (MAX17555)
  - Open-Drain Output ($\overline{RESET}$) for Output Status Monitoring (MAX17555)
- Robust Operation
  - Built-in Hiccup Mode Overload Protection
  - Overtemperature Protection
  - CISPR32 Class B Compliant
  - Wide -40°C to +125°C Ambient Operating Temperature, -40°C to +150°C Junction Temperature

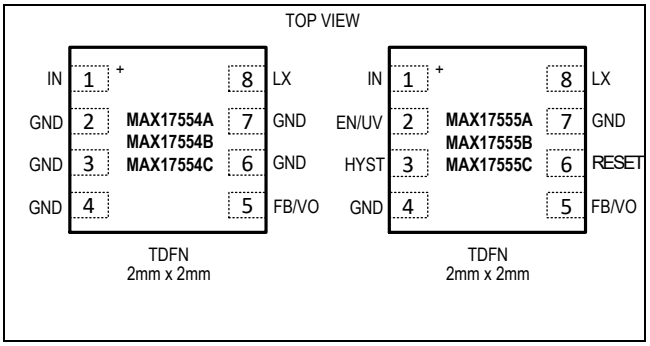
Key Applications

- Factory Automation
  Within the Factory Automation space, one key need is the ability to generate less heat. Heat within the system has to be managed to prevent overheating and shutdown. The MAX17554 and MAX17555 generate less heat since they are fully synchronous integrated FETs DC-DC converters with high efficiency.
- Aftermarket Market Automotive
  Asset tracking application is an example within the aftermarket automotive space where the MAX17554 and MAX17555 would provide a benefit. Typically, these units are designed to be as small as possible. The MAX17554 and MAX17555 have integrated FETs and internal loop compensation in delivering a small solution size.
- General Point of Load
  General point of load applies to a switching regulator that serves many applications and design environments. Robustness of the power conversion is critical to any environment. With an operating range of -40°C to +125 °C, current limit protection, overtemperature protection, and the ability to adhere to the CISPR32 class B emission standards, the MAX17554 and MAX17555 deliver a small, highly efficient power conversion in the most adverse environments.

Simplified Application Diagram



Pin Description



***Ordering Information* appears at end of data sheet.**

19-101535; Rev 1; 5/22

Absolute Maximum Ratings

IN to GND ..... -0.3V to +70V

LX to GND ..... -0.3V to V_{IN} + 0.3V

EN/UV to GND (MAX17555) ..... -0.3V to V_{IN} + 0.3V

HYST, $\overline{RESET}$ to GND (MAX17555) ..... -0.3V to +6V

FB/VO to GND (MAX17554A, MAX17554B, MAX17555A, MAX17555B) ..... -5.5V to +6V

FB/VO to GND (MAX17554C, MAX17555C) ..... -0.3V to +6V

Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70°C, 8-Pin TDFN, derate 6.2mW/°C above +70°C) 496mW

Operating Temperature Range (*Note 1*) ..... -40°C to +125°C

Junction Temperature ..... -40°C to +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C

Note 1: Junction temperatures greater than +125°C degrade operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 TDFN	
Package Code	T822CN+1
Outline Number	*21-0487*
Land Pattern Number	*90-0349*
Thermal Resistance, Four Layer Board	
Junction-to-Ambient (θ_{JA})	162°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	20°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 24V, $V_{EN/UV}$ = 24V (MAX17555), V_{GND} = 0V, C_{IN} = 1µF, $V_{FB/VO}$ = 1.05 × V_{FB-REG}, LX = Unconnected, HYST = $\overline{RESET}$ = Unconnected (MAX17555), T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted. (*Note 2*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)							
Input Voltage Range	V_{IN}	MAX17554		10		60	V
		MAX17555		4		60	
Input Shutdown Current	I_{IN-SH}	$V_{EN/UV}$ = 0V (MAX17555)			3.8		µA
Input Supply Current	I_{IN-NL}	No Load (*Note 3*)	MAX17554A, MAX17555A		146		µA
			MAX17554B, MAX17555B		181		
			MAX17554C, MAX17555C		389		
TURN ON/OFF INPUT VOLTAGE (MAX17554)							
Input Voltage Turn-On Threshold	V_{ON}	V_{IN} rising		40	41.25	42.5	V
Input Voltage Turn-Off Threshold	V_{OFF}	V_{IN} falling		8	9	10	V
ENABLE/UNDERVOLTAGE (EN/UV) (MAX17555)							
EN/UV Threshold	V_{ENR}	$V_{EN/UV}$ rising		1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UV}$ falling		1.068	1.09	1.112	
	$V_{EN-TRUESD}$	$V_{EN/UV}$ falling, true shutdown			0.75		
EN/UV Input Leakage Current	$I_{EN/UV}$	$V_{EN/UV}$ = 1.3V, T_A = +25°C		-100		+100	nA
HIGH-SIDE AND LOW-SIDE MOSFETS							
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.05A (Sourcing)			5.4	10	Ω
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.05A (Sinking)			1.5	3	Ω
LX Leakage Current	I_{LX_LKG}	T_A = +25°C, V_{LX} = (V_{GND} + 1V) to (V_{IN} - 1V)		-1.5		+1	µA
SOFT-START (SS)							
Soft-Start Time	t_{SS}			0.72	0.8	0.88	ms
SS Delay		MAX17555, $V_{EN/UV}$ > V_{ENR}			170	275	µs
FEEDBACK/VOUTPUT (FB/VO)							
FB Regulation Voltage	V_{FB-REG}	MAX17554A, MAX17555A		3.25	3.3	3.35	V
		MAX17554B, MAX17755B		4.93	5	5.07	
		MAX17554C, MAX17555C		0.79	0.8	0.81	
FB Input Bias Current	$I_{FB/VO}$	MAX17554A/MAX17554B, MAX17555A/MAX17555B			360		µA
		MAX17554C, MAX17555C T_A = T_J = +25°C		-100		+100	nA

(V_{IN} = 24V, $V_{EN/UV}$ = 24V (MAX17555), V_{GND} = 0V, C_{IN} = 1µF, $V_{FB/VO}$ = 1.05 × V_{FB-REG}, LX = Unconnected, HYST = $\overline{RESET}$ = Unconnected (MAX17555), T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted. (*Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		210	240	280	mA
Valley Current-Limit Threshold	$I_{VALLEY-LIMIT}$	Up to 2 x t_{SS}	115	150	170	mA
		After 2 x t_{SS}	0	22	32	
Zero-Cross Threshold	I_{ZX}		-6	+2	+10	mA
OSCILLATOR						
Switching Frequency	f_{SW}			70		kHz
Switching Frequency Accuracy			-10		+10	%
TIMING						
Minimum On-Time	t_{ON_MIN}			80	105	ns
Minimum Off-Time	t_{OFF_MIN}			75	95	ns
Hiccup Timeout				64		ms
OUTPUT VOLTAGE STATUS ($\overline{RESET}$) (MAX17555)						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			400	mV
$\overline{RESET}$ Output Leakage Current		T_A = +25°C, $V_{\overline{RESET}}$ = 5.5V	-100		+100	nA
FB Thresholds for $\overline{RESET}$ Rising	V_{OKR}		93	95	97	%
FB Thresholds for $\overline{RESET}$ Falling	V_{OKF}		90	92	94	%
$\overline{RESET}$ Delay After FB Reach 95% Regulation	t_D			30		µs
HYST (MAX17555)						
HYST Output Level Low		V_{IN} = 2V, $V_{EN/UV}$ < V_{ENF}, I_{HYST} = 100µA			0.4	V
HYST Hi-Z Output Leakage Current		T_A = T_J = +25°C, V_{HYST} = 1.2V, $V_{EN/UV}$ > V_{ENR}	-100		+100	nA
HYST Sink Capability					100	µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		160		°C
Thermal Shutdown Hysteresis				20		°C

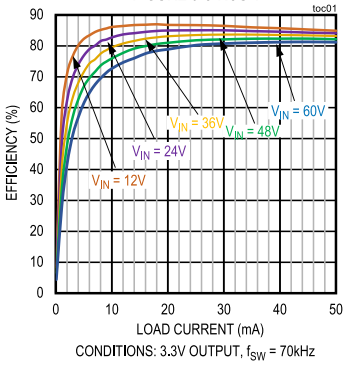
Note 2: All Electrical Specifications are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design and characterization.

Note 3: No load current is measured in the application circuits. For MAX17554C and MAX17555C, the output voltage is programmed to 3.3V

Typical Operating Characteristics

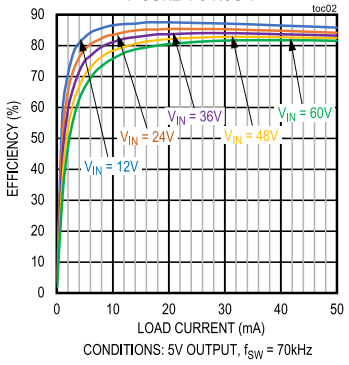
(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted. All voltages are referenced to GND, unless otherwise noted.)

MAX17554A, EFFICIENCY vs. LOAD CURRENT
FIGURE 3 CIRCUIT



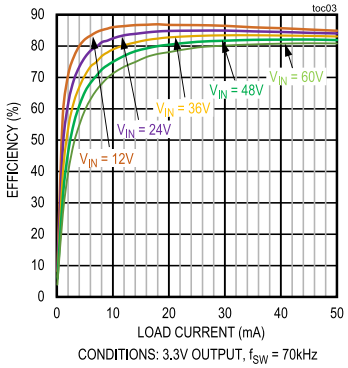
CONDITIONS: 3.3V OUTPUT, f_{SW} = 70kHz

MAX17554B, EFFICIENCY vs. LOAD CURRENT
FIGURE 4 CIRCUIT



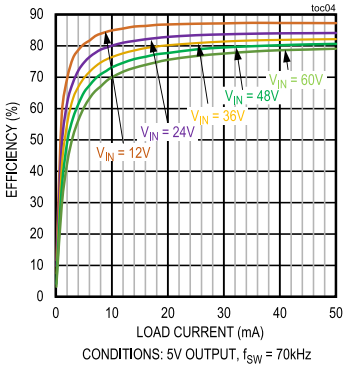
CONDITIONS: 5V OUTPUT, f_{SW} = 70kHz

MAX17555A, EFFICIENCY vs. LOAD CURRENT
FIGURE 5 CIRCUIT



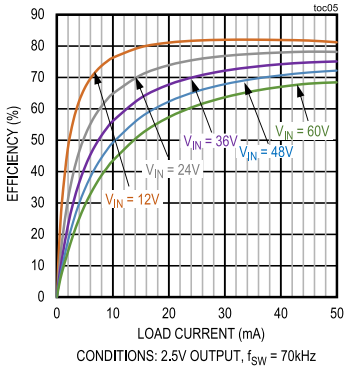
CONDITIONS: 3.3V OUTPUT, f_{SW} = 70kHz

MAX17555B, EFFICIENCY vs. LOAD CURRENT
FIGURE 6 CIRCUIT



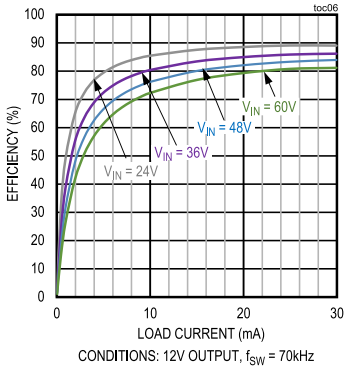
CONDITIONS: 5V OUTPUT, f_{SW} = 70kHz

MAX17554C, EFFICIENCY vs. LOAD CURRENT
FIGURE 7 CIRCUIT



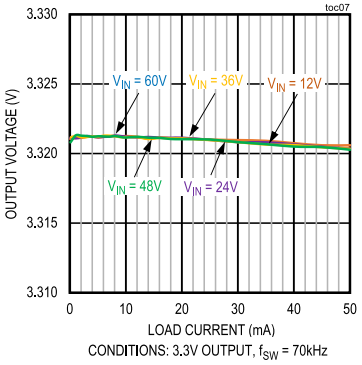
CONDITIONS: 2.5V OUTPUT, f_{SW} = 70kHz

MAX17555C, EFFICIENCY vs. LOAD CURRENT
FIGURE 8 CIRCUIT



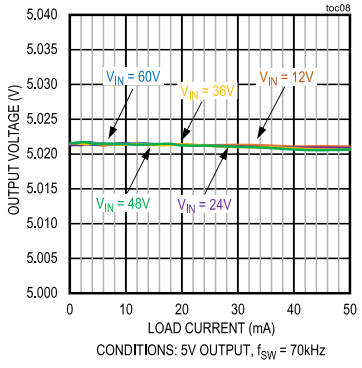
CONDITIONS: 12V OUTPUT, f_{SW} = 70kHz

MAX17554A, OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 3 CIRCUIT



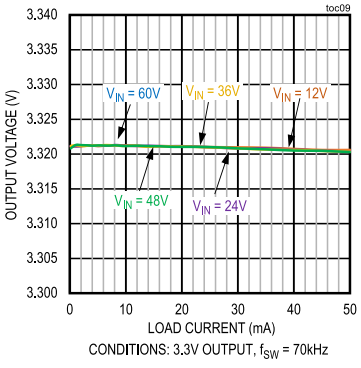
CONDITIONS: 3.3V OUTPUT, f_{SW} = 70kHz

MAX17554B, OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 4 CIRCUIT



CONDITIONS: 5V OUTPUT, f_{SW} = 70kHz

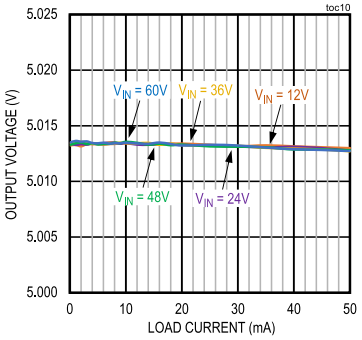
MAX17555A, OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 5 CIRCUIT



CONDITIONS: 3.3V OUTPUT, f_{SW} = 70kHz

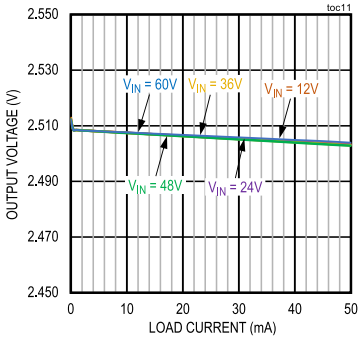
(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted. All voltages are referenced to GND, unless otherwise noted.)

MAX17555B, OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 6 CIRCUIT



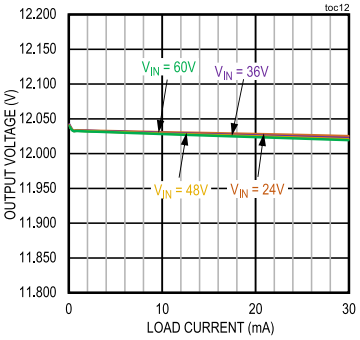
CONDITIONS: 5V OUTPUT, f_{SW} = 70kHz

MAX17554C, OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 7 CIRCUIT



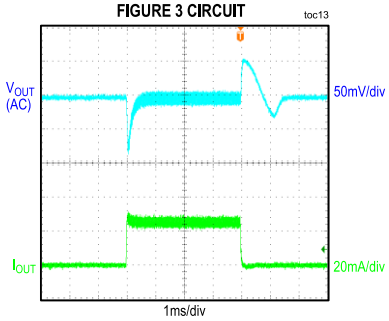
CONDITIONS: 2.5V OUTPUT, f_{SW} = 70kHz

MAX17555C, OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 8 CIRCUIT



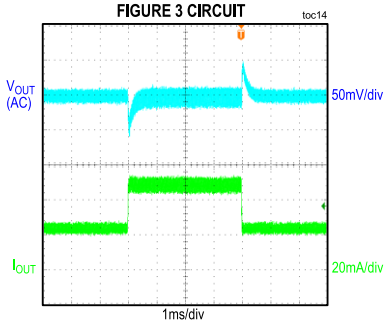
CONDITIONS: 12V OUTPUT, f_{SW} = 70kHz

MAX17554A
LOAD TRANSIENT BETWEEN 1mA AND 26mA
FIGURE 3 CIRCUIT



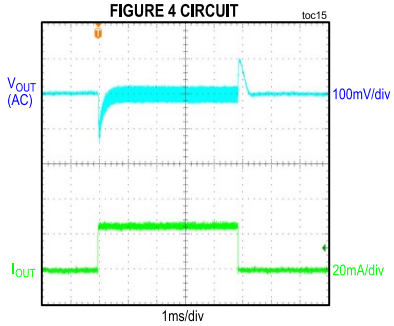
CONDITIONS: 3.3V OUTPUT, f_{SW} = 70kHz

MAX17554A
LOAD TRANSIENT BETWEEN 25mA AND 50mA
FIGURE 3 CIRCUIT



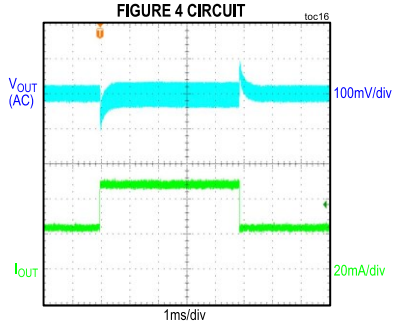
CONDITIONS: 3.3V OUTPUT, f_{SW} = 70kHz

MAX17554B
LOAD TRANSIENT BETWEEN 1mA AND 26mA
FIGURE 4 CIRCUIT



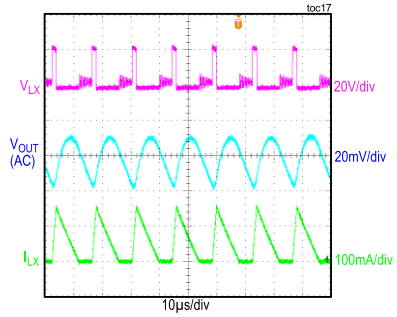
CONDITIONS: 5V OUTPUT, f_{SW} = 70kHz

MAX17554B
LOAD TRANSIENT BETWEEN 25mA AND 50mA
FIGURE 4 CIRCUIT



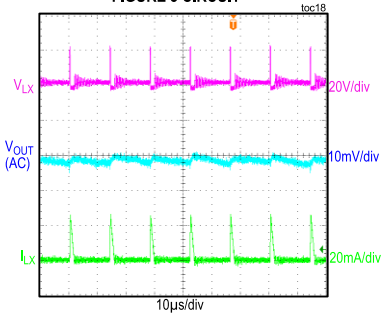
CONDITIONS: 5V OUTPUT, f_{SW} = 70kHz

MAX17554A, STEADY STATE PERFORMANCE
FIGURE 3 CIRCUIT



CONDITIONS: 3.3V OUTPUT, 50mA LOAD, f_{SW} = 70kHz

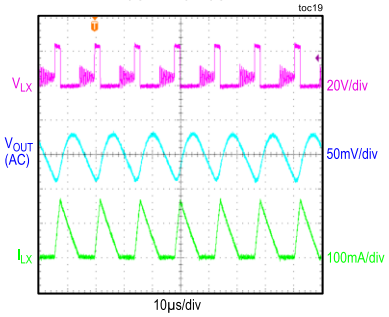
MAX17554A, STEADY STATE PERFORMANCE
FIGURE 3 CIRCUIT



CONDITIONS: 3.3V OUTPUT, 1mA LOAD, f_{SW} = 70kHz

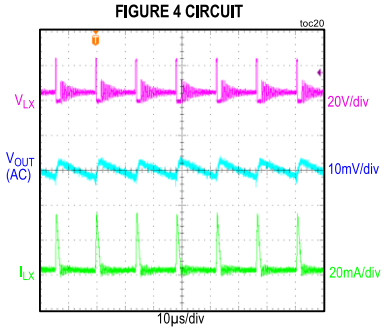
(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted. All voltages are referenced to GND, unless otherwise noted.)

MAX17554B, STEADY STATE PERFORMANCE
FIGURE 4 CIRCUIT



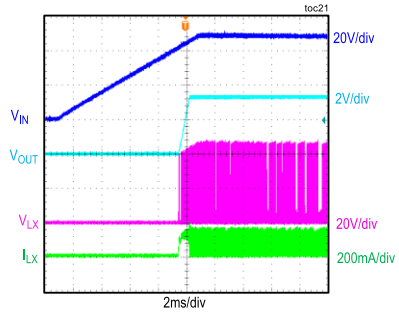
CONDITIONS: 5V OUTPUT, 50mA LOAD, f_{SW} = 70kHz

MAX17554B, STEADY STATE PERFORMANCE
FIGURE 4 CIRCUIT



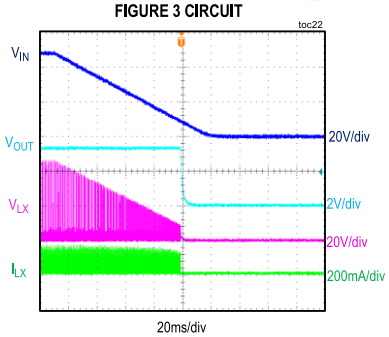
CONDITIONS: 5V OUTPUT, 1mA LOAD, f_{SW} = 70kHz

MAX17554A, SOFT-START THROUGH V_{IN}
FIGURE 3 CIRCUIT



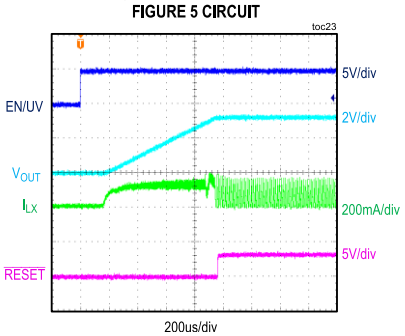
CONDITIONS: 3.3V OUTPUT, 66Ω LOAD, f_{SW} = 70kHz

MAX17554A, SHUT DOWN THROUGH V_{IN}
FIGURE 3 CIRCUIT



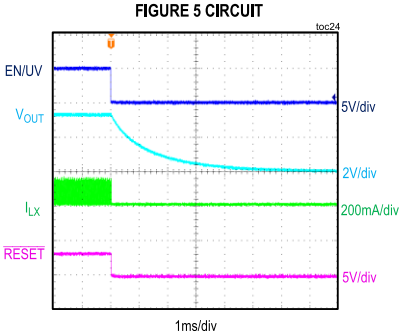
CONDITIONS: 3.3V OUTPUT, 66Ω LOAD, f_{SW} = 70kHz

MAX17555A, SOFT-START THROUGH EN/UV
FIGURE 5 CIRCUIT



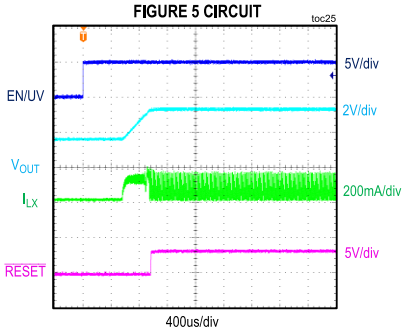
CONDITIONS: 3.3V OUTPUT, 66Ω LOAD, f_{SW} = 70kHz

MAX17555A, SHUT DOWN THROUGH EN/UV
FIGURE 5 CIRCUIT



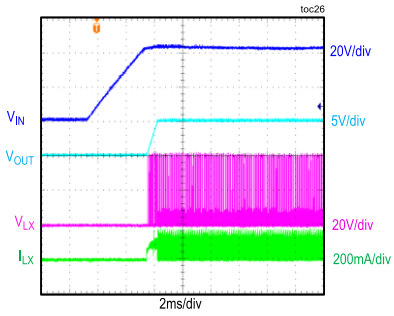
CONDITIONS: 3.3V OUTPUT, 66Ω LOAD, f_{SW} = 70kHz

MAX17555A
SOFT-START WITH PREBIAS VOLTAGE OF 1.65V
FIGURE 5 CIRCUIT



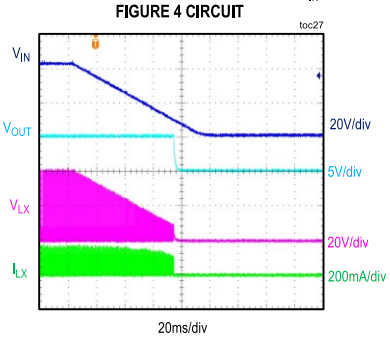
CONDITIONS: 3.3V OUTPUT, 66Ω LOAD, f_{SW} = 70kHz

MAX17554B, SOFT-START THROUGH V_{IN}
FIGURE 4 CIRCUIT



CONDITIONS: 5V OUTPUT, 100Ω LOAD, f_{SW} = 70kHz

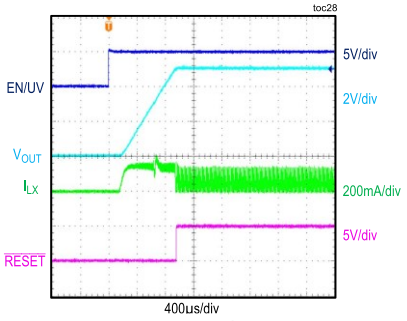
MAX17554B, SHUT DOWN THROUGH V_{IN}
FIGURE 4 CIRCUIT



CONDITIONS: 5V OUTPUT, 100Ω LOAD, f_{SW} = 70kHz

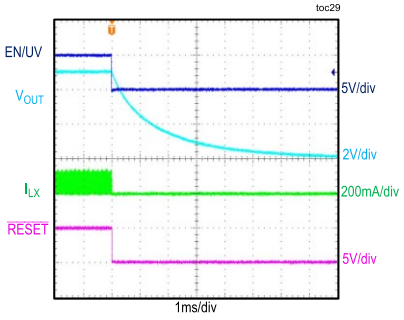
(V_{IN} = $V_{EN/UV}$ = 24V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted. All voltages are referenced to GND, unless otherwise noted.)

MAX17555B, SOFT-START THROUGH EN/UV
FIGURE 6 CIRCUIT



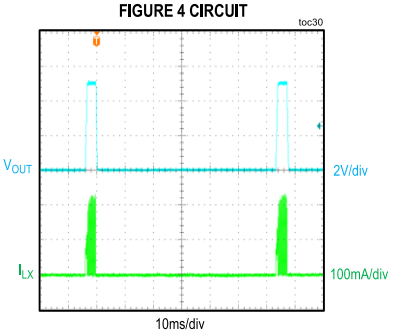
CONDITIONS: 5V OUTPUT, 100Ω LOAD, f_{SW} = 70kHz

MAX17555B, SHUT DOWN THROUGH EN/UV
FIGURE 6 CIRCUIT

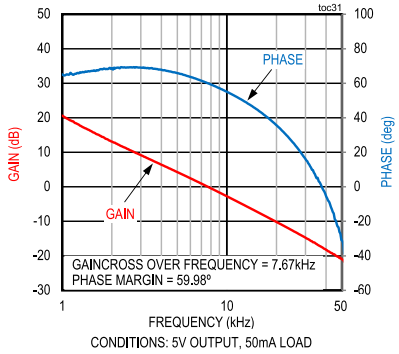


CONDITIONS: 5V OUTPUT, 100Ω LOAD, f_{SW} = 70kHz

MAX17554B, OVERLOAD PROTECTION
FIGURE 4 CIRCUIT

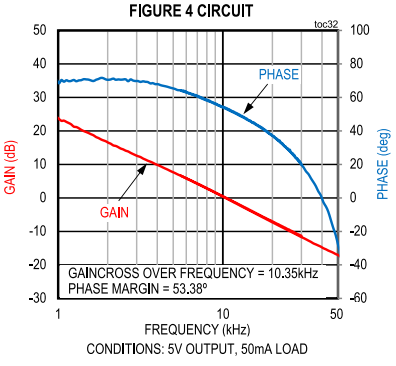


MAX17554A, BODE PLOT
FIGURE 3 CIRCUIT



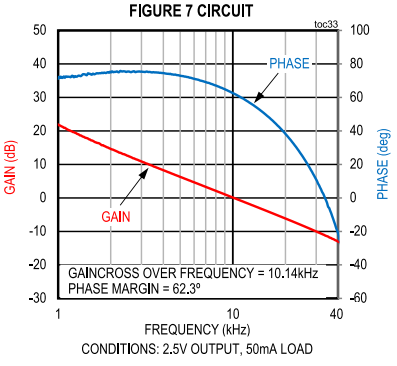
CONDITIONS: 5V OUTPUT, 50mA LOAD

MAX17554B, BODE PLOT
FIGURE 4 CIRCUIT



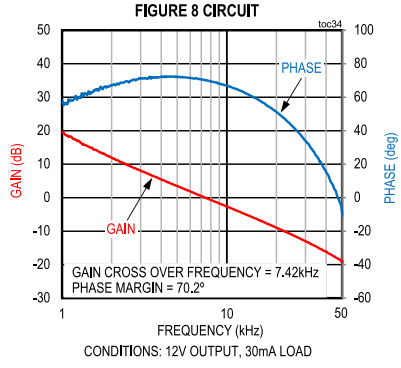
CONDITIONS: 5V OUTPUT, 50mA LOAD

MAX17554C, BODE PLOT
FIGURE 7 CIRCUIT



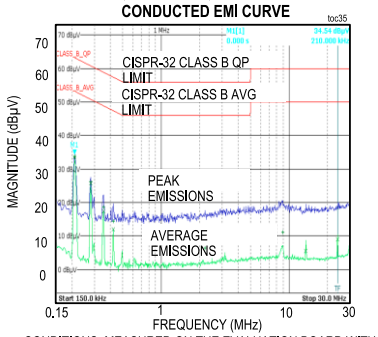
CONDITIONS: 2.5V OUTPUT, 50mA LOAD

MAX17555C, BODE PLOT
FIGURE 8 CIRCUIT



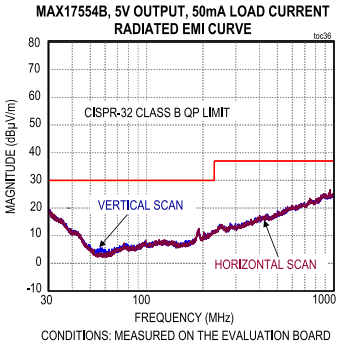
CONDITIONS: 12V OUTPUT, 30mA LOAD

MAX17554B, 5V OUTPUT, 50mA LOAD CURRENT
CONDUCTED EMI CURVE



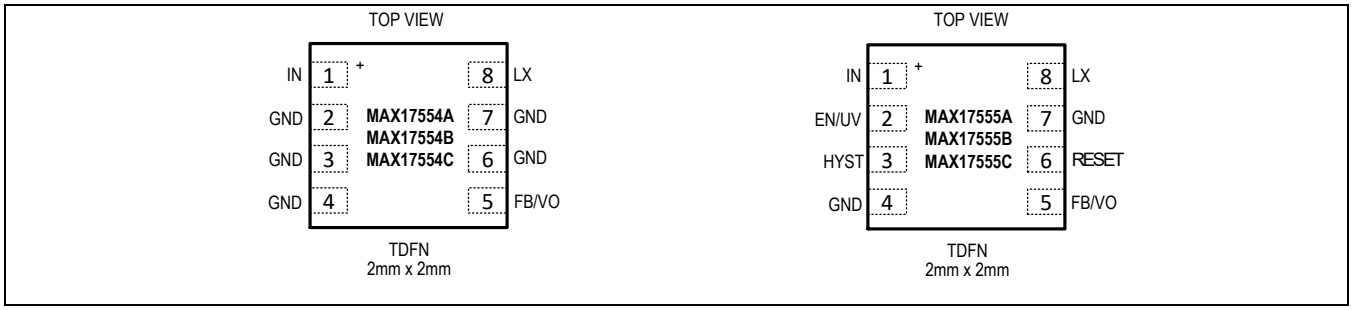
CONDITIONS: MEASURED ON THE EVALUATION BOARD WITH L2 = 15µH, C2 = 4.7µF/100V/X7R/0805

MAX17554B, 5V OUTPUT, 50mA LOAD CURRENT
RADIATED EMI CURVE



CONDITIONS: MEASURED ON THE EVALUATION BOARD

Pin Configurations

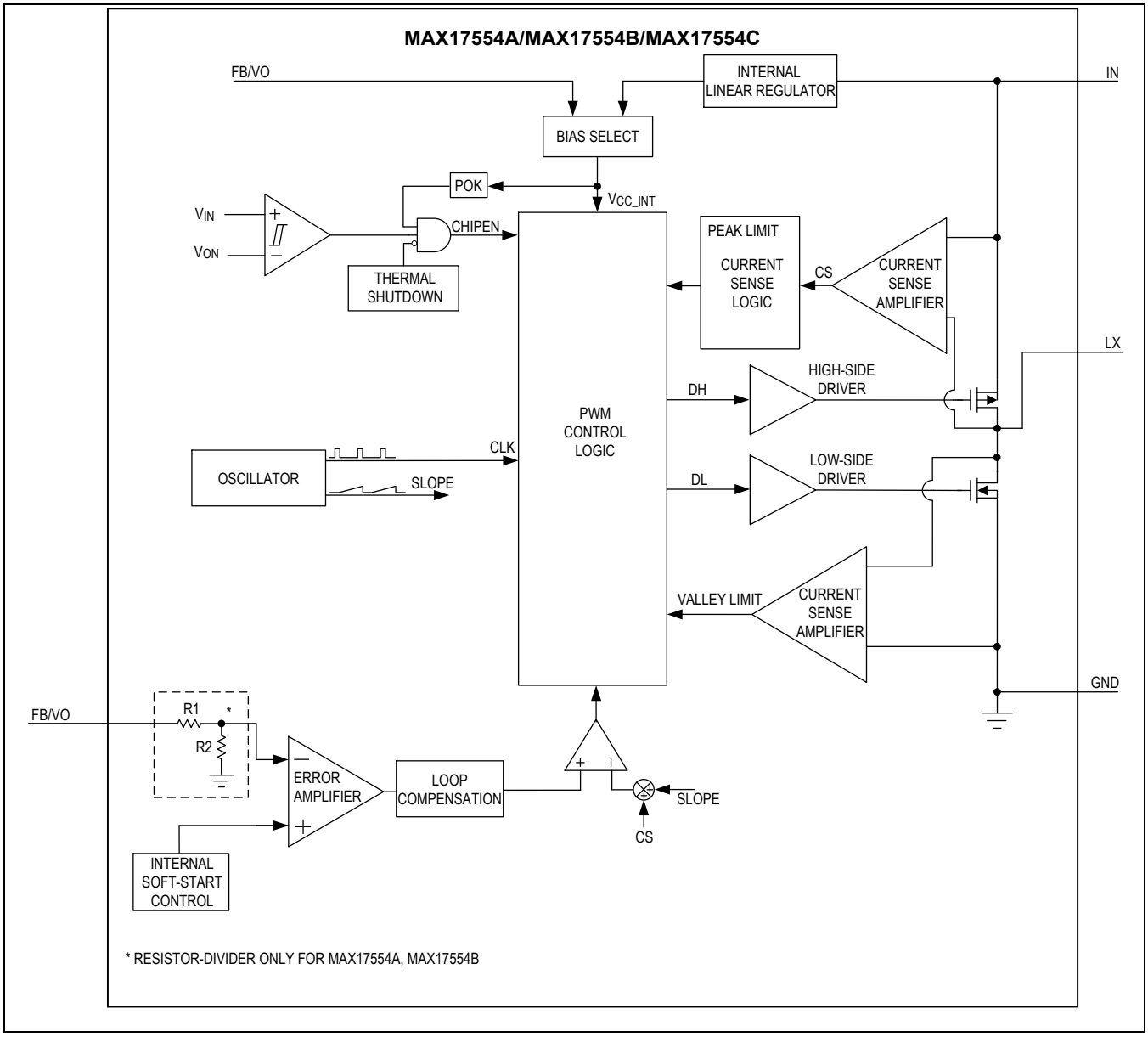


Pin Descriptions

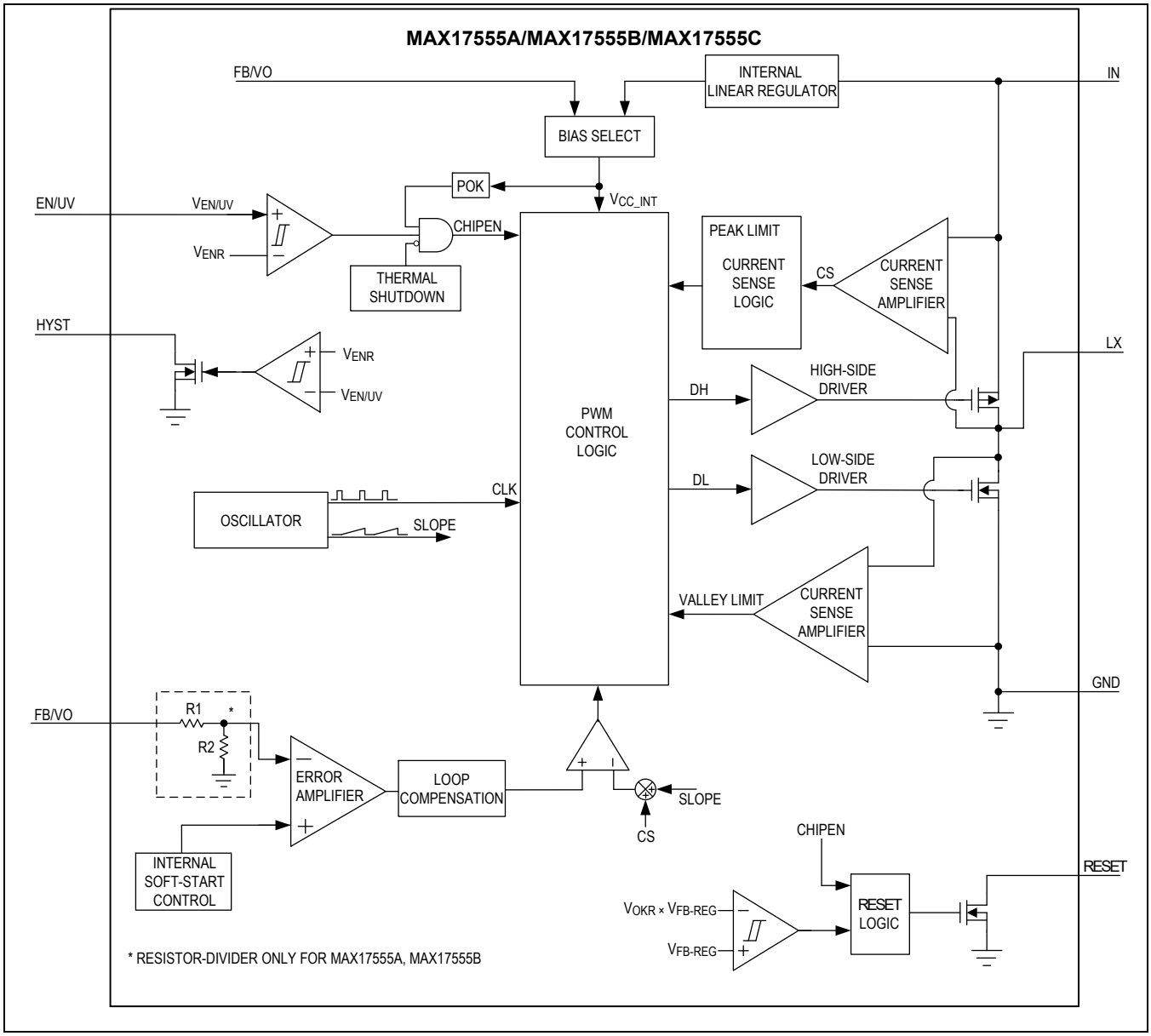
PIN	NAME	FUNCTION
1	IN	Power Supply Input Pin. Decouple to GND with a 1µF capacitor. Place the capacitor close to IN and GND pins.
2	GND, EN/UV	MAX17554: Connect to GND. MAX17555: Enable/Undervoltage Lockout Pin. Drive EN/UV high to enable the output voltage. Connect to the midpoint of a resistor-divider from IN to GND to set the input voltage at which the device turns ON. The allowed minimum turn off input voltage is 3.85V. Pull low to GND for disabling the device.
3	GND, HYST	MAX17554: Connect to GND. MAX17555: Converter Turn ON/OFF Hysteresis Programming Pin. Connect HYST to EN/UV with an external resistor to set the required hysteresis. HYST goes high impedance when EN/UV > 1.215V (typ) and pulls low when EN/UV < 1.09V (typ)
4	GND	Connect to GND.
5	FB/VO	Feedback Input. For fixed output parts (MAX17554A/MAX17554B, MAX17555A/MAX17555B), connect the output voltage node V_{OUT} to FB/VO pin for both feedback and boot-strap function. Connect FB/VO to the center node of an external resistor-divider from the output to GND to set the output voltage for MAX17554C and MAX17555C. See the *Adjusting the Output Voltage* section for more details.
6	GND, $\overline{\text{RESET}}$	MAX17554: Connect to GND. MAX17555: Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB/VO drops below 92% (typ) of its set value. $\overline{\text{RESET}}$ goes high impedance 30µs after FB/VO voltage rises above 95% (typ) of its set value. See Electrical Characteristics section for more details.
7	GND	Ground. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. See the *PCB Layout Guidelines* section.
8	LX	Switching Node Pin. Connect LX to the switching-side of the inductor. LX is high impedance when the device is in shutdown mode.

Functional Block Diagrams

MAX17554



MAX17555


MAX17555A/MAX17555B/MAX17555C
FB/VO
INTERNAL LINEAR REGULATOR
IN
BIAS SELECT
POK
VCC_INT
EN/UV
VEN/UV
VENR
CHIPEN
THERMAL SHUTDOWN
PEAK LIMIT
CURRENT SENSE LOGIC
CS
CURRENT SENSE AMPLIFIER
HYST
VENR
VEN/UV
LX
DH
HIGH-SIDE DRIVER
PWM CONTROL LOGIC
DL
LOW-SIDE DRIVER
CLK
OSCILLATOR
SLOPE
VALLEY LIMIT
CURRENT SENSE AMPLIFIER
GND
FB/VO
R1
*
R2
ERROR AMPLIFIER
LOOP COMPENSATION
SLOPE
CS
CHIPEN
RESET
INTERNAL SOFT-START CONTROL
VOKR × VFB-REG
VFB-REG
RESET LOGIC
* RESISTOR-DIVIDER ONLY FOR MAX17555A, MAX17555B

Detailed Description

MAX17554 and MAX17555 are ultra-small, high-efficiency, high voltage, synchronous step-down DC-DC converters with integrated MOSFETs that operate over a wide input voltage range and deliver up to 50mA of load current. The MAX17554 operates over a wide input voltage range from 10V to 60V and the MAX17555 operates over a wide input voltage range from 4V to 60V. The MAX17554 offers a converter solution with only three active pins, whereas the MAX17555 offers a flexible converter design in terms of EN/UV and HYST thresholds and $\overline{\text{RESET}}$ features. MAX17554A/MAX17555A and MAX17554B/MAX17555B are fixed 3.3V and 5V output voltage devices, respectively. MAX17554C/MAX17555C are adjustable output (0.8V to 0.9 x V_{IN}) devices. The feedback voltage regulation accuracy of the converters over the -40°C to +125°C temperature range is ±1.5% for MAX17554A/MAX17555A and MAX17554B/MAX17555B, and ±1.25% for MAX17554C/MAX17555C.

The devices feature a peak-current mode control architecture. During normal operation, at each rising edge of the clock, the high-side p-MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached or the peak current limit is detected. During the high-side p-MOSFET on-time, the inductor current ramps up. During the rest of the switching cycle or until the inductor current reaches zero, the high-side p-MOSFET remains off, the low-side n-MOSFET remains on, and the inductor current ramps down. The device features the Discontinuous Conduction Mode (DCM), in which the negative inductor current is inhibited to enable higher light load efficiency. In DCM, the device operates at a fixed switching frequency until the minimum on-time is reached. If the load demand is less than the energy corresponding to the minimum on-time pulse, the converter skips pulses to maintain output voltage regulation.

A fixed soft-start time of 0.8ms (typ) allows users to reduce input inrush current. The MAX17555 features an enable/undervoltage lockout (EN/UV) and a hysteresis (HYST) pins to allow the users to turn the device on or off at the desired input-voltage level. The MAX17555 also features an open-drain $\overline{\text{RESET}}$ pin to provide a power-good signal to the system upon achieving successful regulation of the output voltage.

Enable/Undervoltage Input (EN/UV) with HYST (MAX17555)

The device features an enable/undervoltage lockout (EN/UV) pin and a hysteresis (HYST) pin that allow the user to turn the device on or off at the desired input-voltage level. EN/UV can also be used to enable/disable the converter. Driving EN/UV low (below V_{ENF}) disables both power MOSFETs as well as other internal circuitry, and reduces IN quiescent current to below 3.8µA (typ). Driving EN/UV high (above V_{ENR}) enables the converter. An external voltage-divider between IN and EN/UV to GND and an external resistor from HYST to EN/UV adjusts the input voltage at which the device turns on or turns off. See the *Setting the Input Undervoltage Level with Hysteresis* section for more details.

When the part is enabled, the device's internal error-amplifier reference voltage starts to ramp up after an internal delay. In the MAX17555 while operating within input range, the maximum internal delay of 170µs (typ) is observed when EN/UV voltage rises above 1.215V (typ). In the MAX17554, the maximum internal delay of 170µs (typ) is observed when the input voltage rises above V_{ON}. The duration of the soft-start ramp is 800µs (typ), allowing a smooth increase of the output voltage.

Reset Output ($\overline{\text{RESET}}$) (MAX17555)

The device includes an open-drain $\overline{\text{RESET}}$ output to monitor the output voltage. $\overline{\text{RESET}}$ goes to high impedance 30µs (typ) after the regulator output voltage increases above 95% (typ) of the nominal set voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops below 92% (typ) of the nominal set voltage. $\overline{\text{RESET}}$ also goes low when EN/UV is pulled low, and during the hiccup time out period.

Startup into Prebiased Output

The device supports prebiased startup. When the device starts into a prebiased output, both the high-side and the low-side MOSFETs are turned off so that the converter does not sink current from the output. High-side and low-side MOSFETs do not start switching until the pulse width modulation (PWM) comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Overcurrent Protection

The devices implement a hysteretic peak current limit protection scheme to protect the internal MOSFETs and inductor under output short circuit conditions. When the inductor peak current exceeds $I_{PEAK-LIMIT}$ (0.24A typ), the high side switch is turned off and the low side switch is turned on to reduce the inductor current. After the current is reduced to $I_{VALLEY-LIMIT}$ (0.15A typ during startup and 0.022A typ during steady state), the high-side MOSFET is turned on at the rising edge of the next clock pulse. Since the inductor current is bounded between the two values, the inductor current runaway never happens in this scheme. The devices enter hiccup mode if the inductor current hits $I_{PEAK-LIMIT}$ for 16 consecutive times. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 64ms (typ). Once the hiccup timeout period expires, soft-start is attempted again. The hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the devices. When the junction temperature of the devices exceeds +160°C (typ), a thermal sensor shuts down the devices, allowing the devices to cool. The thermal sensor turns the devices on again after the junction temperature cools by 20°C (typ). Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown protection in normal operation.

Applications Information

Inductor Selection

The MAX17554/5 are designed for discontinuous conduction mode (DCM) of operation to achieve high light load efficiency. Operating the converter in DCM for the entire operating range allows the selection of a smaller inductor, and hence reduces the solution size. Use the following equation to keep the converter in DCM for the entire operating range:

$$L_{MAX} \leq \frac{V_{OUT} + I_{OUT(MAX)} \times (R_{DS\text{-}ONL(MAX)} + R_{DCR(MAX)})}{2 \times I_{OUT(MAX)} \times f_{SW}} \times \left(1 - \frac{V_{OUT} + I_{OUT(MAX)} \times (R_{DS\text{-}ONL(MAX)} + R_{DCR(MAX)})}{V_{IN(MIN)} - I_{OUT(MAX)} \times (R_{DS\text{-}ONH(MAX)} - R_{DS\text{-}ONL(MAX)})}\right) \times (1\text{-}TOL)$$

where:

V_{OUT} = Steady-state output voltage in V,

$I_{OUT(MAX)}$ = Maximum load current in A,

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor in Ω,

f_{SW} = Switching frequency in Hz,

$V_{IN(MIN)}$ = Minimum operating input voltage in V,

$R_{DS\text{-}ONL(MAX)}$ and $R_{DS\text{-}ONH(MAX)}$ = Worst-case on-state resistance of low-side and high-side MOSFETs respectively in Ω,

TOL = Tolerance of inductor in pu.

The inductor peak current should not exceed the minimum peak current limit of the device ($I_{PEAK\text{-}LIMIT}$, 210mA min) in order to not trigger overcurrent/hiccup protection. Use the following equation to ensure the maximum inductor peak current is less than 210mA:

$$L_{MIN} \geq \frac{45.4 \times I_{OUT} \times V_{OUT}}{(1\text{-}TOL) \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The selected inductor (L_{SEL}) should meet following criteria:

$$L_{MIN} \leq L_{SEL} \leq L_{MAX}$$

In the design cases where the calculated L_{MIN} is higher than L_{MAX}, either reduce the output current or increase the $V_{IN(MIN)}$ for a feasible design solution.

Since the MAX17554/5 operates in DCM, the device switches at a fixed frequency until the minimum on-time (t_{ON_MIN}) is reached. If the load demand is less than the energy corresponding to the minimum on-time pulse, the converter skips switching pulses to maintain the output voltage regulation. For the L_{SEL}, use the following formula to calculate the minimum load current required to operate at a fixed switching frequency:

$$I_{OUT\_MIN} = \frac{0.5 \times (V_{IN} - V_{OUT}) \times V_{IN} \times t^2_{ON\_MIN} \times f_{SW}}{V_{OUT} \times L_{SEL}}$$

where:

V_{IN} = Operating input voltage in V,

t_{ON_MIN} = Minimum on-time in s.

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source, switching noise, and voltage ripple on the input. Use low-ESR ceramic capacitors with high ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Decouple IN to GND with a minimum of 1µF/1206 package or equivalent capacitor. Calculate the input capacitance using the following equation based on the input ripple requirement:

$$C_{IN} = \frac{I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

V_{IN} = Input voltage in V,

V_{OUT} = Steady-state output voltage in V,

$I_{OUT(MAX)}$ = Maximum load current in A,

f_{SW} = Switching frequency in Hz,

ΔV_{IN} = Allowable input voltage ripple in V,

η = Efficiency.

In applications where the source is distant from the device input, an appropriate electrolytic capacitor should be added to provide necessary damping for potential oscillations caused by the inductance of the input power path and input ceramic capacitor.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability at temperatures in industrial applications. It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in the application. The output capacitor has two functions: it stores sufficient energy to support the output voltage under load transient conditions and stabilizes the device's internal control loop. The required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{18.7 \times 10^{-3}}{V_{OUT}} \sqrt{\frac{L_{SEL}}{\frac{V_{OUT}}{I_{OUT}} \times (1 - \frac{V_{OUT}}{60})}}$$

The approximate steady state output voltage ripple in DCM can be calculated by the following equation:

$$\Delta V_{OUTDCM} = \frac{0.5 \times (I_{PK\text{-}DCM} - I_{OUT})^2 \times L_{SEL}}{C_{OUT}} \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)$$

$$I_{PK\text{-}DCM} = \sqrt{\frac{2 \times I_{OUT} \times V_{OUT}}{L_{SEL} \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where:

I_{OUT} = Load current in A,

L_{SEL} = Selected inductance in H,

V_{IN} = Input voltage in V,

V_{OUT} = Steady-state output voltage in V,

f_{SW} = Switching frequency in Hz.

Setting the Input Undervoltage Level with Hysteresis (MAX17555)

The device offers an adjustable input undervoltage and adjustable hysteresis levels. Set the voltage at which the device turns on with a resistive voltage-divider connected from IN to GND and a resistor from HYST to EN/UV (see *Figure 1*).

Connect the center node of the resistive voltage-divider to EN/ UV pin. Choose R1 to be 3.32MΩ (max) and then calculate R2 and R3 as follows:

$$R2=\frac{V_{ENF}\times R1}{(V_{IN(OFF)}-V_{ENF})}$$

$$R3=\frac{V_{ENR}\times R1\times R2}{\left(V_{IN(ON)}\times R2-V_{ENR}\times(R1+R2)\right)}$$

where $V_{IN(ON)}$ and $V_{IN(OFF)}$ are the voltages at which the device is required to turn on and turn off, respectively. While selecting the above resistors, the HYST pin sink current capability given in *Electrical Characteristics* table should be considered.

When the HYST function is not used, connect the HYST pin to GND (see *Figure 1*) and calculate R2 as follows:

$$R2=\frac{V_{ENR}\times R1}{(V_{IN(ON)}-V_{ENR})}$$

If the EN/UV pin is driven from an external signal source, it is recommended to place a series resistance of minimum 1kΩ between the signal source output and the EN/UV pin to reduce voltage ringing on the line.

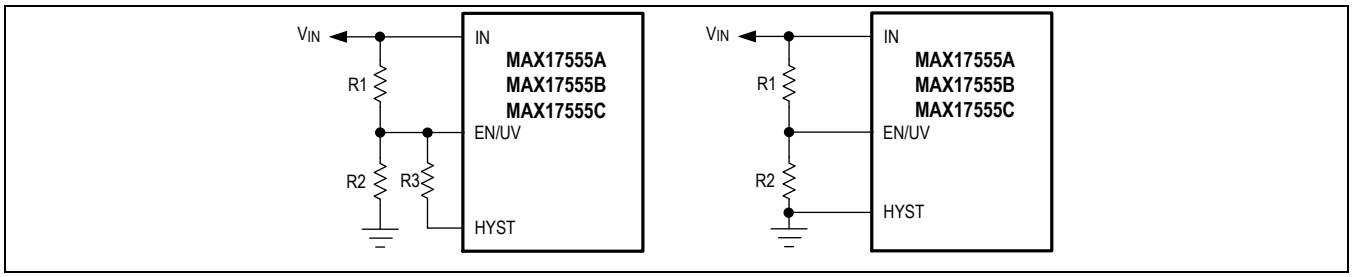


Figure 1. Setting the Input Undervoltage Level with and without Hysteresis

Adjusting the Output Voltage

For the MAX17554A, MAX17554B, MAX17555A, and MAX1755B, connect FB/VO directly to the output node of the step-down converter. The output voltage of MAX17554C and MAX17555C can be programmed from 0.8V to 0.9 x VIN. Set the output voltage by using a resistive feedback divider from output to GND (see *Figure 2*). Connect the center node of the divider to the FB/VO pin. Choose R_B less than or equal to 100kΩ and calculate R_U with the following equation:

$$R_U=R_B\times\left[\frac{V_{OUT}}{0.8}-1\right]$$

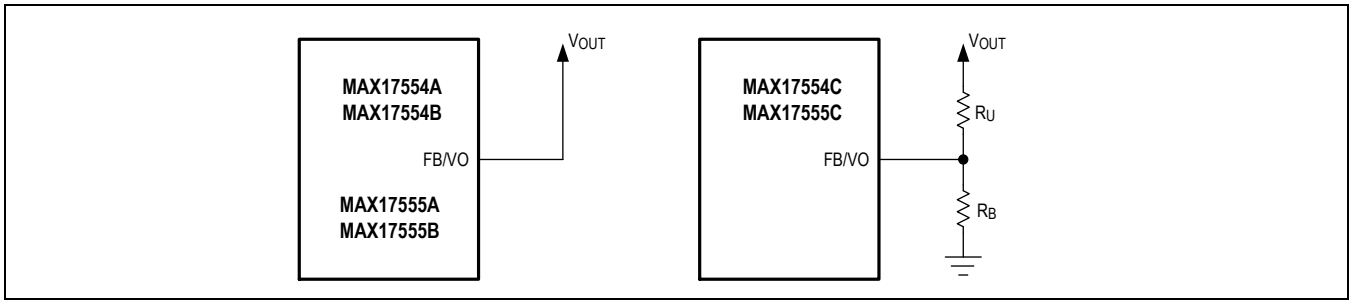


Figure 2. Setting the Output Voltage

Power Dissipation

At a particular operating condition, the power losses that lead to the temperature rise of the device are estimated as follows:

$$P_{LOSS} = P_{OUT} \times \left(\frac{1}{\eta} - 1\right) - \left(I_{OUT}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

P_{OUT} = Output power in W,

η = Efficiency of the converter,

R_{DCR} = DC resistance of the output inductor in Ω.

See the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions. The Theta-JA (θ_{JA}) of the package is as follows:

$$\theta_{JA} = 162°C/W$$

The maximum junction temperature ($T_{J(MAX)}$) of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + \left(\theta_{JA} \times P_{LOSS}\right)$$

Junction temperature greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the IN pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity. PCB layout also affects the thermal performance of the design. For a sample layout that ensures first pass success, refer to the MAX17554 evaluation kit layout available at *www.maximintegrated.com.*

Typical Application Circuits

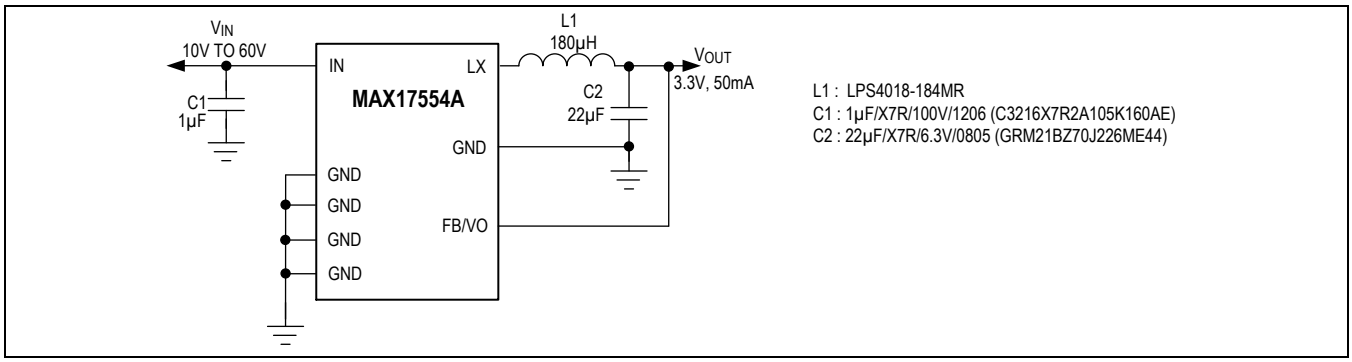


Figure 3. Fixed 3.3V, 50mA Step-Down Converter Output with 10V VINMIN

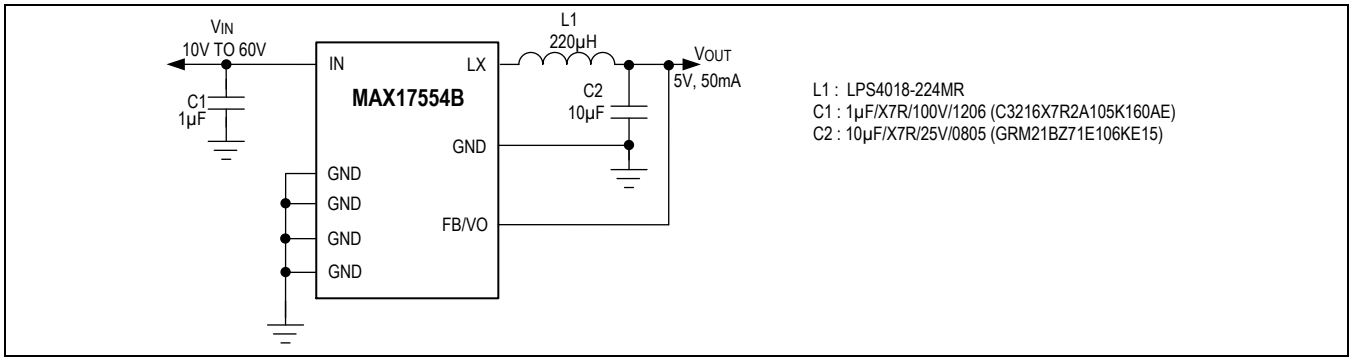


Figure 4. Fixed 5V, 50mA Step-Down Converter Output with 10V VINMIN

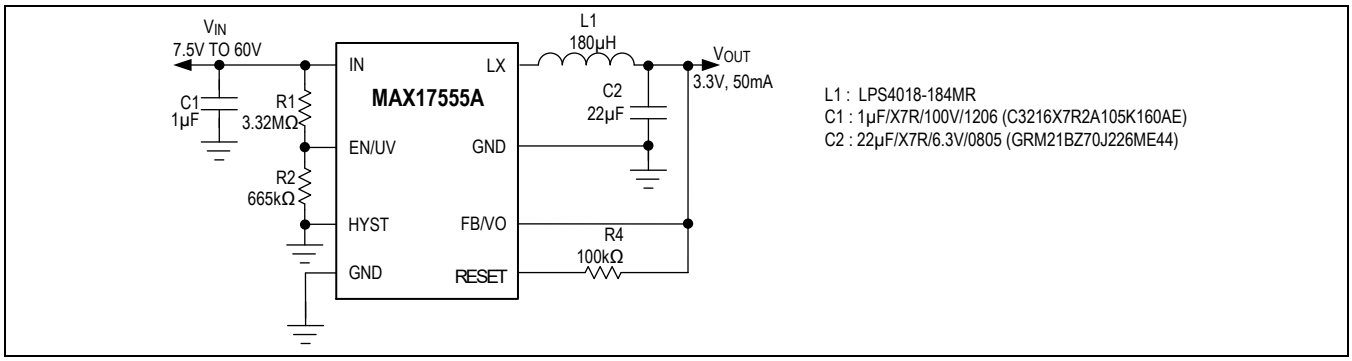


Figure 5. Fixed 3.3V, 50mA Step-Down Converter Output with 7.5V VINMIN

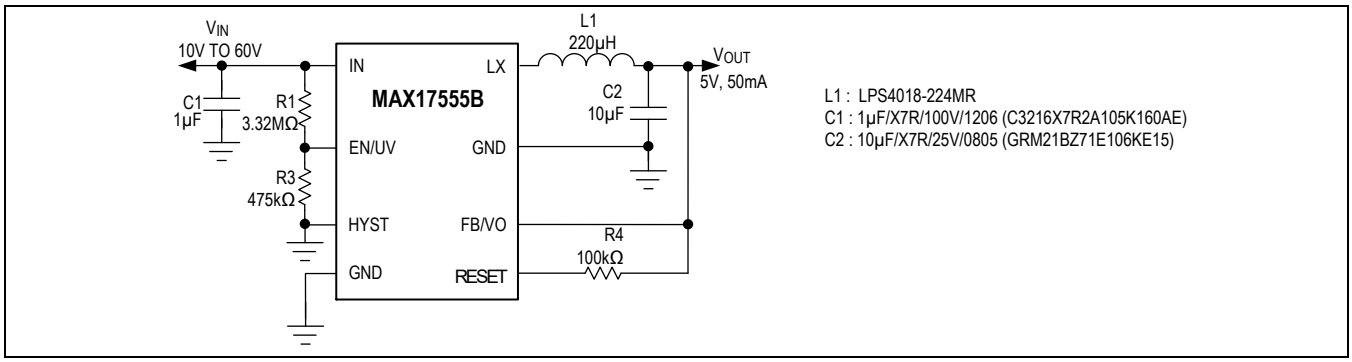


Figure 6. Fixed 5V, 50mA Step-Down Converter Output with 9.5V VINMIN

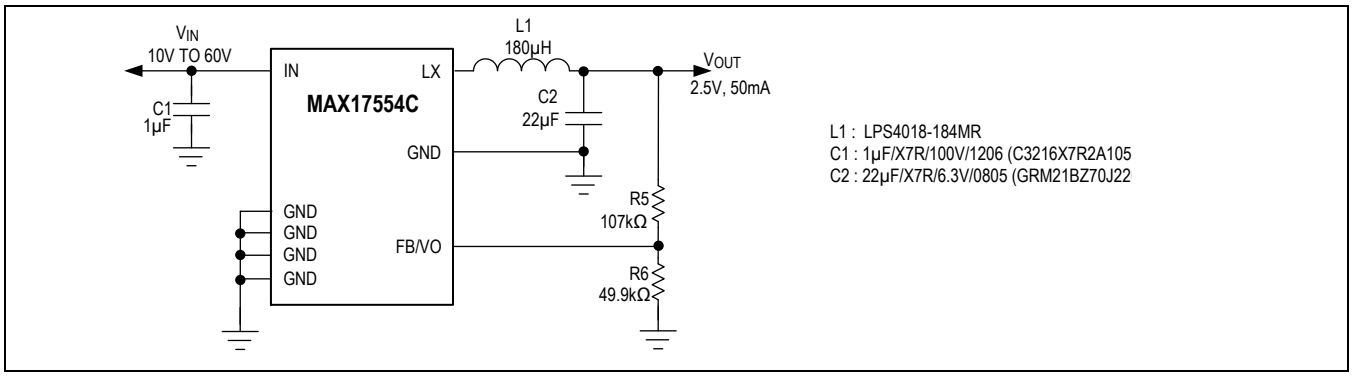


Figure 7. 2.5V, 50mA Step-Down Converter Output with 10V VINMIN

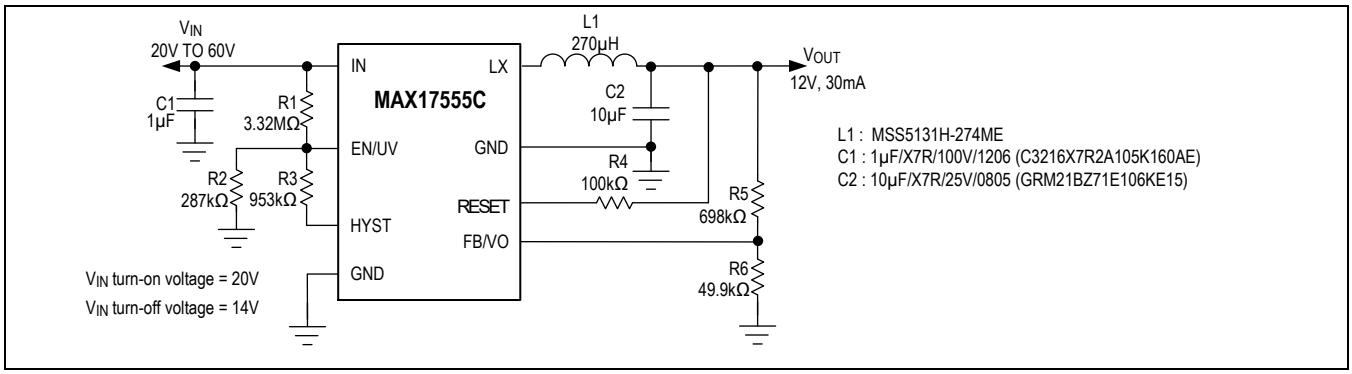


Figure 8. 12V, 30mA Step-Down Converter Output with 20V VINMIN

Ordering Information

PART NUMBER	OUTPUT VOLTAGE	PIN-PACKAGE
MAX17554AATA+	3.3	8-TDFN
MAX17554AATA+T	3.3	8-TDFN
MAX17554BATA+	5	8-TDFN
MAX17554BATA+T	5	8-TDFN
MAX17554CATA+	Adjustable	8-TDFN
MAX17554CATA+T	Adjustable	8-TDFN
MAX17555AATA+	3.3	8-TDFN
MAX17555AATA+T	3.3	8-TDFN
MAX17555BATA+	5	8-TDFN
MAX17555BATA+T	5	8-TDFN
MAX17555CATA+	Adjustable	8-TDFN
MAX17555CATA+T	Adjustable	8-TDFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/22	Release for Market Intro	—
1	5/22	Updated TOC36 in the *Typical Operating Characteristics* section, and the *Ordering Information* table	8, 20