MP6619L

2.5V to 28V, 5A H-Bridge Motor Driver

DESCRIPTION

The MP6619L is an H-bridge motor driver. It operates from a supply input voltage (V_{IN}) up to 28V and delivers a motor current up to 5A. The MP6619L is ideally suited to drive a brushed DC motor.

The MP6619L also has a configurable current limit. Full protection features include over-current protection (OCP), V_{IN} over-voltage protection (OVP), V_{CC} under-voltage lockout (UVLO), and thermal shutdown.

The MP6619L is available in a QFN-19 (3mmx3mm) package.

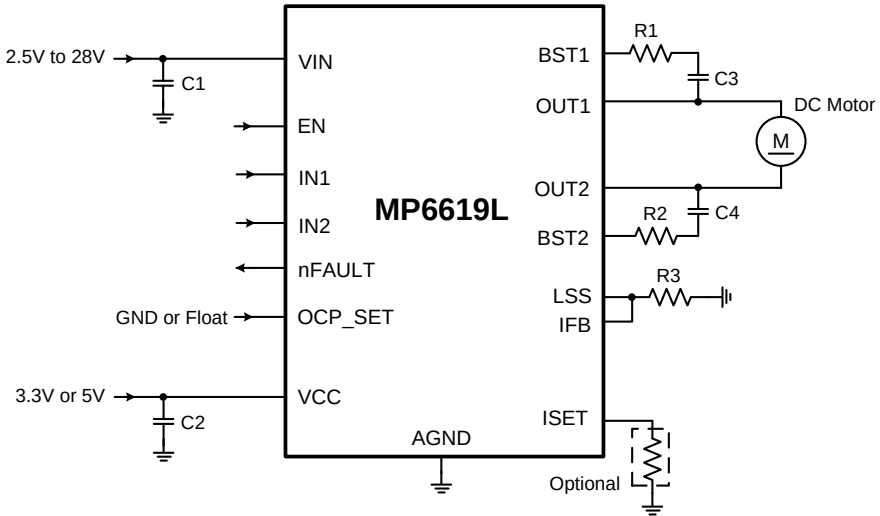
FEATURES

- Wide 2.5V to 28V Operating Input Voltage (V_{IN}) Range
- Up to 5A Peak Output Current (I_{OUT})
- Compliance with 3.3V and 5V Systems
- Internal H-Bridge Driver
- Configurable Current Limit
- 65mΩ On Resistance ($R_{DS(ON)}$) for Each Half-Bridge MOSFET with 5V V_{CC}
- 100% Duty Cycle Operation of H-Bridge
- 1μA Shutdown Mode
- Over-Current Protection (OCP)
- V_{IN} Over-Voltage Protection (OVP)
- V_{CC} Under-Voltage Lockout (UVLO)
- Over-Temperature (OT) Shutdown
- Fault Indication Output
- Available in a QFN-19 (3mmx3mm) Package

APPLICATIONS

- DC Motors
- Solenoids and Actuators

TYPICAL APPLICATION

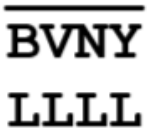


ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6619LGQ	QFN-19 (3mmx3mm)	*See Below*	1

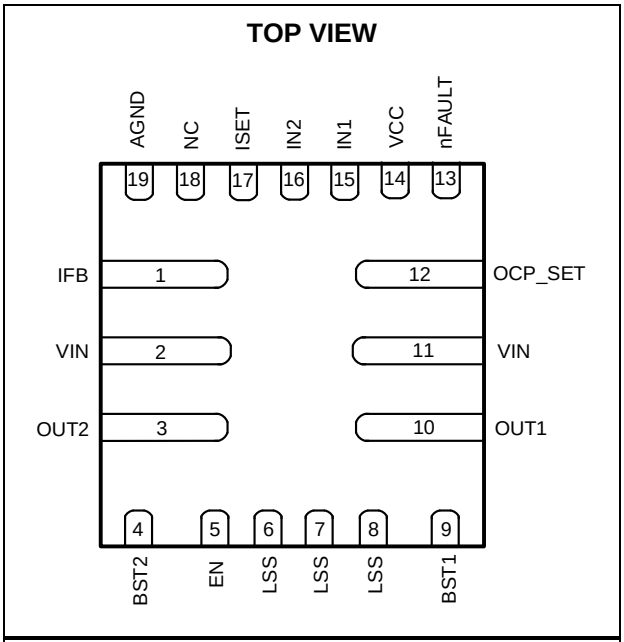
* For Tape & Reel, add suffix -Z (e.g. MP6619LGQ-Z).

TOP MARKING



BVN: Product code of MP6619LGQ
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-19 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	IFB	**Current-sense signal feedback.** Connect the IFB pin to LSS.
2, 11	VIN	**Input supply for motor driver.**
3	OUT2	**Output terminal 2.**
4	BST2	**Bootstrap (BST) pin for the OUT2 high-side MOSFET (HS-FET) gate driver.** Connect a capacitor between the BST2 and OUT2 pins.
5	EN	**IC enable.** Pull down the EN pin internally.
6, 7, 8	LSS	**Low-side (LS) source connection.** For current sense, connect a current-sense resistor between the LSS pin and power ground.
9	BST1	**BST pin for the OUT1 HS-FET gate driver.** Connect a capacitor between the BST1 and OUT1 pins.
10	OUT1	**Output terminal 1.**
12	OCP_SET	**Over-current protection (OCP) setting.** Float the OCP_SET pin or connect it to AGND. Float OCP_SET to enable OCP; pull OCP_SET logic low to disable OCP.
18	NC	**Not connected.** Float the NC pin or connect it to AGND.
13	nFAULT	**Fault indication output.** Pull the nFAULT pin active low for fault conditions.
14	VCC	**Logic supply input for internal driver and logic.**
15	IN1	**Output 1 control input.** Pull the IN1 pin down internally.
16	IN2	**Output 2 control input.** Pull the IN2 pin down internally.
17	ISET	**Current trip voltage setting.** Connect a resistor from the ISET pin to ground.
19	AGND	**Ground for internal logic.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 36V
Supply voltage (V_{CC}) 6V
V_{OUTx} ..... -0.3V to V_{IN} + 0.3V
V_{BST1} ..... V_{OUT1} + 6V
V_{BST2} ..... V_{OUT2} + 6V
LSS voltage (V_{LSS}) ..... -0.3V to +0.6V
All other pins ..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-19 (3mmx3mm) 2.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.5V to 28V
Supply voltage (V_{CC}) ..... 2.8V (4) to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-19 (3mmx3mm)	50	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) 2.8V is the minimum VCC operating voltage when V_{CC} is falling.
5) Measured on JESD51-7, a 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
VIN operating range	V_{IN}		2.5		28	V
VCC operating range	V_{CC}	After start-up	2.8	3.3	5.5	V
V_{CC} start-up threshold (under-voltage lockout, UVLO)	V_{CC_ON}	V_{CC} rising edge	2.7	2.9	3.1	V
		V_{CC} falling edge	2.4	2.6	2.8	V
Start-up hysteretic voltage	V_{CC_HY}			0.3		V
IC Supply						
V_{CC} shutdown current	I_{VCC_SD}	EN = 0			1	µA
V_{CC} quiescent current	I_{VCC_SBY}	EN = 1, no load		1.6	2.2	mA
V_{IN} quiescent current	I_{VIN_SBY}	EN = 1, no load		210	350	µA
Logic						
Logic high threshold	V_{IH}				1.5	V
Logic low threshold	V_{IL}		0.4			V
Internal pull-down resistance	R_{PD}			500		kΩ
IC start-up delay	t_{DELAY}	EN active to switching		230	350	µs
Current Control						
Current trip voltage	V_{ITRIP}	V_{ITRIP} = 200mV	180	200	220	mV
		V_{ITRIP} = 100mV	85	100	115	mV
Off time	t_{ITRIP}	After I_{TRIP}		1		ms
Switching Frequency						
Pulse-width modulation (PWM) frequency on IN1 and IN2	f_{PWM}				400	kHz
Power MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{CC} = 3.3V, I_{OUT} = 500mA	50	78	110	mΩ
		V_{CC} = 5V, I_{OUT} = 500mA	42	65	93	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 3.3V, I_{OUT} = 500mA	50	78	110	mΩ
		V_{CC} = 5V, I_{OUT} = 500mA	42	65	93	mΩ
Minimum on time	t_{MIN_ON}			200		ns
Bootstrap (BST) for High-Side (HS) Driver						
Forward voltage for BST charge	V_{FBST}			0.5		V
BST UVLO	V_{BST_UVLO}	Rising edge		2		V
Protection						
Over-current protection (OCP) retry time	t_{OCP}			1		ms
OCP threshold	I_{OCP}		5.5	10	18.5	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

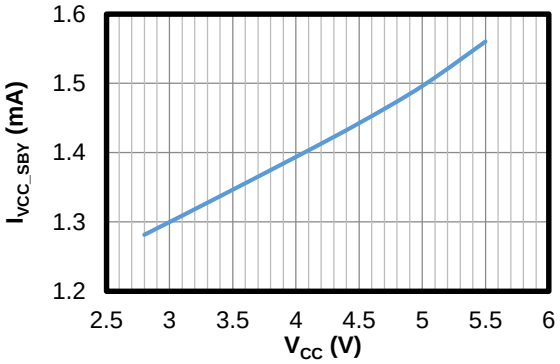
Parameters	Symbol	Condition	Min	Typ	Max	Units
V_{IN} over-voltage protection (OVP) threshold	V_{IN_OVP}		32.2	34	35.5	V
Thermal shutdown (6)	T_{SD}			150		°C
Thermal shutdown hysteresis (6)	T_{SD_HY}			20		°C

Note:

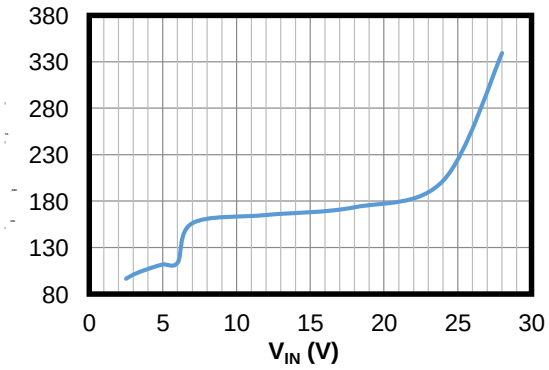
6) Not tested in production.

TYPICAL CHARACTERISTICS

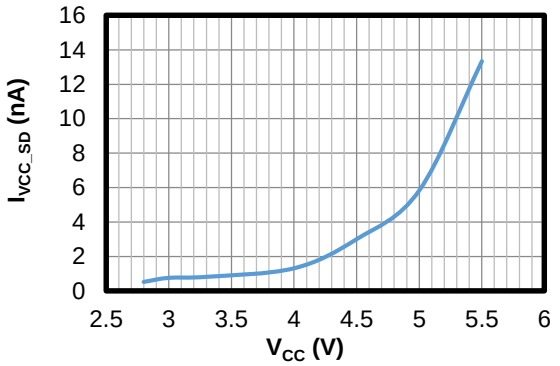
V_{CC} Quiescent Current vs. V_{CC}
EN = 1, no load



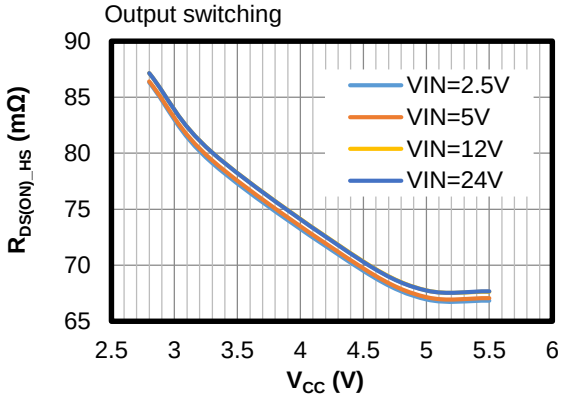
V_{IN} Quiescent Current vs. V_{IN}
EN = 1, no load



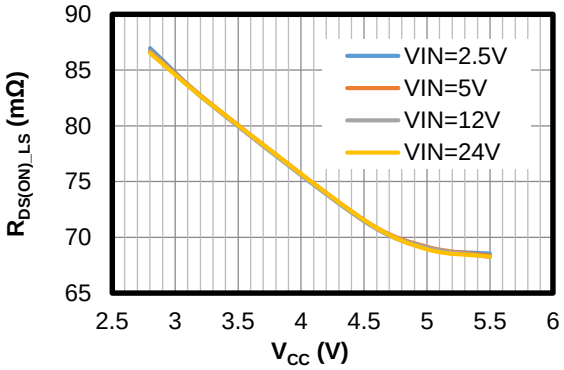
V_{CC} Shutdown Current vs. V_{CC}
EN = 0, no load



HS-FET On Resistance vs. V_{CC}
Output switching



LS-FET On Resistance vs. V_{CC}

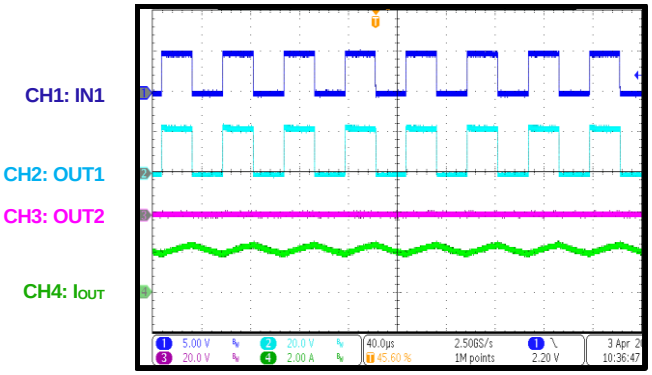


TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 5V, IN1 = 20kHz, duty = 50%, T_A = 25°C, unless otherwise noted.

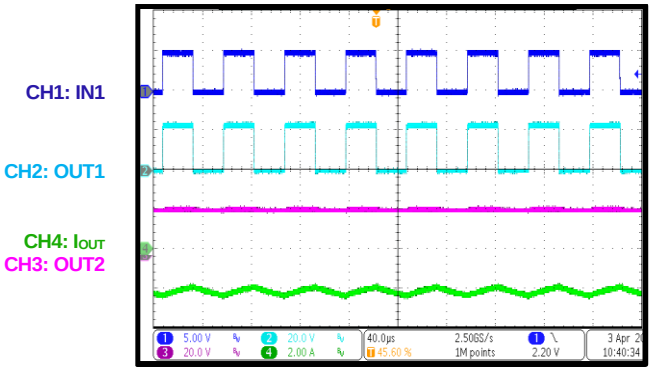
Normal Operation

V_{IN} = 24V, IN2 = low, load = 5Ω + 700μH



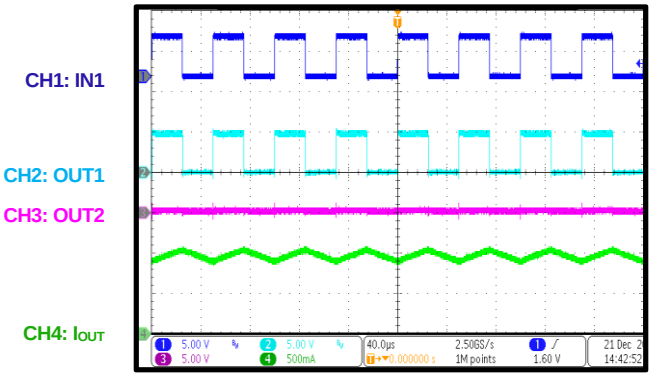
Normal Operation

V_{IN} = 24V, IN2 = high, load = 5Ω + 700μH



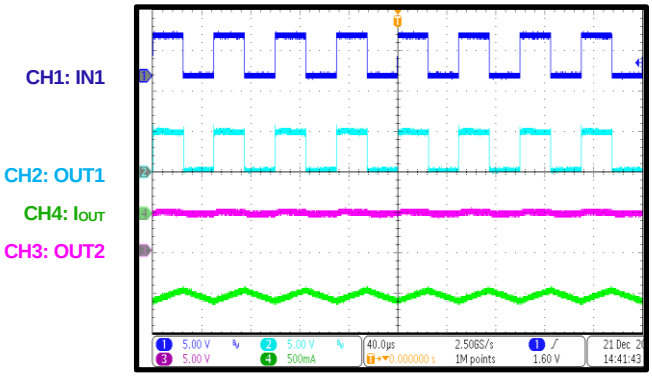
Normal Operation

V_{IN} = 5V, IN2 = low, load = 2Ω + 470μH



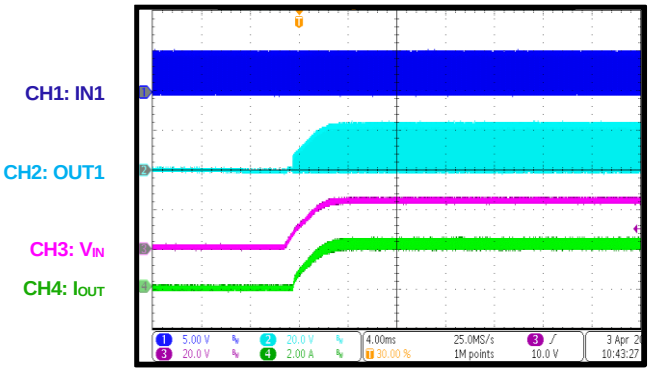
Normal Operation

V_{IN} = 5V, IN2 = high, load = 2Ω + 470μH



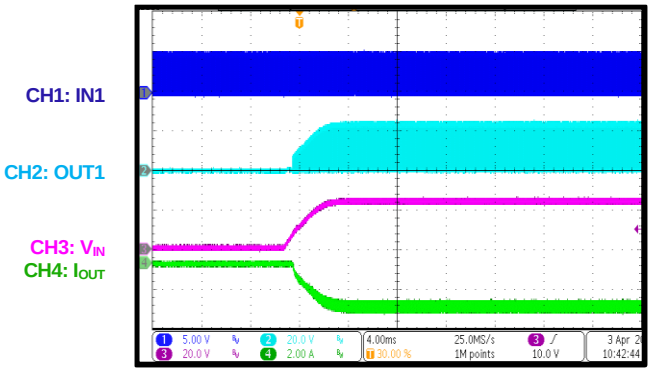
Start-Up through VIN

V_{IN} = 24V, IN2 = low, load = 5Ω + 700μH



Start-Up through VIN

V_{IN} = 24V, IN2 = high, load = 5Ω + 700μH

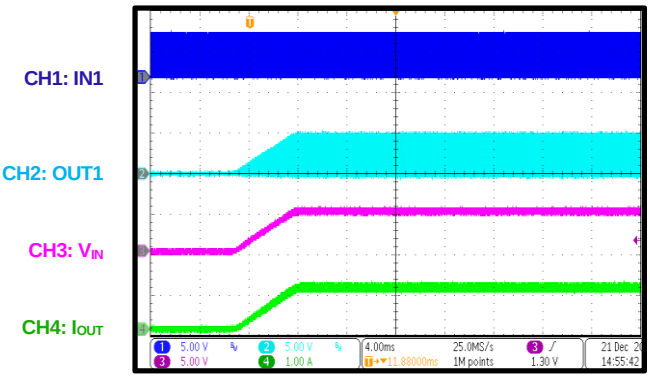


TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 5V, IN1 = 20kHz, duty = 50%, T_A = 25°C, unless otherwise noted.

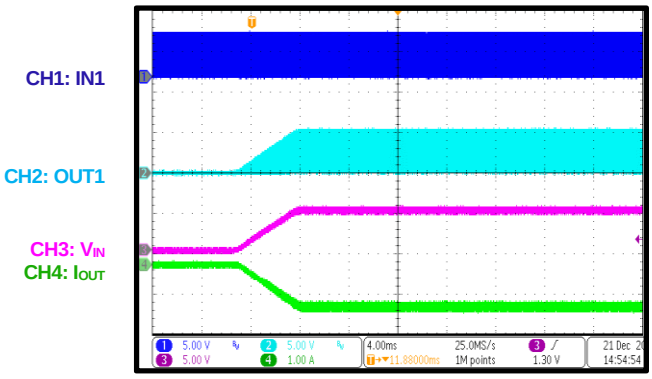
Start-Up through VIN

V_{IN} = 5V, IN2 = low, load = 2Ω + 470μH



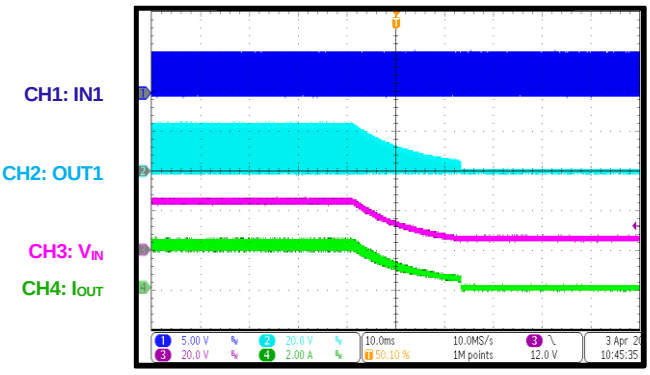
Start-Up through VIN

V_{IN} = 5V, IN2 = high, load = 2Ω + 470μH



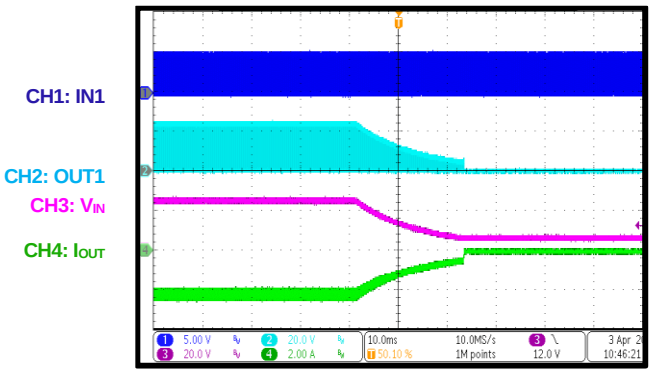
Shutdown through VIN

V_{IN} = 24V, IN2 = low, load = 5Ω + 700μH



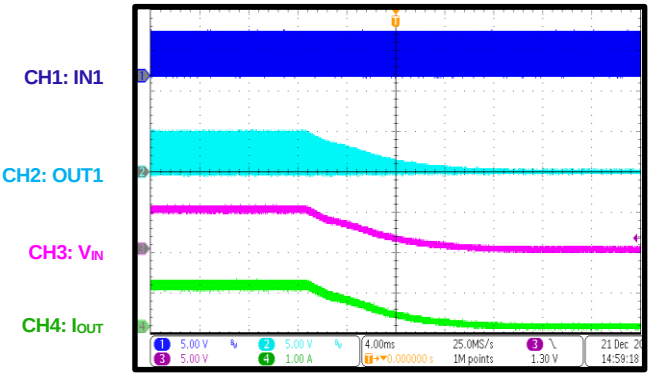
Shutdown through VIN

V_{IN} = 24V, IN2 = high, load = 5Ω + 700μH



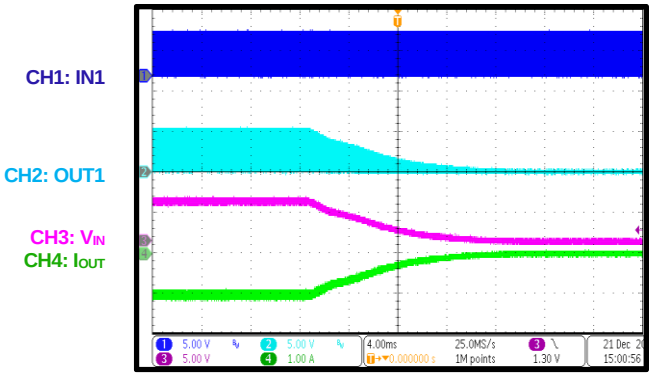
Shutdown through VIN

V_{IN} = 5V, IN2 = low, load = 2Ω + 470μH



Shutdown through VIN

V_{IN} = 5V, IN2 = high, load = 2Ω + 470μH

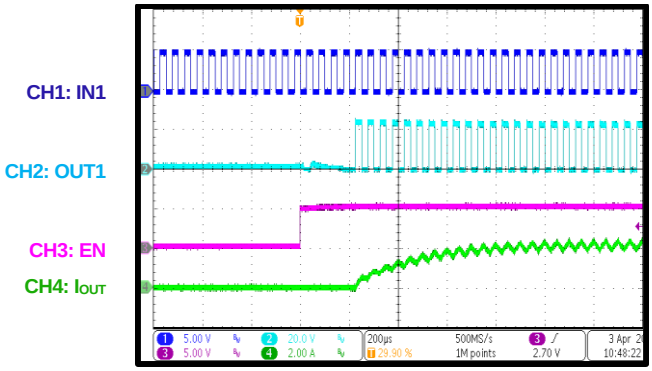


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 3.3V, EN = 5V, IN1 = 20kHz, duty = 50%, T_A = 25°C, unless otherwise noted.

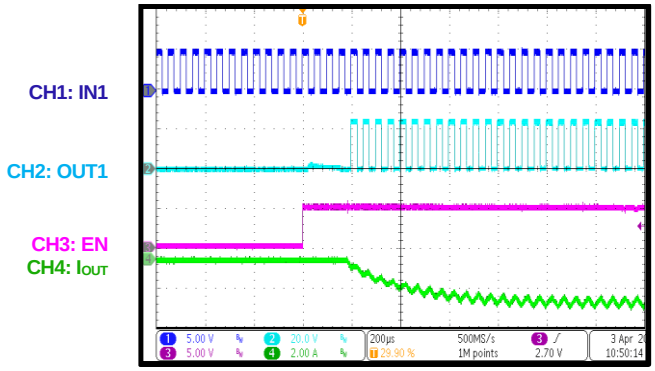
IC Enabled

V_{IN} = 24V, IN2 = low, load = 5Ω + 700μH



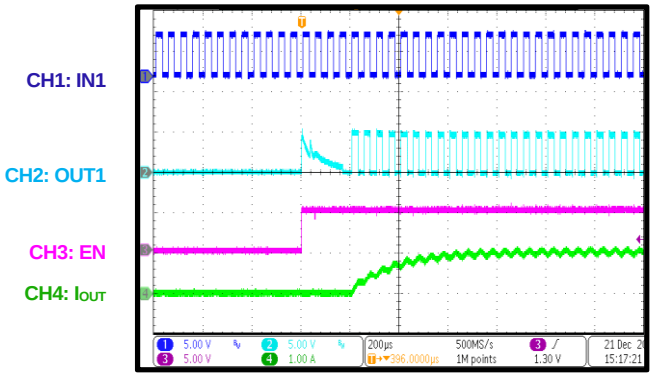
IC Enabled

V_{IN} = 24V, IN2 = high, load = 5Ω + 700μH



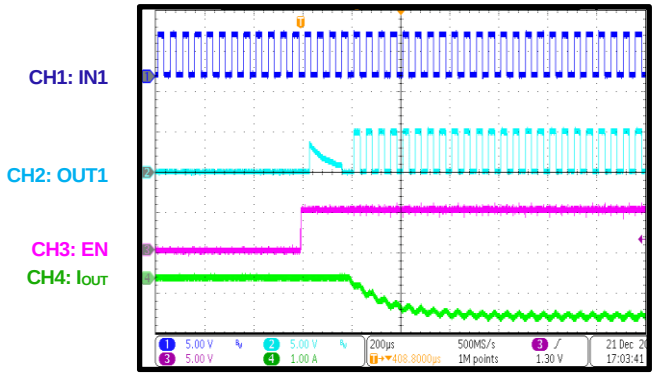
IC Enabled

V_{IN} = 5V, IN2 = low, load = 2Ω + 470μH



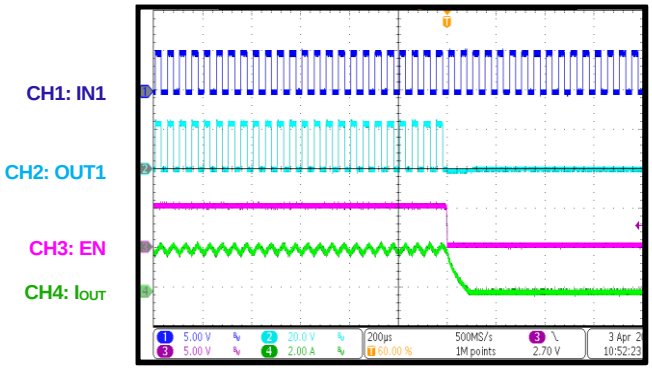
IC Enabled

V_{IN} = 5V, IN2 = high, load = 2Ω + 470μH



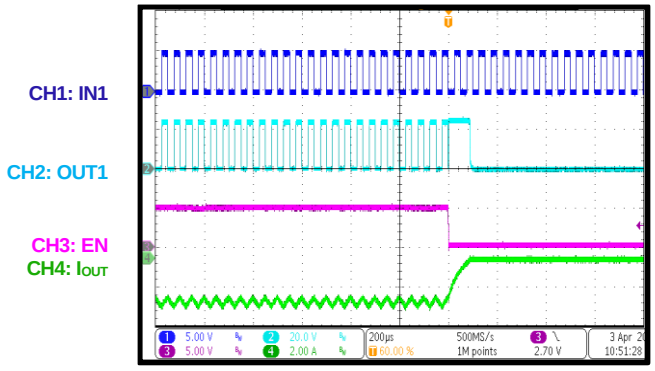
IC Disabled

V_{IN} = 24V, IN2 = low, load = 5Ω + 700μH



IC Disabled

V_{IN} = 24V, IN2 = high, load = 5Ω + 700μH

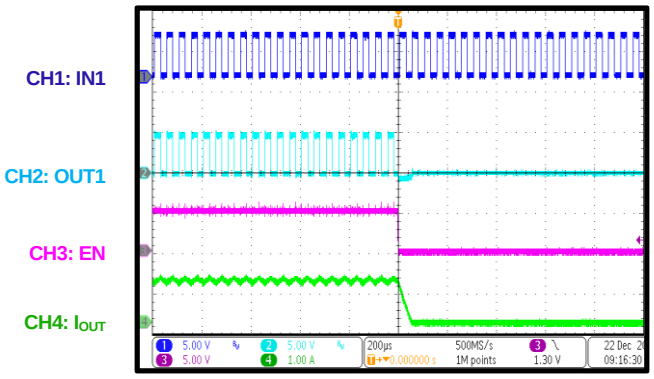


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 3.3V, EN = 5V, IN1 = 20kHz, duty = 50%, T_A = 25°C, unless otherwise noted.

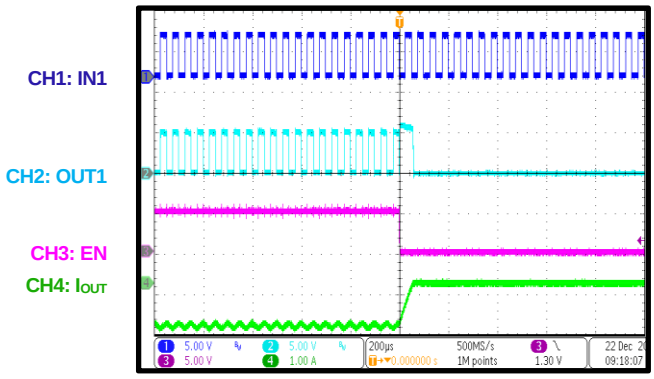
IC Disabled

V_{IN} = 5V, IN2 = low, load = 2Ω + 470μH



IC Disabled

V_{IN} = 5V, IN2 = high, load = 2Ω + 470μH



FUNCTIONAL BLOCK DIAGRAM

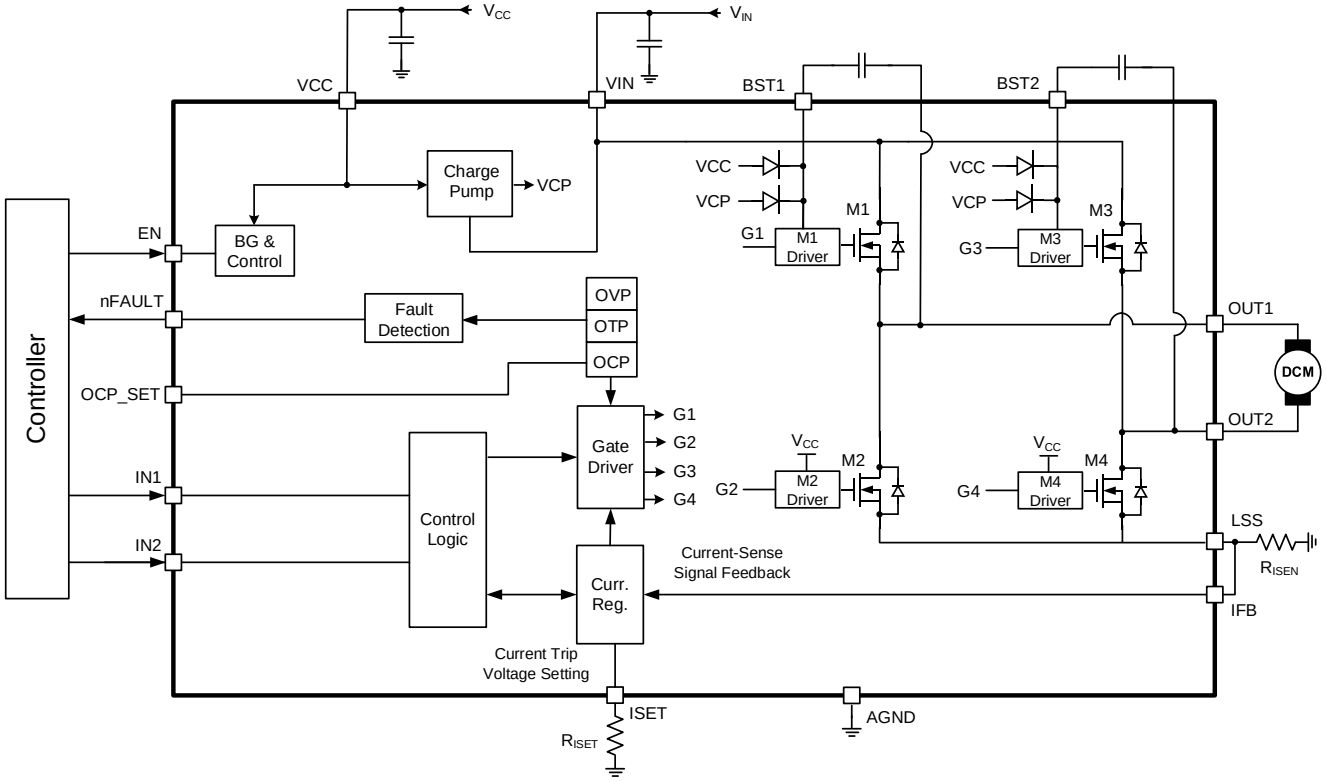


Figure 1: Functional Block Diagram

OPERATION

The MP6619L is an H-bridge motor driver that operates from a supply input voltage (V_{IN}) up to 28V and delivers a motor current up to 5A. Typically, the MP6619L drives a brushed DC motor.

Input Logic

Each of the MP6619L's half-bridges is controlled independently via the EN, IN1, and/or IN2 pins (see Table 1).

Table 1: Truth Table

EN	INx	OUTx
0	x	Z
1	0	L
1	1	H

Shutdown Mode

If the EN signal is pulled low, then the MP6619L shuts down. During shutdown, all circuits and blocks are disabled, and the MP6619L consumes below 1μA of shutdown current. There is a deglitch time of about 150ns on EN to avoid mistriggering.

Current Limit

The MP6619L has a configurable current limit. The output current (I_{OUT}) flowing through the two low-side MOSFETs (LS-FETs) is sensed by an external sense resistor. When I_{OUT} reaches the current trip threshold, a current limit condition is triggered. The entire H-bridge switches to a high-impedance state with all the MOSFETs turned off. After a fixed off time (t_{ITRIP}), the MOSFETs are re-enabled, and the cycle repeats.

The current limit is triggered when the IFB pin voltage (V_{IFB}) reaches the current trip voltage (V_{ITRIP}). For example, if a 40mΩ sense resistor is connected from the LSS pin to ground and the current trip voltage (V_{ITRIP}) is 200mV, then V_{IFB} reaches 200mV and a current trip occurs once I_{OUT} reaches 5A.

Current Trip Voltage Setting

The current control trip value is set by connecting a resistor between the ISET pin and ground. When ISET is floating, the current trip voltage is set to the default 200mV. If a resistor is connected between ISET and ground, then the current trip voltage can drop below 200mV to reduce power loss on the sense resistor. The MP6619L requires about 0.3ms to detect whether a resistor is available on ISET when the IC starts up for the first time (V_{CC} > under-voltage lockout, UVLO, and EN = 1). During this time, the IC is not switching. The relationship between the current trip voltage and ISET resistance (R_{ISET}) can be calculated using Equation (1):

$$V_{ITRIP}(V) = 0.2 \times \frac{40}{R_{ISET}(k\Omega)} \quad (1)$$

For example, if R_{ISET} is 80kΩ, the trip voltage is 100mV. For improved accuracy, a 40kΩ to 80kΩ resistance is recommended to achieve a 200mV to 100mV current trip voltage.

V_{CC} Under-Voltage Lockout (UVLO)

Whenever the VCC voltage (V_{CC}) falls below the UVLO threshold, all circuitry in the device is disabled and the internal logic resets. Once V_{CC} exceeds the UVLO threshold, the MP6619L resumes normal operation.

High-Side MOSFET (HS-FET) Driver

The two high-side MOSFETs (HS-FETs) (M1 and M3) are N-channel MOSFETs. When the HS-FETs turn on, a bootstrap (BST) supply voltage (V_{BSTx}) across BST1 and BST2 is required. V_{BSTx} is generated by a combination of the internal charge pump and V_{CC}. This allows the IC to operate at 100% duty cycle to provide sufficient driver voltage for the HS-FETs.

Over-Current Protection (OCP)

The MP6619L provides over-current protection (OCP) for each MOSFET by floating the OCP_SET pin. Pull OCP_SET logic low to disable OCP.

The OCP circuit limits the current through each MOSFET by reducing the gate driver voltage to the MOSFET. If the MOSFET current remains in the OCP condition (exceeds the OCP threshold, I_{OCP}) for longer than the OCP deglitch time, all MOSFETs in the H-bridge are disabled and nFAULT is pulled low. The driver remains disabled during the OCP retry time (t_{OCP}) and then is re-enabled automatically.

Table 2 shows the OCP setting options.

Table 2: OCP Setting

OCP_SET	Over-Current Protection
Float	Enabled
0	Disabled

Input Over-Voltage Protection (OVP)

During the freewheeling time, the energy stored in I_{OUT} is delivered to the input side. When V_{IN} and I_{OUT} are sufficiently high, the energy sent back to the input side causes V_{IN} to increase. The MP6619L employs V_{IN} protection to avoid IC damage due to a high voltage spike.

If V_{IN} exceeds the OVP threshold, the H-bridge output is disabled and nFAULT is pulled low. This protection is released once V_{IN} drops to a safe level.

Junction Over-Temperature Protection (OTP)

If the die temperature exceeds safe limits, all H-bridge MOSFETs are disabled and nFAULT is pulled low. Once the die temperature drops to a safe level, the MP6619L resumes normal operation automatically.

Fault Indication Output (nFAULT)

The MP6619L provides an nFAULT pin that is pulled active low if any of the protection circuits are activated. These fault conditions include OCP, over-temperature protection (OTP), and over-voltage protection (OVP). If a current-limit trip occurs, then nFAULT is also pulled low. nFAULT is an open-drain output and requires an external pull-up resistor. Once the fault condition is removed, nFAULT is pulled inactive high via the pull-up resistor.

Enable and Disable (EN)

To enable the MP6619L, apply a logic high signal to EN, where the high-level signal time must exceed about 10µs. To shut down the IC, pull EN logic low and set the low-level signal above 100ns.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor (C_{IN}) reduces the surge current drawn from the input supply as well as the switching noise from the device. C_{IN} impedance at the switching frequency (f_{SW}) must be below the input source impedance to prevent the high-frequency switching current from passing through to the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. A high-value capacitor is helpful for reducing V_{IN} ripple and noise. For most applications, two 22µF ceramic capacitors in parallel are sufficient. It is recommended to connect one capacitor to each VIN pin.

Setting the Output Current limit

If a resistor is connected between ISET and ground, then the output current limit (I_{OUT_LIM}) can be calculated using Equation (2):

$$I_{OUT\_LIM}(A) = 0.2 \times \frac{40}{R_{ISET}(k\Omega)} \times \frac{1}{R_{ISEN}(\Omega)} \quad (2)$$

If ISET remains floating, then I_{OUT_LIM} can be calculated using Equation (3):

$$I_{OUT\_LIM}(A) = \frac{0.2}{R_{ISEN}(\Omega)} \quad (3)$$

For example, if R_{ISET} is 80kΩ, then the trip voltage is 100mV. For improved accuracy, a 40kΩ to 80kΩ resistance is recommended to achieve a 200mV to 100mV current trip voltage.

Setting the Sense Resistor

The sensing resistor's power loss (P_{LOSS_RIFB}) can be calculated using Equation (4):

$$P_{LOSS\_RIFB}(W) = \frac{V_{ITRIP}{}^2(V)}{R_{ISEN}(\Omega)} \quad (4)$$

To guarantee a current reference, the sensing resistor's nominal power rating is recommended to be two times the calculated power loss with at least a 1% accuracy resistor.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 2 and follow the guidelines below:

1. Place the input bypass capacitor as close as possible to the VIN, VCC, and GND pins.
2. Use a wide copper plane for the input, output, and ground connection to improve thermal performance.
3. Place as many GND vias near the output capacitor (C_{OUT}) and C_{IN} as possible to improve thermal performance.
4. Keep the sense resistor loop as short as possible.
5. Keep the current-sense feedback signal far away from noise sources.

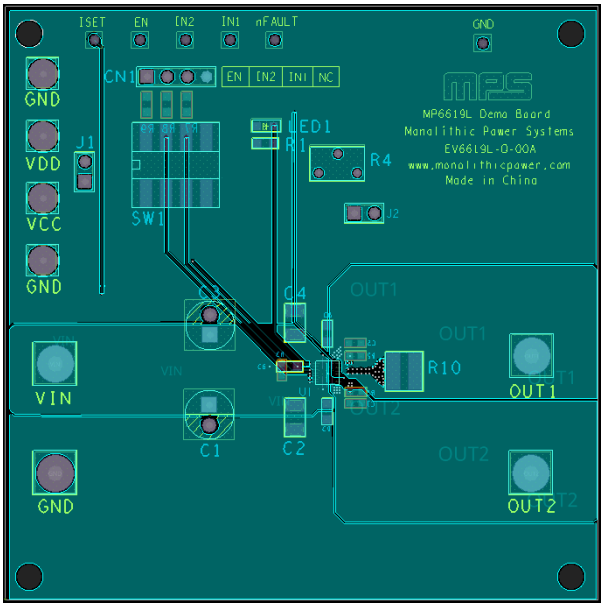


Figure 2: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

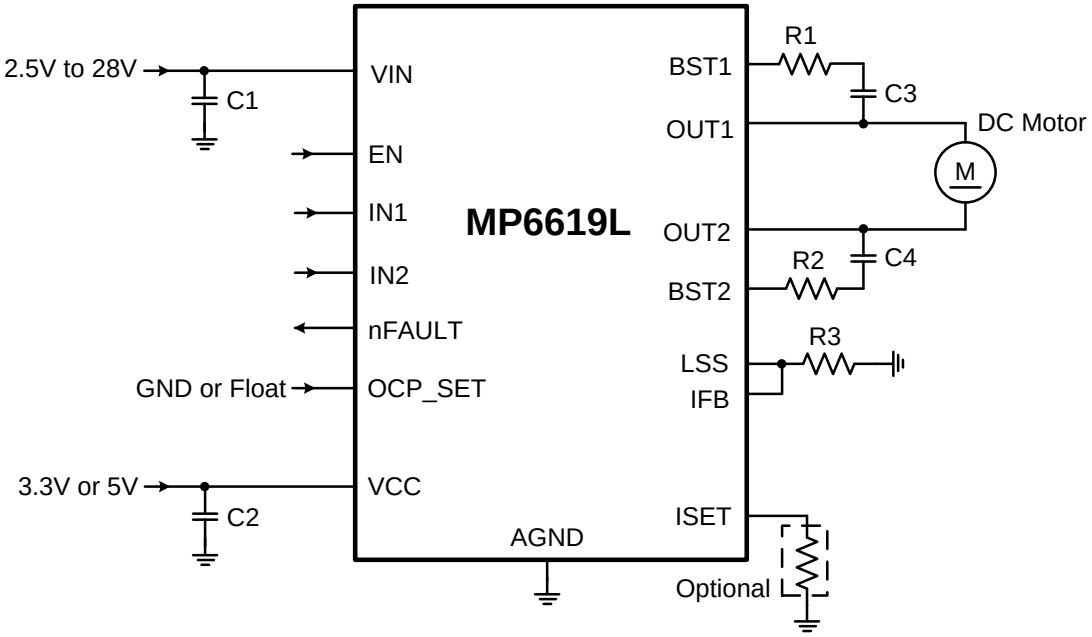
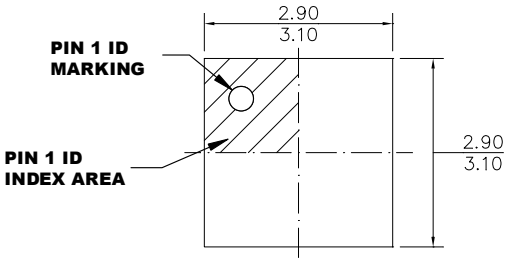


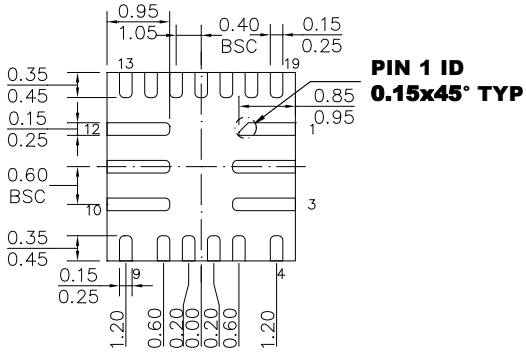
Figure 3: Typical Application Circuit

PACKAGE INFORMATION

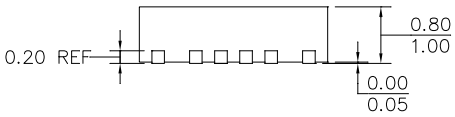
QFN-19 (3mmx3mm)



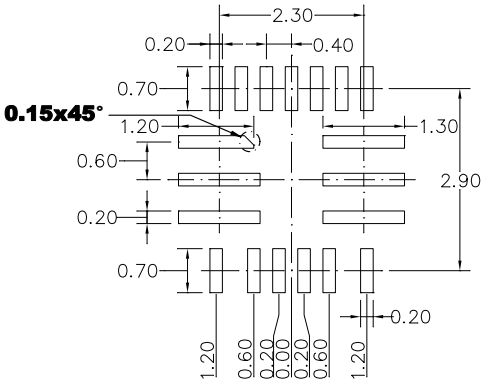
TOP VIEW



BOTTOM VIEW



SIDE VIEW

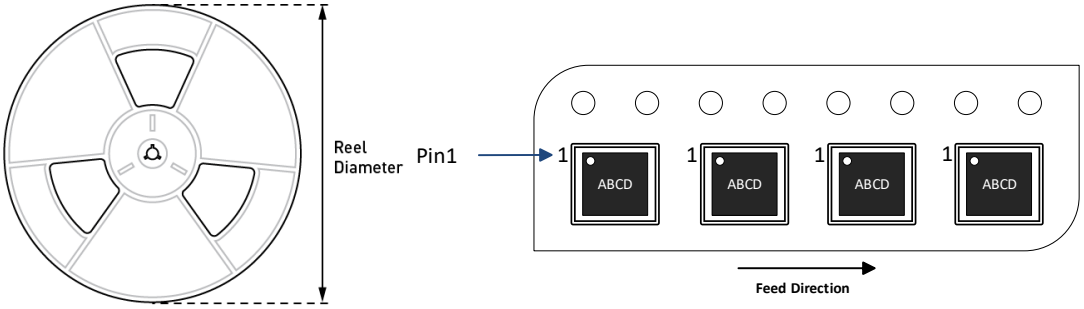


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PINS 2, 3, 10, 11, AND 12 HAVE THE SAME SHAPE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6619LGQ-Z	QFN-19 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/20/2022	Initial Release	-