MAX96717R

CSI-2 to GMSL2 Serializer

General Description

The MAX96717R GMSL™ serializer receives video on a 4-lane MIPI CSI-2 interface and outputs it on a GMSL2 serial link transceiver for transport over a coaxial cable. Simultaneously, it sends and receives bidirectional control channel data across the same GMSL2 link. The GMSL2 link operates at a fixed rate of 3Gbps in the forward direction and 187.5Mbps in the reverse direction. The device is programmed through a local I^2C interface or across the link from a matching deserializer. The MAX96717R features flexible GPIO tunnels and register-programmed GPIO. Operation is specified over the automotive temperature range of -40°C to +105°C. The device is AEC-Q100 grade 2 qualified.

Data can be transported over low-cost 50Ω coax cables that meet the GMSL2 channel specification. Table 1 provides guidance to typical maximum lengths of commonly used automotive cables. Contact the factory for the GMSL2 Channel Specification.

Table 1. **Typical Maximum Cable Length vs. Attenuation**

	3.2mm Ø 50Ω Coax, Foam Dielectric	**2.7mm Ø 50Ω Coax, Solid Dielectric**
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m
Attenuation at 3GHz (Max, Aged, +105°C)	1.1dB/m	2.0dB/m
GMSL Fwd/Rev Data Rate	**Typical Maximum Cable Length at +105ºC**	
3Gbps/187.5Mbps	20m	10m

Applications

- Advanced Driver Assistance Systems (ADAS)
- Surround View Systems (SVS)
- Driver Monitor Systems (DMS)
- Rear View Camera (RVC)
- Systems with Multiple Synchronized Cameras

Benefits and Features

- Automotive-Grade High-Speed Link
  - Supports 19dB Insertion Loss at 1.5GHz
  - Auto Adapt for Changes in Channel Conditions
  - Operates -40°C to +105°C Ambient
- Four-Lane MIPI CSI-2 v1.3 Input Port
  - MIPI D-PHY v1.2 Rated at 600Mbps/Lane
  - Polarity Flip and Data-Lane Reassignment
  - Supports 4 Virtual Channels
- Single GMSL2 Output
  - 3Gbps in GMSL2 Forward Link-Rate
  - 187.5Mbps Reverse Link-Rate
- Bidirectional Control Channel Supports
  - Seven Configurable GPIO
  - 1 x I^2C Port, up to 1MHz
- Reduce BOM and Space Savings
  - Tiny, 5mm x 5mm TQFN
  - Industry's Smallest Power over Coax (PoC)

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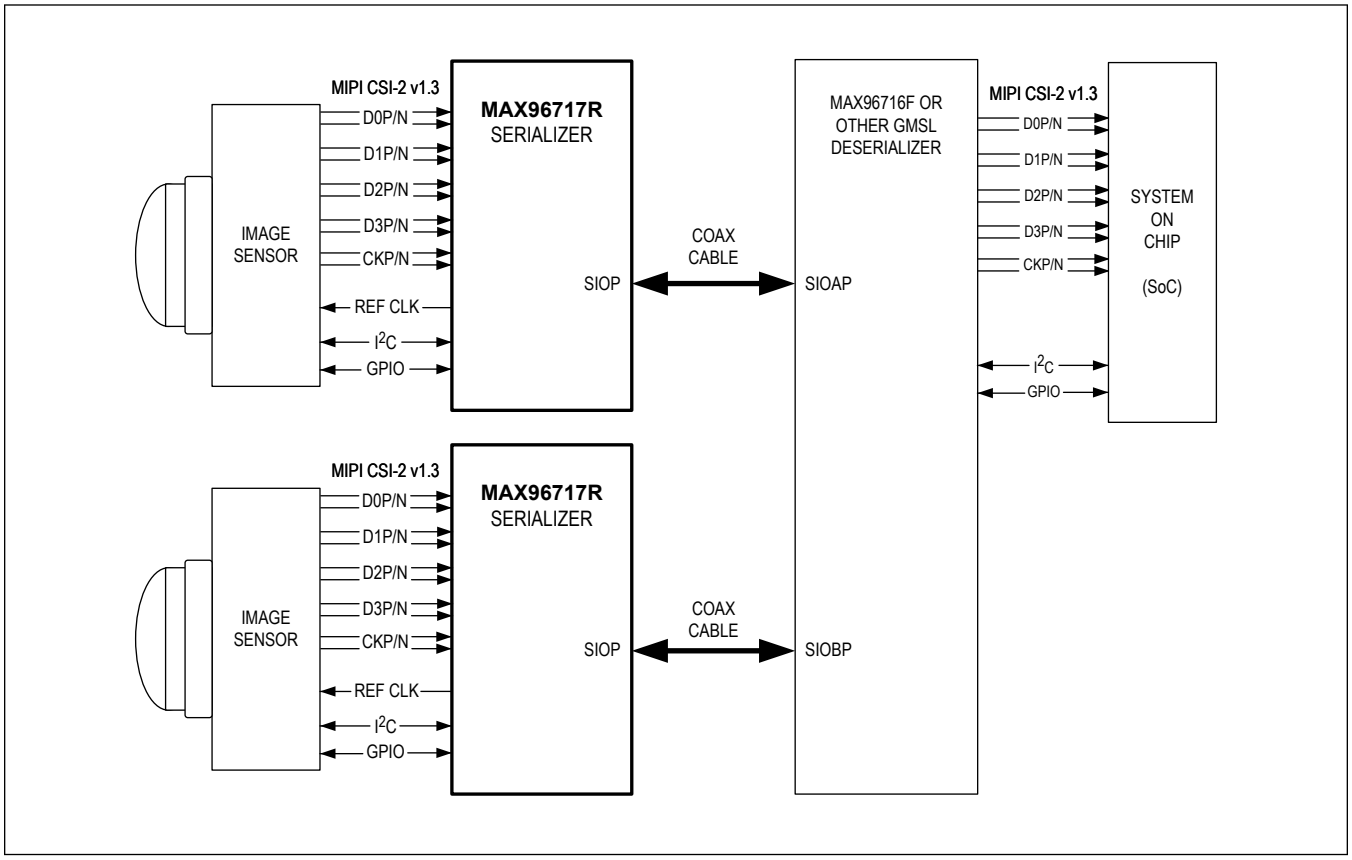
***Ordering Information** appears at end of data sheet.*

19-101157; Rev 1; 3/23

Simplified Application Circuit



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Absolute Maximum Ratings

(All voltages with respect to ground) .....
V_{DD18} ..... -0.3V to +2.0V
V_{DD} ..... -0.3V to +2.0V
CAP_VDD ..... 0.3V to +1.2V
SIO_(Active State) (Note A) ..... -0.3V to (CAP_VDD + 0.3V)
SIO_(Inactive State) (Note A)..... -0.3V to (CAP_VDD + 0.3V)
D_P/N, CKP/N ..... -0.3V to +1.35V
XRES, X2 ..... -0.3V to (V_{DD18} + 0.3V)
All Other Pins ..... -0.3V to (V_{DD18} + 0.3V)
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note A: Active state means the device is powered-up and not in a power-down mode. Inactive means the device is not powered-up or powered-up in power-down mode.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN

Package Code	T3255+8
Outline Number	21-0140
Land Pattern Number	90-0013
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

For the latest package outline information and land patterns (footprints), go to *www.analog.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board in still air. For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.26V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD-CHANNEL SERIAL INPUTS/OUTPUTS (SIOP, SION)—SEE Figure 1						
Output-Voltage Swing (Single-Ended)	V_O	R_L = 100Ω ±1%, (V_{OH} - V_{OL}) for both outputs	300	400	500	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1%, offset voltage in each output state	0.4	0.5	0.6	V
Termination Resistance (Internal)	R_O	Any pin to V_{DD18}	45	50	55	Ω
DC ELECTRICAL CHARACTERISTICS / D-PHY HS RECEIVER						
Common-Mode Voltage HS Receive Mode	$V_{CMRX(DC)}$		70		330	mV
Differential Input High Threshold	V_{IDTH}				40	mV
Differential Input Low Threshold	V_{IDTL}		-40			mV
Single-Ended Input High Voltage	V_{IHHS}				460	mV
Single-Ended Input Low Voltage	V_{ILHS}		-40			mV
Single-Ended Threshold for HS Termination Enable	$V_{TERM-EN}$				450	mV
Differential Input Impedance	Z_{ID}		80	100	125	Ω
DC ELECTRICAL CHARACTERISTICS / I/O PINS (GPIO)						
High-Level Input Voltage	V_{IH}		0.7 x V_{DD18}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DD18}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DD18} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	V_{IN} = 0 to V_{DD18}. All pullup/pulldown devices disabled.			1	µA
Input Capacitance	C_{IN}	Each pin		5		pF
Input Pullup/Pulldown Resistance	R_{IN}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH2}		0.7 x V_{DD18}			V
Low-Level Input Voltage	V_{IL2}				0.3 x V_{DD18}	V

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.26V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA				0.4	V
Input Current	I_{IN}	V_{IN} = 0 to V_{DD18}. All pullup/pulldown devices disabled.				1	µA
Input Capacitance	C_{IN}	Each pin			3		pF
Internal Pullup Resistor	R_{PU}	40kΩ enabled			40		kΩ
		1MΩ enabled			1		MΩ
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT							
High-Level Input Voltage	V_{IH}			0.7 x V_{DD18}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{DD18}	V
Input Current	I_{IN}	V_{IN} = 0 to V_{DD18}				6	µA
Input Capacitance	C_{IN}				3		pF
Internal Pulldown Resistor	R_{PD}				1		MΩ
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS (GPIO)							
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA		V_{DD18} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA				0.4	V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (CRYSTAL) (X1, X2)							
X1 Input Capacitance	C_{IN_X1}				3		pF
X2 Input Capacitance	C_{IN_X2}				1		pF
Internal X2 Limit Resistor	R_{LIM}				1.2		kΩ
Internal Feedback Resistor	R_{FB}				10		kΩ
Transconductance	g_m				28		mA/V
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENTS							
Supply Current (*Note 3*)	I_{DD}	RGB888, 3Gbps, 4-lane CSI-2 input, 600Mbps per lane	V_{DD18} = 1.9V		46	53	mA
			V_{DD} = 1.05V		74	228	
			V_{DD} = 1.26V		74	238	
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT							
Maximum Power-Down Current	I_{DD}	V_{DD18} at 1.9V	T_A = +25ºC		10		µA
			T_A = +105ºC		10		
		V_{DD} at 1.26V	T_A = +25ºC		3		
			T_A = +105ºC		48		
AC ELECTRICAL CHARACTERISTICS / FORWARD CHANNEL SWITCHING CHARACTERISTICS							
Serial-Output Rise Time	t_R	20% to 80%, V_{OD} = 800mV differential, R_L = 100Ω, 500mV single-ended R_L = 50Ω			50		ps

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.26V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Serial-Output Fall Time	t_F	80% to 20%, V_{OD} = 800mV differential, R_L = 100Ω, 400mV single-ended R_L = 50Ω			50		ps
Total Serial-Output Jitter	t_{TSOJ}	PRBS7, single-ended or differential			0.15		UI (p-p)
Deterministic Serial-Output Jitter	t_{DSOJ}	PRBS7, single-ended or differential			0.10		UI (p-p)
Lock Time	t_{LOCK}	Time from deassertion of PWDNB until LOCK = '1'. See Figure 17.			45		ms
Maximum Video Latency	t_{VL}	Time from CSI-2 input to SIO± output in GMSL2 packet. See Figure 4	Pixel mode		120 x t_{PCLK}		s
			Tunneling mode 3G		30 x t_{PCLK} + 2µs		
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the device.			1		ms
GPI-to-GPO Delay	t_{GPD1}	Delay compensated mode.			10		µs
	t_{GPD2}	Non-delay compensated mode.			3		
GPI-GPO Skew Reverse Path	t_{SKEW}	Delay compensated mode.			7		ns
AC ELECTRICAL CHARACTERISTICS / D-PHY HS RECEIVER							
Common-Mode Interference Beyond 450MHz	$\Delta V_{CMRX(HF)}$	*Note 2*, *Note 5*, *Note 7*	Data rate > 1.5Gbps			50	mV
Common-Mode Interference 50MHz–450MHz	$\Delta V_{CMRX(LF)}$	*Note 2*, *Note 5*, *Note 6*	Data rate > 1.5Gbps	-25		25	mV
Common-Mode Reflection Coefficient	Scc_{RX}	450MHz < f < 1.875GHz			-5		dB
Differential-Mode Reflection Coefficient	Sdd_{RX}	f < 20MHz			-22.5		dB
		f = 1.25GHz			-12		
		f = 1.875GHz			-9.7		
AC ELECTRICAL CHARACTERISTICS / D-PHY LP RECEIVER—SEE Figure 5 (*Note 2*)							
Input Pulse Rejection	e_{SPIKE}	See Figure 5				300	V*ps
Minimum Pulse Width Response	t_{MIN-RX}	See Figure 5		20			ns
Peak Interference Amplitude	V_{INT}					200	mV
Interference Frequency	f_{INT}			450			MHz
AC ELECTRICAL CHARACTERISTICS / D-PHY DATA CLOCK TIMING—SEE Figure 6 (*Note 2*)							
UI Variation	ΔUI	UI ≥ 1ns, within a single burst		-10%		+10%	UI
		0.667ns < UI < 1ns, within a single burst		-5%		5%	
Data to Clock Setup Time	$t_{SETUP[RX]}$	< 1.0Gbps		0.15			UI_{INST}
		> 1.0Gbps		0.2			

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.26V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data to Clock Hold Time	$t_{HOLD[RX]}$	< 1.0Gbps	0.15			UI_{INST}
		> 1.0Gbps	0.2			
AC ELECTRICAL CHARACTERISTICS / D-PHY GLOBAL OPERATION TIMING (*Note 2*)						
Time Interval When the HS Receiver Ignores Any Clock Lane HS Transitions, Starting from the Beginning of $T_{CLK-PREPARE}$.	$t_{CLK-SETTLE}$	See Figure 9	95		300	ns
Time for the Clock Lane Receiver to Enable the HS Line Termination, Starting from the Time Point When Dn Crosses $V_{IL,MAX}$.	$t_{CLK-TERM-EN}$	See Figure 9	Time for Dn to reach $V_{TERM-EN}$		38	ns
Time for the Data Lane Receiver to Enable the HS Line Termination, Starting from the Time Point When Dn Crosses $V_{IL,MAX}$.	$t_{D-TERM-EN}$	See Figure 7 and Figure 8	Time for Dn to reach $V_{TERM-EN}$		35ns + 4*UI	ns
Time Interval When the HS Receiver Ignores Any Data Lane HS Transitions, Starting from the Beginning of $T_{HS-PREPARE}$.	$t_{HS-SETTLE}$	See Figure 7 and Figure 8	85 + 6*UI		145 + 10*UI	ns
AC ELECTRICAL CHARACTERISTICS / I^2C PORT TIMING—SEE Figure 3						
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DD18}, (*Note 2*)	20 x V_{DD18}/5.5V		150	ns
I^2C Wake Time		From power-up or rising edge of PWDNB to local register access. For remote register access, I^2C wake time is the same as lock time (t_{LOCK}).		1.1		ms
AC ELECTRICAL CHARACTERISTICS / I^2C TIMING—SEE Figure 3						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range : (I2CMSTBT = 010, I2CSLVSH = 10)	9.6		100	kHz
		Mid f_{SCL} range : (I2CMSTBT = 101, I2CSLVSH = 01)	100		400	
		High f_{SCL} range : (I2CMSTBT = 111, I2CSLVSH = 00)	400		1000	
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, Low	4			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.26V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, Low	4.7			µs
		f_{SCL} range, Mid	1.3			
		f_{SCL} range, High	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, Low	4			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, Low	4.7			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, Low	0			ns
		f_{SCL} range, Mid	0			
		f_{SCL} range, High	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, Low	250			ns
		f_{SCL} range, Mid	100			
		f_{SCL} range, High	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, Low	4			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, Low	4.7			µs
		f_{SCL} range, Mid	1.3			
		f_{SCL} range, High	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, Low			3.45	µs
		f_{SCL} range, Mid			0.9	
		f_{SCL} range, High			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, Low			3.45	µs
		f_{SCL} range, Mid			0.9	
		f_{SCL} range, High			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, Low			50	ns
		f_{SCL} range, Mid			50	
		f_{SCL} range, High			50	
Capacitive Load on Each Bus Line	C_B				100	pF
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT REQUIREMENTS (CRYSTAL) (X1,X2) (*Note 2*)						
Frequency		Fundamental mode only		25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK OUTPUT (RCLKOUT)						
Frequency	f_{REF}	Crystal or reference clock input.		25		MHz

Electrical Characteristics (continued)

(V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.26V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{DD18} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time	t_R	20% to 80%, C_L = 10pF, 12.5MHz (25MHz divided by 2), (*Note 4*)		2		ns
Fall Time	t_F	80% to 20%, CL = 10pF, 12.5MHz (25MHz divided by 2), (*Note 4*)		2		ns
Jitter	t_J	C_L = 10pF, Rising or falling edge, 12.5MHz (25MHz divided by 2)		100		ps (p-p)

Note 1: Limits are 100% tested at T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: Color bar pattern. Maximum supply currents are measured at indicated supply voltages. Typical supply currents are measured at the typical supply voltages.

Note 4: MFP pin speed programmed to fastest setting. See the *Multifunction Pin Assignments* section.

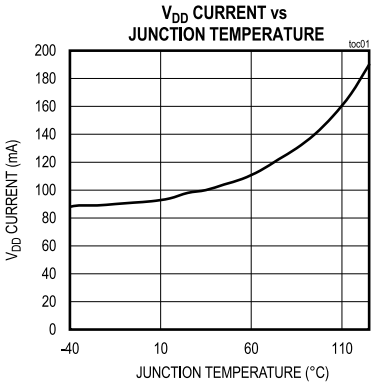
Note 5: Excluding static ground shift of 50mV.

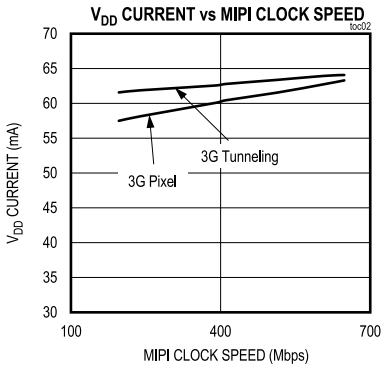
Note 6: Voltage difference compared to the DC average common-point potential.

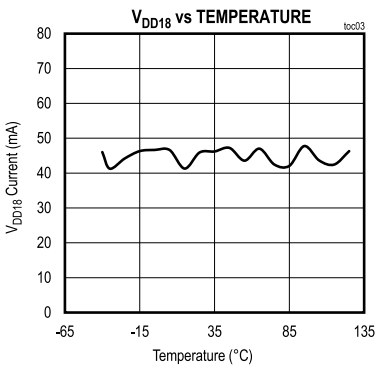
Note 7: $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

Typical Operating Characteristics

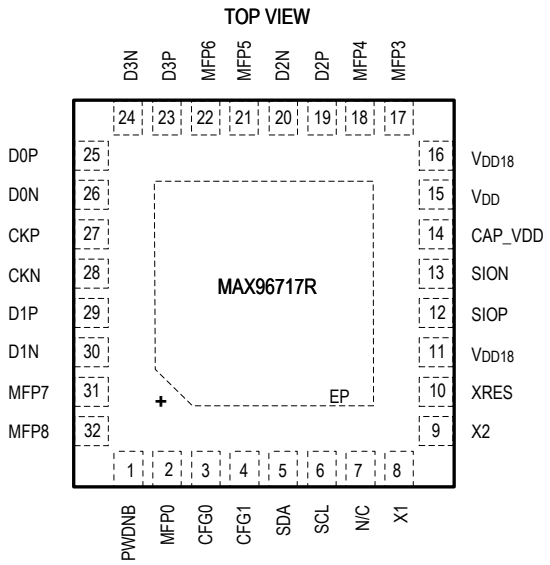
(V_{DD18} = 1.8V, V_{DD} = 1.0V, T_A = +25°C unless otherwise noted. 3Gbps forward rate, 187.5Mbps reverse rate, PRBS24 data, 600Mbps per lane on 4 lanes DPHY.)







Pin Configuration



TQFN
5mm x 5mm

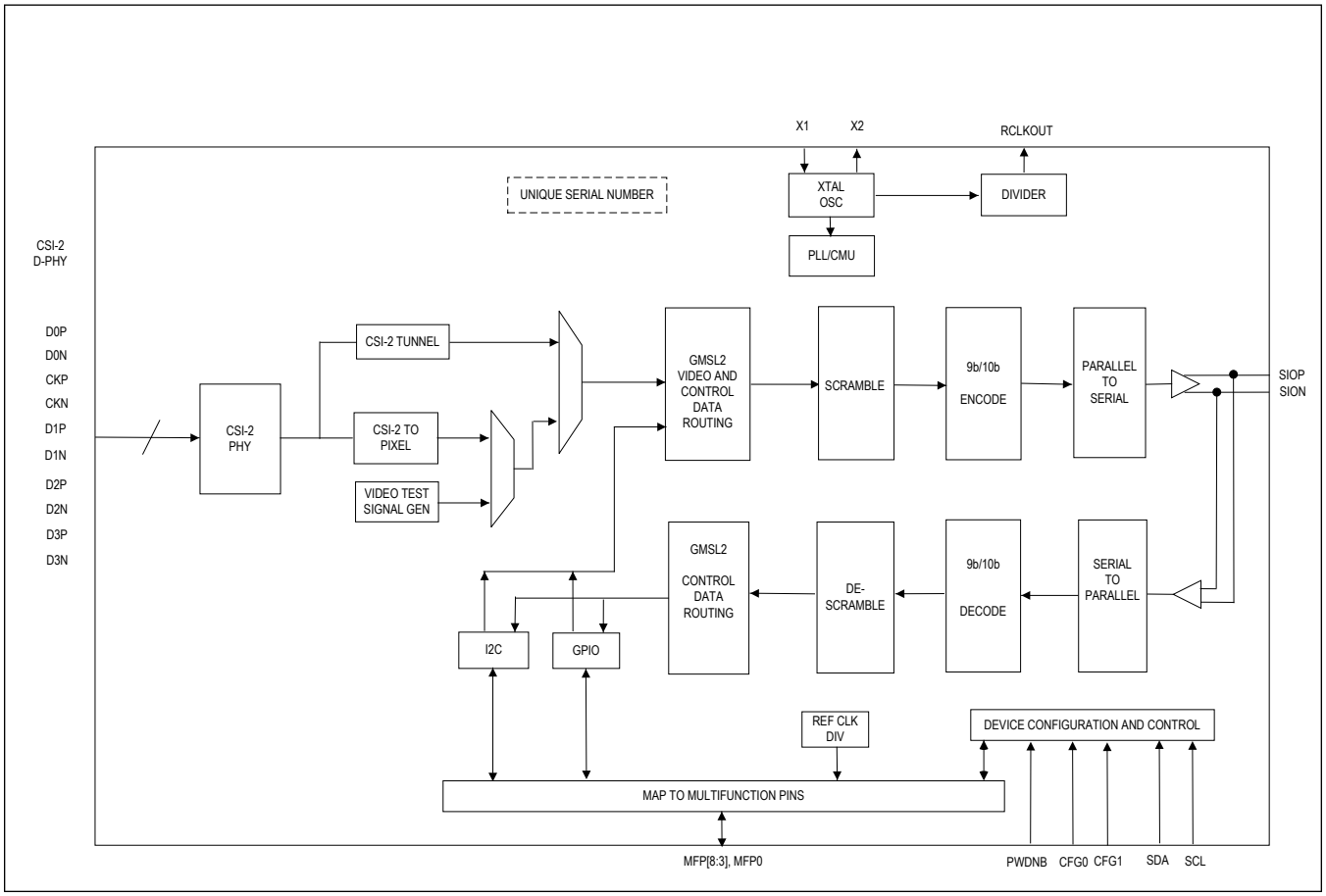
Pin Descriptions

PIN	NAME	FUNCTION MODE	FUNCTION
		GMSL2	
GMSL2 SERIAL LINK			
12	SIOP	SIOP	Coax Serial-Data Input/Output.
13	SION	SION	Inverted Serial-Data Input/Output. Terminate with 100nF in series with 50Ω to ground
CSI-2 INTERFACE			
19	D2P	D2P	CSI-2 Data Lane 2 Noninverted Input. Leave open if unused.
20	D2N	D2N	CSI-2 Data Lane 2 Inverted Input. Leave open if unused.
23	D3P	D3P	CSI-2 Data Lane 3 Noninverted Input. Leave open if unused.
24	D3N	D3N	CSI-2 Data Lane 3 Inverted Input. Leave open if unused.
25	D0P	D0P	CSI-2 Data Lane 0 Noninverted Input. Leave open if unused.
26	D0N	D0N	CSI-2 Data Lane 0 Inverted Input. Leave open if unused.
27	CKP	CKP	CSI-2 Clock Lane Noninverted Input.
28	CKN	CKN	CSI-2 Clock Lane Inverted Input.
29	D1P	D1P	CSI-2 Data Lane 1 Noninverted Input. Leave open if unused.

PIN	NAME	FUNCTION MODE	FUNCTION
		GMSL2	
30	D1N	D1N	CSI-2 Data Lane 1 Inverted Input. Leave open if unused.
MULTIFUNCTION, I²C AND CONFIG PINS (*) INDICATES DEFAULT STATE AFTER POWER-UP (LEAVE OPEN IF NOT USED)			
2	MFP0	GPIO0* VTG0	GPIO0: Configurable General-Purpose Input or Output. Power-up default is high impedance, disabled, with a 1MΩ pulldown resistor. VTG0: Selectable Video Timing Generator Output for VS, HS or PCLK
3	CFG0	CFG0	CFG0: Configuration Pin. Voltage at pin sets device modes, which are latched at power-up. Connect to a resistor divider between V_{DD18} and ground. See Table 7.
4	CFG1	CFG1	CFG1: Configuration Pin. Voltage at pin sets device modes, which are latched at power-up. Connect to a resistor divider between V_{DD18} and ground. See Table 8.
17	MFP3	GPIO3* LOCK ERRB VTG3	GPIO3: Configurable General-Purpose Input or Output. Power-up default is high impedance with a 1MΩ pulldown resistor. LOCK: High Indicates PLLs Locked with Correct Serial Word Boundary Alignment. ERRB: Error Output. Goes low when an error is detected. VTG3: Selectable Video Timing Generator Output for VS, HS or PCLK
18	MFP4	GPIO4* RCLKOUT VTG4	GPIO4: Configurable General-Purpose Input or Output. Power-up default is high impedance with a 1MΩ pulldown resistor. RCLKOUT: 25MHz Frequency Reference Output. Divide by 2 or 4 available. VTG4: Selectable Video Timing Generator Output for VS, HS or PCLK
21	MFP5	ODO5_GPI5	ODO5_GPI5: Configurable General-Purpose Input or Open-Drain Output. Power-up default is high impedance with a 1MΩ pulldown resistor.
22	MFP6	ODO6_GPI6	ODO6_GPI6: Configurable General-Purpose Input or Open-Drain Output. Power-up default is high impedance with a 1MΩ pulldown resistor.
31	MFP7	GPIO7* VTG7	GPIO7: Configurable General-Purpose Input or Output. Power-up default is as a GPI with a 1MΩ pulldown resistor. VTG7: Selectable Video Timing Generator Output for VS, HS or PCLK.
32	MFP8	GPIO8* ERRB (Alt) VTG8	GPIO8: Configurable General-Purpose Input or Output with an Internal 40kΩ Pullup to V_{DD18}. Power-up default is GPIO with logic high. ERRB (Alternate): Error Output. Goes low when a CSI-2 ECC or checksum error is detected. VTG8: Selectable Video Timing Generator Output for VS, HS or PCLK
5	SDA	SDA	SDA: I²C Serial-Data Input/Open-Drain Output. Internal 40kΩ pullup to V_{DD18}.
6	SCL	SCL	SCL: I²C Serial-Clock Input/Open-Drain Output. Internal 40kΩ pullup to V_{DD18}.
POWER SUPPLIES—SEE Table 3 FOR DECOUPLING CAPACITOR RECOMMENDATIONS			
11, 16	V_{DD18}	V_{DD18}	1.8V Analog Supply.
14	CAP_VDD	CAP_VDD	Decoupling Capacitor Pin for 1V Core Supply.

PIN	NAME	FUNCTION MODE	FUNCTION
		GMSL2	
15	V_{DD}	V_{DD}	Digital Core Supply. Connect a 1.0V to 1.2V supply.
EP	EP	EP	Exposed Pad. EP is the ground connection to the device. EP MUST be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.
MISCELLANEOUS—SEE Table 3 FOR EXTERNAL COMPONENTS			
1	PWDNB	PWDNB	PWDNB: Active-Low Power-Down Input with a 1MΩ Pulldown to Ground. Set PWDNB low to enter power-down mode.
7	N/C	N/C	No Connect. Internally connected. Leave open.
8	X1	X1	Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal and connect a load capacitor from X1 to EP (load capacitor value depends on the crystal used).
9	X2	X2	Crystal Input. Connect to one terminal of a 25MHz ±200ppm crystal and connect a load capacitor from X2 to EP (load capacitor value depends on crystal used).
10	XRES	XRES	Used to Calibrate SIO Output Driver Swings. Connect a 402Ω ±1% resistor between XRES and Ground (EP).

Functional Diagrams



Detailed Description

Additional Documentation

In addition to the provided information, designers must also use the following information to correctly design systems using the MAX96717R.

- GMSL2 Channel Specification
- GMSL2 Hardware Design Guide
- GMSL2 User Guide
- Device Errata

The Channel Specification contains physical layer requirements for the PCB traces, cables, and connectors that constitute the GMSL link. The Hardware Design Guide contains recommendations for PCB design, applications circuits, selection of external components, and guidelines for use of GMSL signal integrity tools. The User Guide contains detailed programming guidelines for GMSL device features. Errata sheets contain deviations from published device specifications, and are specific to part number and revision ID. Contact the factory for these documents.

Recommended Operating Conditions

Table 2. Recommended Operating Conditions

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Voltage Range	V_{DD18}		1.7	1.8	1.9	V
	V_{DD}		0.95		1.26	
Maximum Supply Noise	V_{DD}	1.0V		25		mV_{P-P}
		1.1V		37.5		
		1.2V		50		
	V_{DD18}			25		
Operating Junction Temperature, T_J			-40		+125	°C

Note: Supply noise < 1MHz. Supply voltage ripple is assumed to be symmetric around the measured DC supply voltage. For example, $25mV_{P-P}$ means ±12.5mV peak voltage.

External Component Requirements

Table 3 details critical components that must be connected to the specified pins for correct operation.

Table 3. External Component Requirements

COMPONENT	SYMBOL	CONDITION	VALUE	UNIT
XRES	R_{XRES}	Connect R_{XRES} resistor between XRES pin and ground. Total variation not to exceed ±3% including tolerance, temperature, and lifetime drift (e.g., ±100ppm/°C temperature coefficient and ±1% lifetime drift).	402 ±1%. Use a single resistor.	Ω
Link-Isolation Capacitors	C_{LINK}	Place in series and in close proximity to the SIO pins (pins 12 and 13).	0.1	µF
Termination Resistor for SIO_N pin	R_{TERM}	Connect in series with C_{LINK} capacitor between SION and ground. Place near associated SION pin.	49.9 ±1%	Ω
Crystal		Place as close as possible to pins X1 (pin 8) and X2 (pin 9), and connect between these two pins.	25MHz ±200ppm	
Crystal Load Capacitors		Use crystal-loading capacitor guidance from the crystal manufacturer. Select values that compensate for the X1 and X2 input and PCB node capacitances. Place the capacitors as close as possible to pins X1 (pin 8) and X2 (pin 9).	Crystal dependent	pF

Table 3. External Component Requirements (continued)

V_{DD18} Decoupling Capacitors*		Place 0.01µF, 0.1µF capacitors as close as possible to each V_{DD18} pin (pins 11 and 16). Include a minimum of 10µF bulk decoupling on the PCB.	0.01 + 0.1 + 10	µF
V_{DD} Decoupling Capacitors*		Place a 0.01µF, 0.1µF capacitors as close as possible to pin V_{DD} (pin 15). Include a minimum of 10µF bulk decoupling on the PCB. See configuration information in the *Power Supplies* section.	0.01 + 0.1 + 10	µF
CAP_VDD Decoupling Capacitor		Place a 0.1µF capacitor as close as possible to pin 14. Include a minimum of 10µF bulk decoupling near the pin.	0.1 + 10	µF
Open-Drain Pullup Resistors		Application-specific. Quantity and values depend on multifunction GPIO pin configurations.		
Resistors for Configuration Pin Resistor Divider	R1, R2	Place resistor-divider close to pin 3 (CFG0).	Use ±1% tolerance resistors. See Table 7.	Ω
	R1, R2	Place resistor-divider close to pin 4 (CFG1).	Use ±1% tolerance resistors. See Table 8.	Ω

*With exception of CAP_VDD, power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

ESD Protection

Table 4. ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SIO_	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±8		kV
		ISO 10605, R_D = 330Ω, C_S = 150pF, Contact Discharge		±6		
		ISO 10605, R_D = 330Ω, C_S = 150pF, Air Discharge		±8		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±4		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Figures

GMSL2 Serial Output Parameters

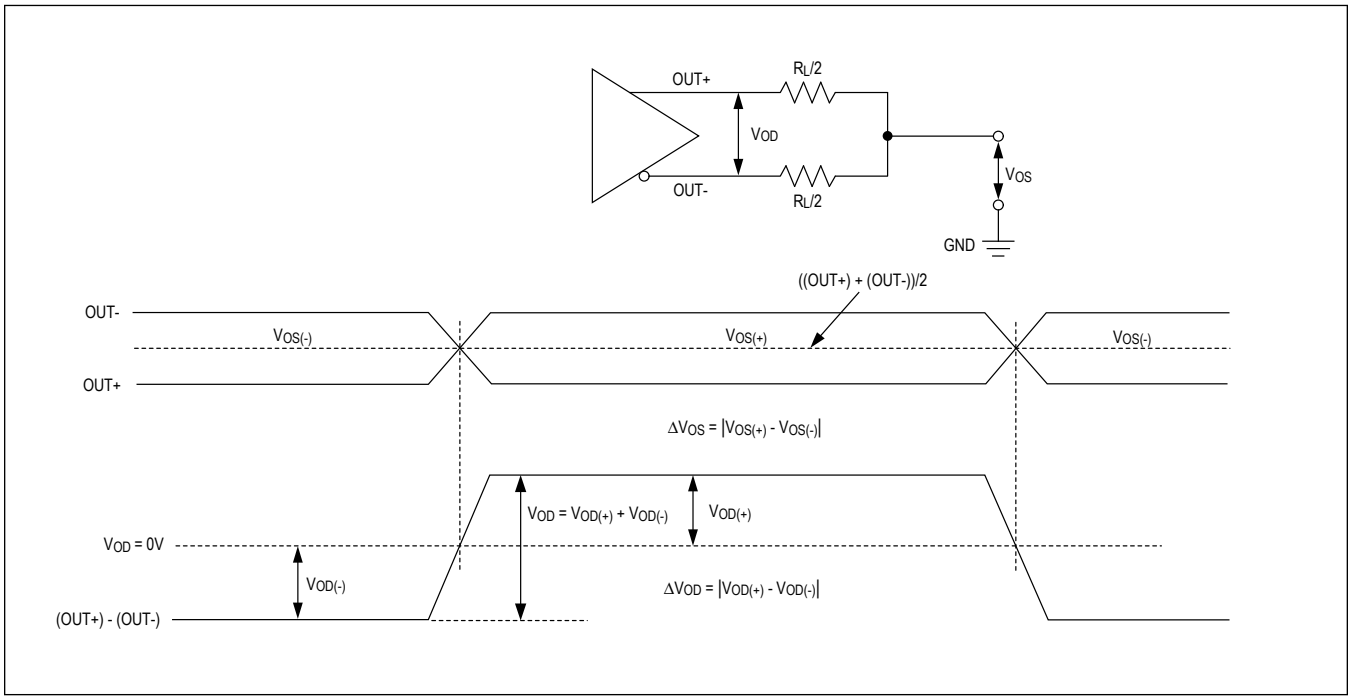


Figure 1. Serial Output Parameters

GMSL2 Data Initialization Time

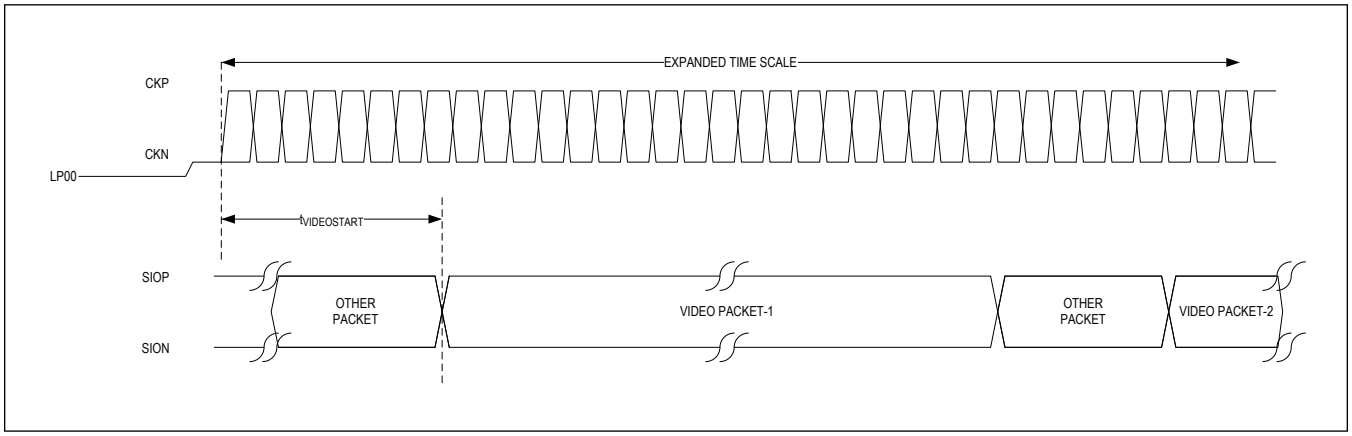


Figure 2. GMSL2 Data Initialization Time

I²C Timing Parameters

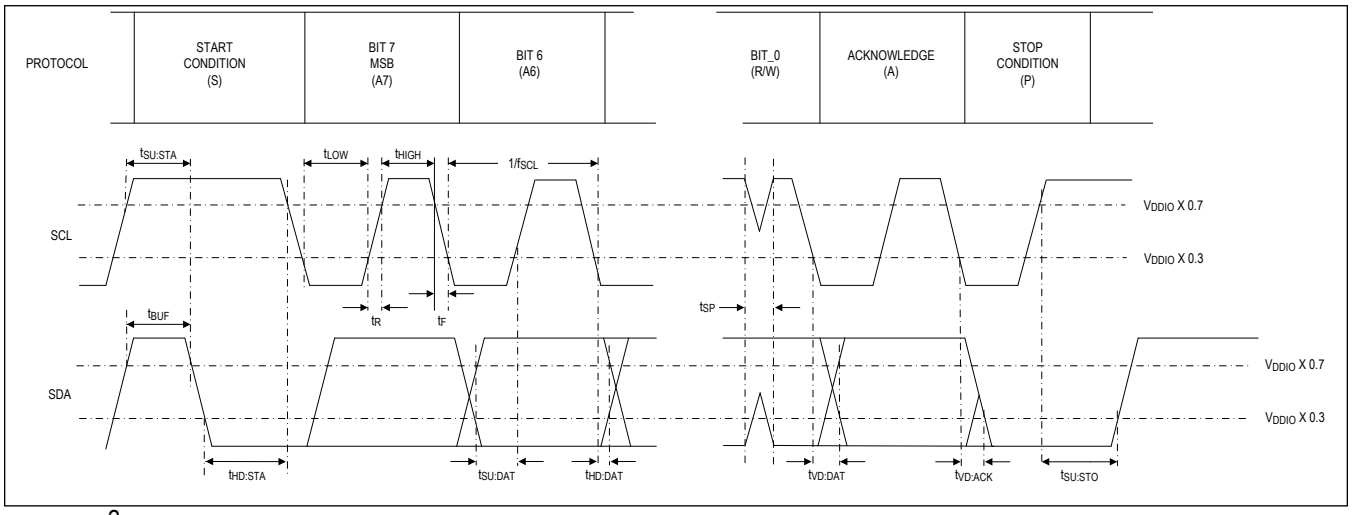


Figure 3. I²C Timing Parameters

GMSL2 Data Latency

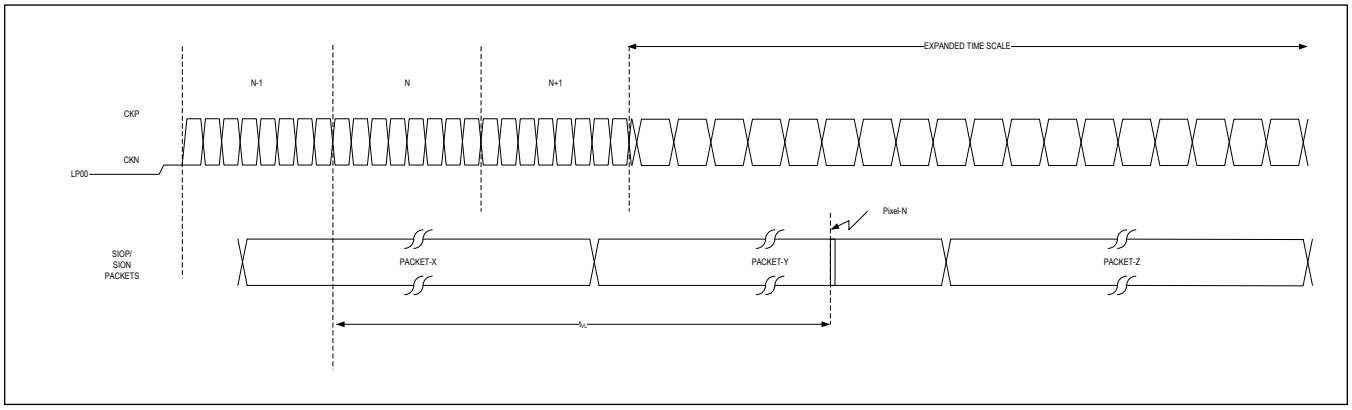


Figure 4. GMSL2 Data Latency

D-PHY LP Receiver Pulse

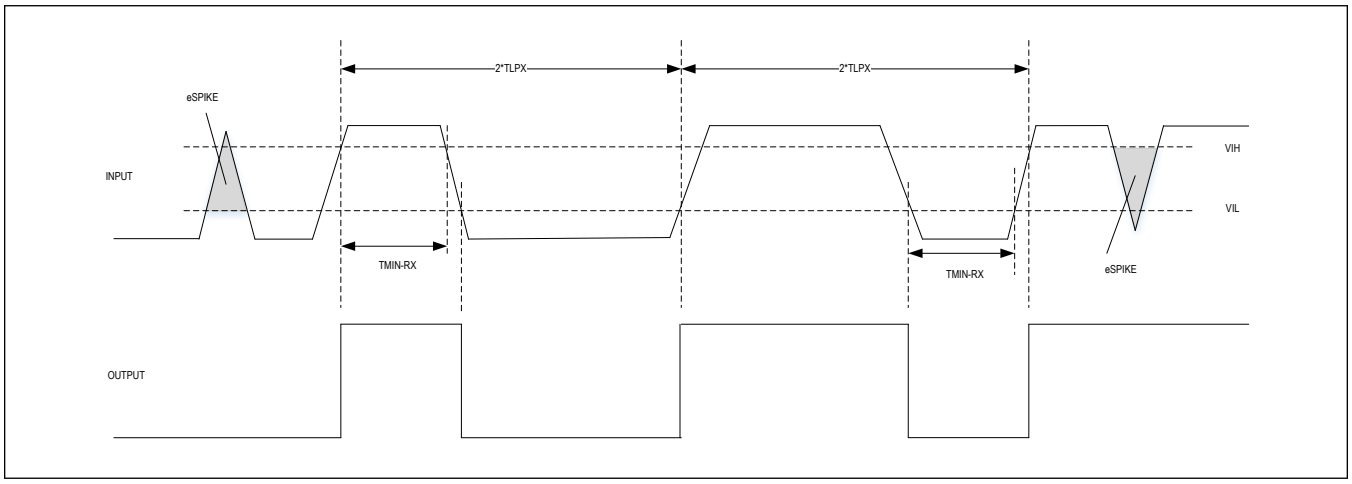


Figure 5. D-PHY LP Receiver Pulse

D-PHY Data Clock Timing

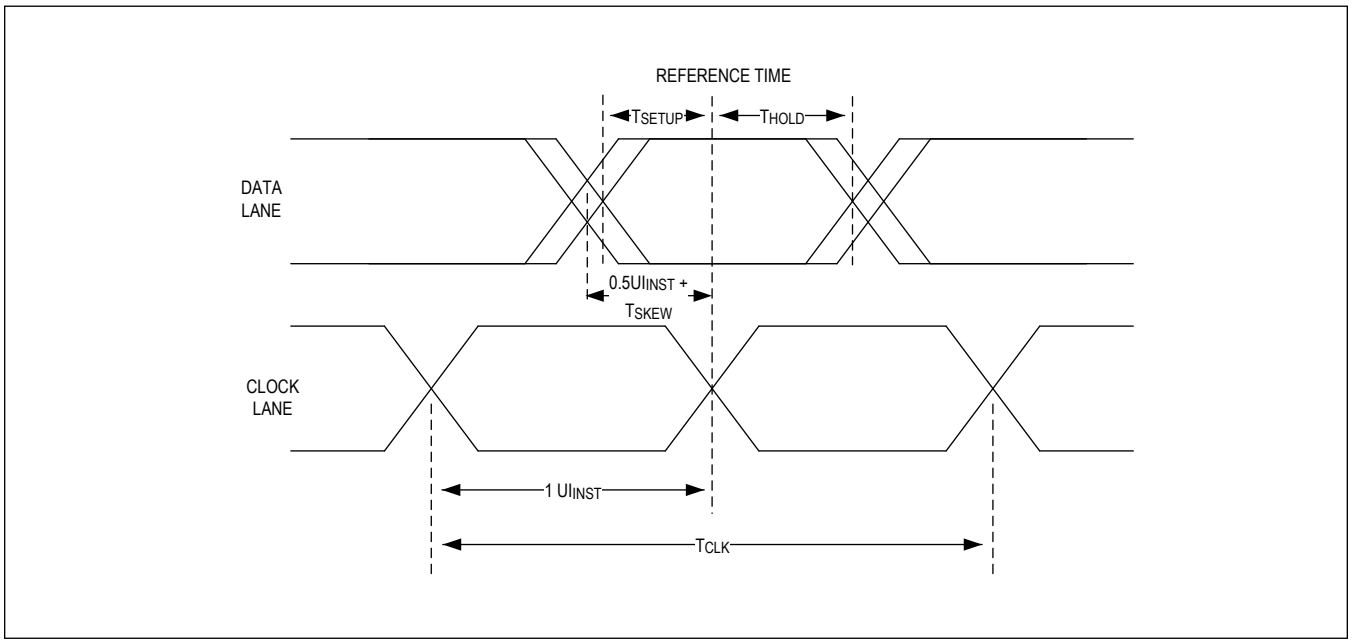


Figure 6. D-PHY Data Clock Timing

High-Speed Data Transmission in Bursts

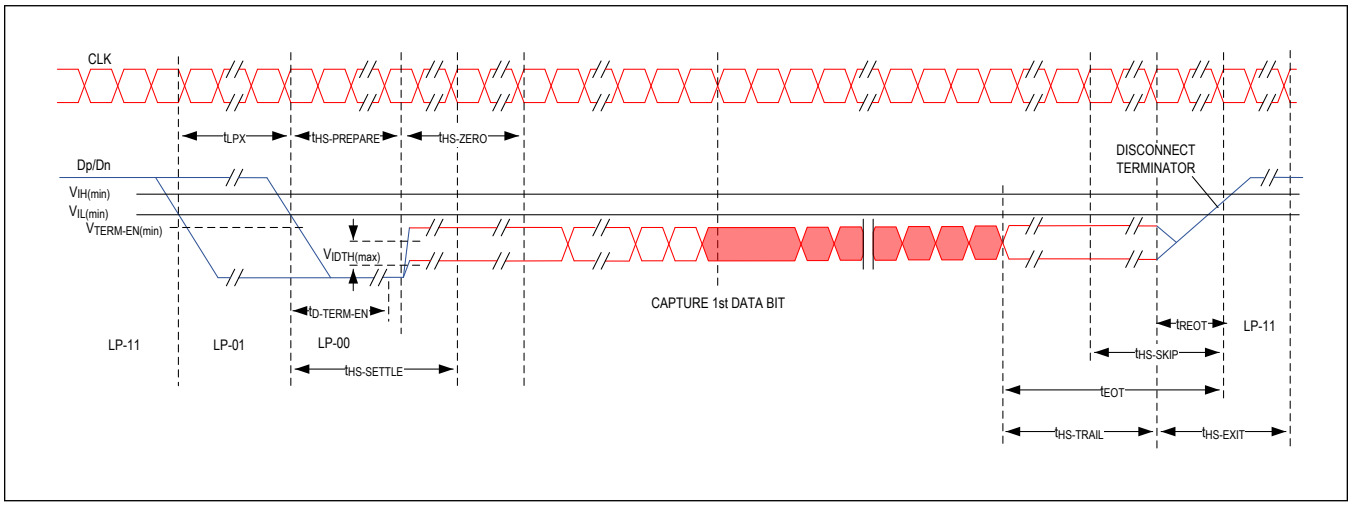


Figure 7. High-Speed Data Transmission in Bursts

D-PHY High-Speed Skew Calibration

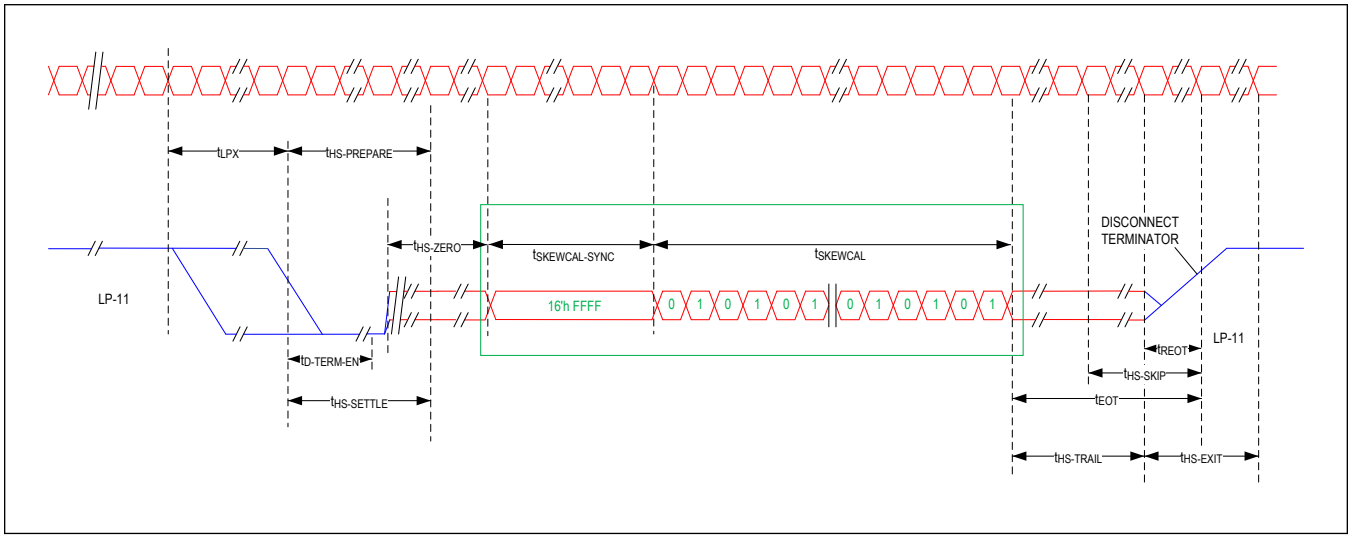


Figure 8. D-PHY High-Speed Skew Calibration

Switching the Clock Lane Between Clock Transmission and Low-Power Mode

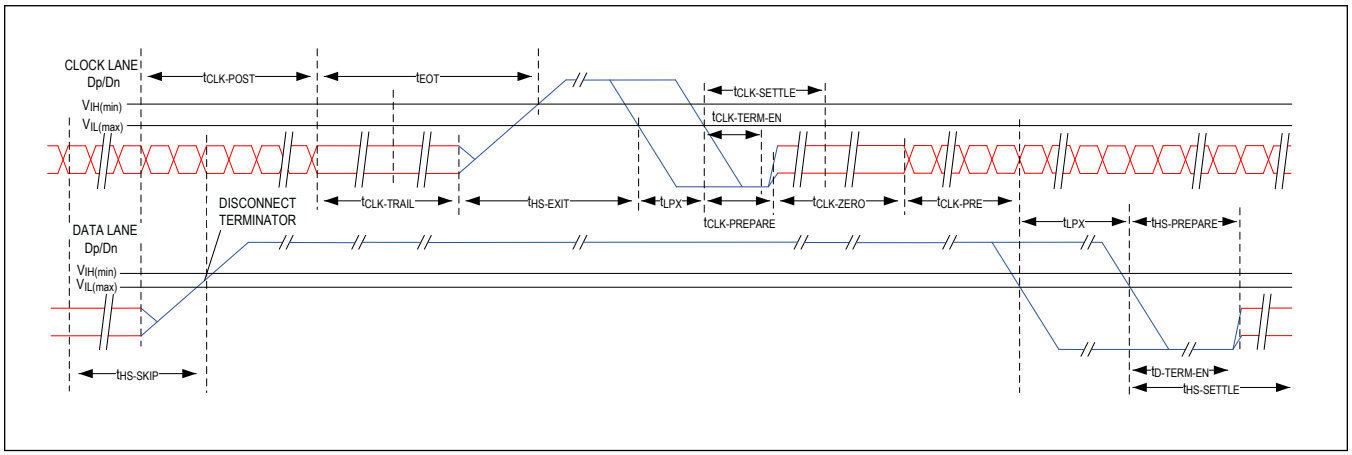


Figure 9. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

Signaling and Contention Voltage Levels

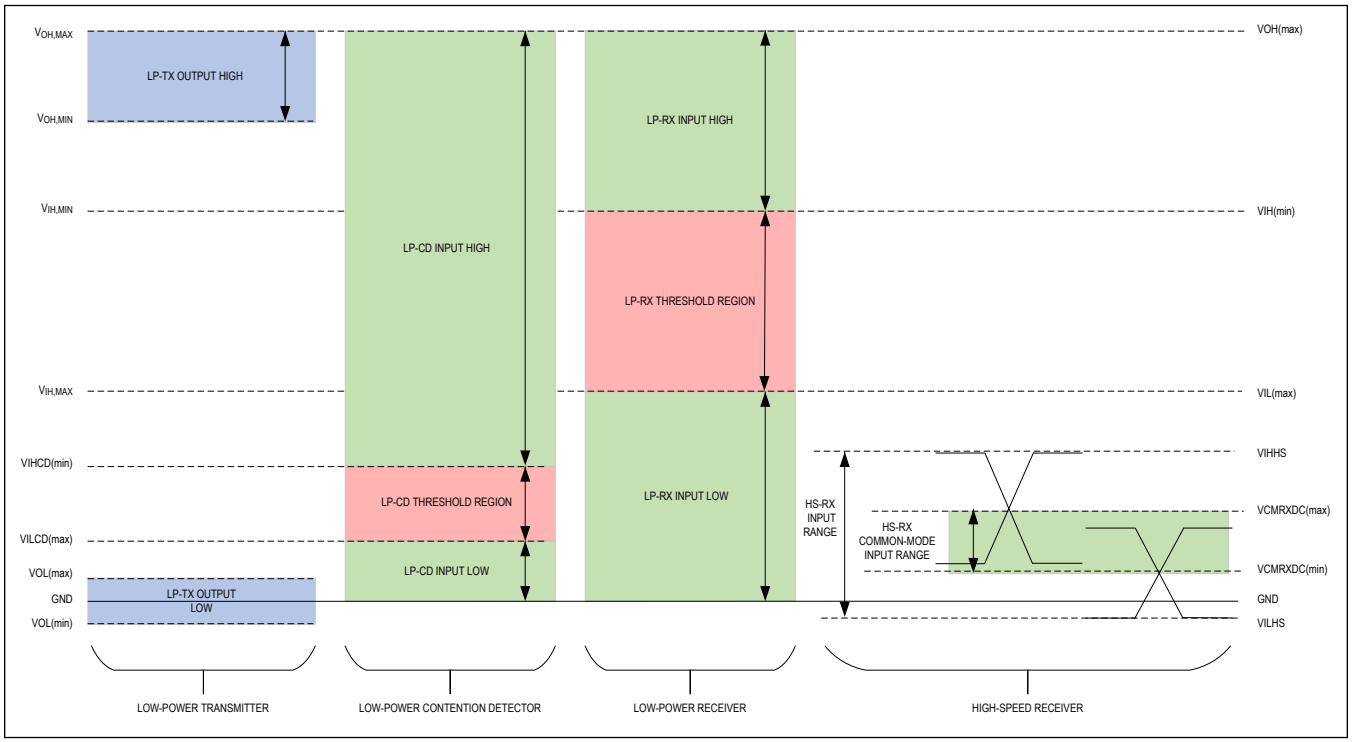


Figure 10. Signaling and Contention Voltage Levels

Introduction

Analog Devices' tunneling GMSL2 serializers and deserializers provide end-to-end data integrity of both sensor data and side-channel data, while also providing sophisticated link management for high-speed, low bit-error-rate, and serial data transport. They support a comprehensive suite of sensor and communication interfaces over a single wire. The serializer provides 3Gbps forward and 187.5Mbps reverse packetized data transmission over each fixed-speed link.

The following sections provide a brief overview of the device functions and features. Contact the factory for additional information, and details on configuration of each function and feature.

Product Overview

The MAX96717R serializer converts MIPI CSI-2 to single-link GMSL2. See Figure 11. It also sends and receives side-channel data, enabling full-duplex transmission of forward-path sensor data and bidirectional data over low-cost 50Ω coax cables meeting the GMSL2 channel specification.

The MAX96717R has a four-lane D-PHY v1.2 that supports a data rate of 108Mbps to 600Mbps per lane. Four virtual channels are also supported.

The MAX96717R is intended for use with a GMSL2 deserializer such as the dual-port MAX96716A/B/F, a quad-port MAX96712 or MAX96722, or a GMSL3 deserializer operating in GMSL2 mode. For example, when used with the MAX96716F, several modes are supported. A single sensor can be connected to an SoC in GMSL2 modes at a data rate of 3Gbps, as shown in Figure 11. Two MAX96717R serializers can be used with one MAX96716F deserializer to connect two sensors to two SoC devices (see Figure 12). The cable types, sensor timing, and data rates do not have to be the same. Data from link A and B are output on separate, dedicated CSI-2 ports for capture by the SoCs.

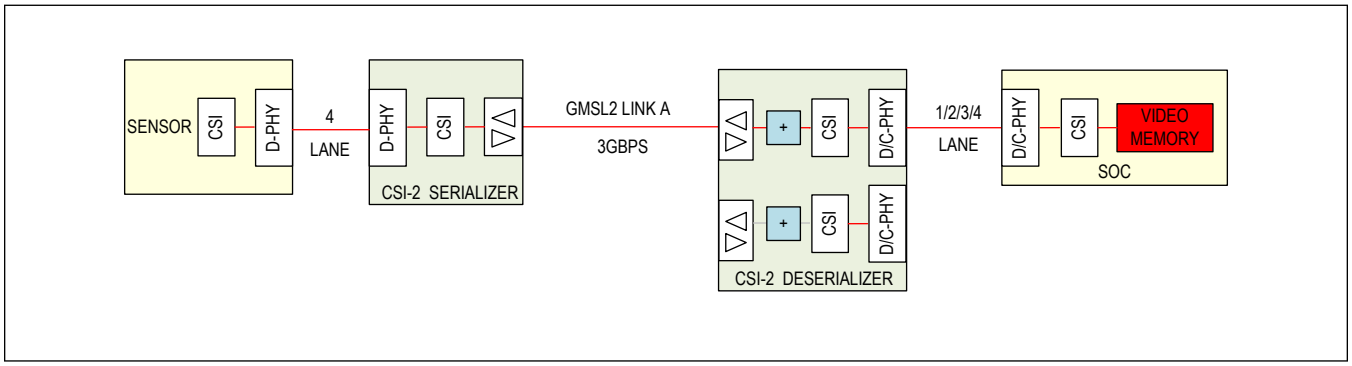


Figure 11. Single Link

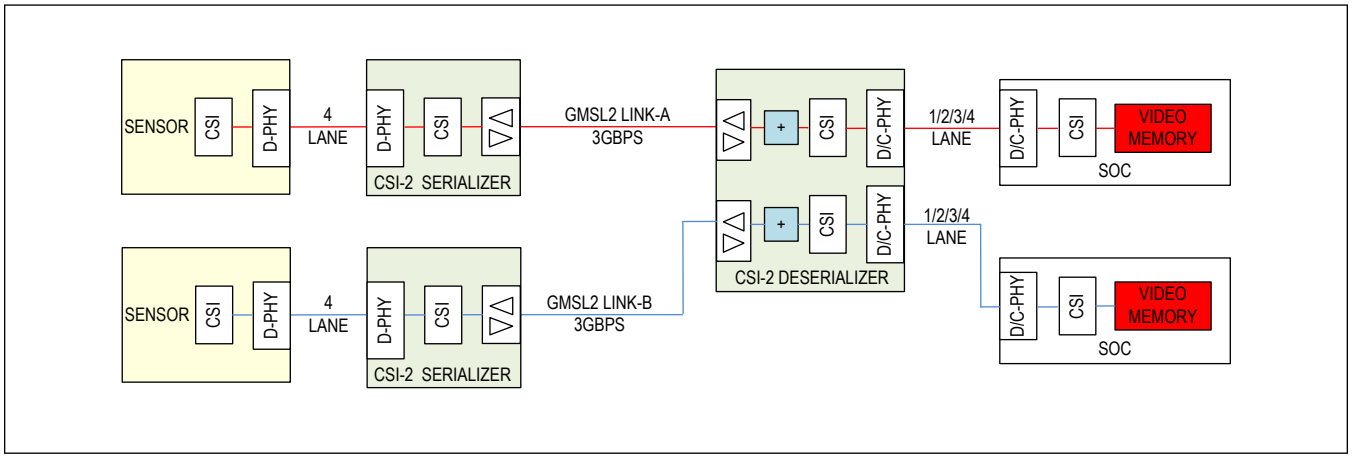


Figure 12. Dual-Link, Separate Data Type

The deserializers support data aggregation, as detailed in Figure 13. The sources can have different video timing and resolution. The SoC identifies the video source by reading the packet's virtual channel. If both sources use the same virtual channel, the MAX96717R can assign a different virtual channel in Pixel mode. Reassignment of up to 16 data types is also possible in Pixel mode. The aggregated data can be replicated to both MIPI ports, allowing multiple SoCs to process the same data, as shown in Figure 14.

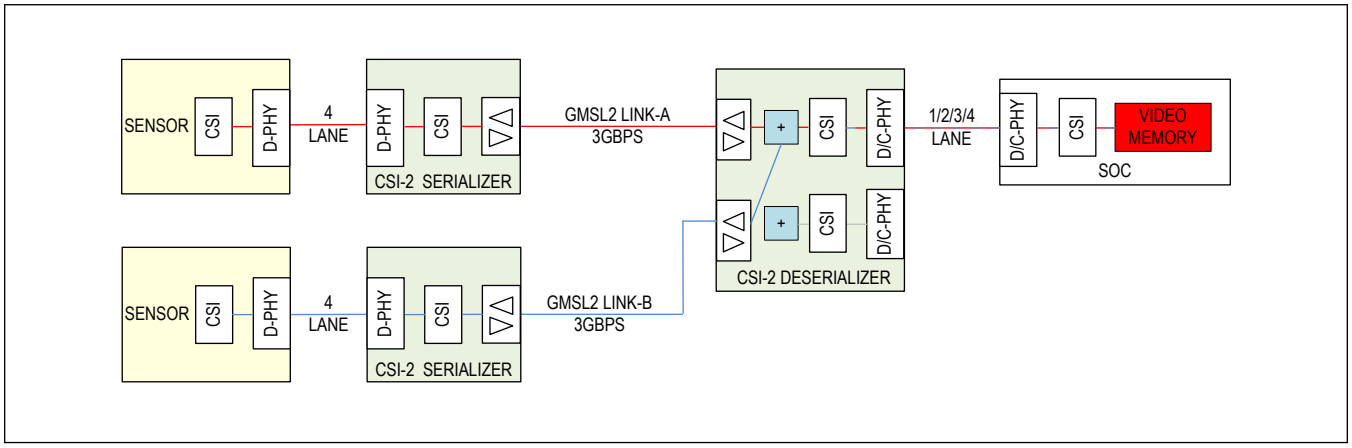


Figure 13. Dual-Link, Data Aggregation

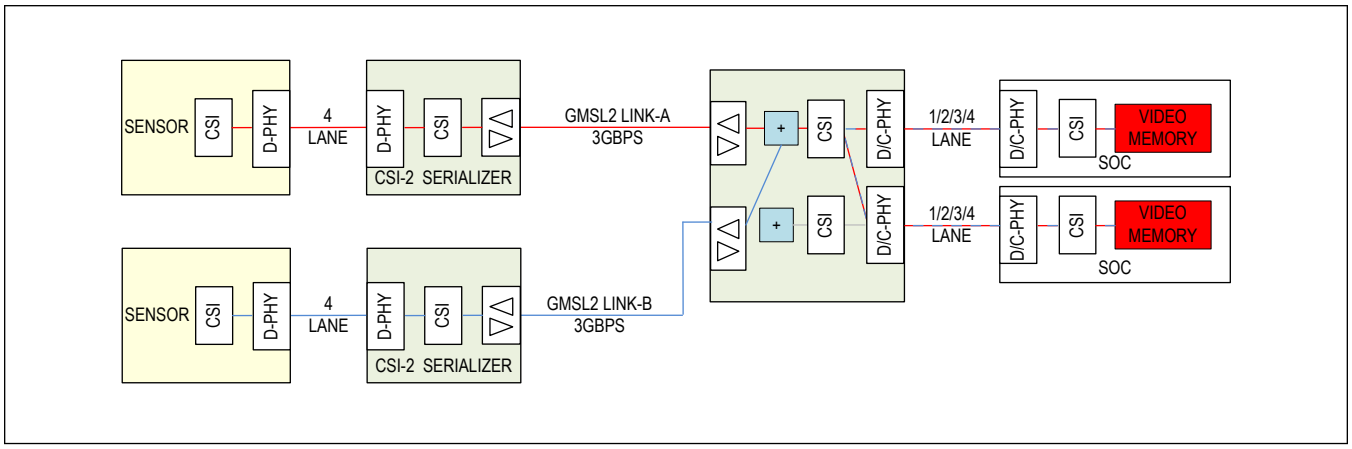


Figure 14. Dual-Link, Data Aggregation and Replication

The MAX96717R is an ideal sensor serializer to use (it has a CSI-2 interface, and single or multiple data types) when various cameras and/or sensors need to be supported.

Tunneling and Pixel Modes

The MAX96717R is specifically designed for advanced driver assistance systems (ADAS), where data integrity is a key safety requirement. Prior GMSL2 solutions supported only Pixel mode for transporting received data from a MIPI CSI-2 interface over the GMSL link. In Pixel mode, the CSI-2 data is depacketized at the serializer's CSI-2 input interface. The received CSI-2 packet header includes an error correction code (ECC), which is checked and removed at the serializer input. The received CSI-2 packet footer contains the CSI-2 cyclic redundancy check (CRC), which is also checked and removed.

Video line pixel data and video routing information, such as data type and virtual channel, are received and extracted at the CSI-2 interface. Both video pixel data, control channel data, and routing information are input into a scheduler in the serializer. The scheduler packetizes and encapsulates the data using GMSL protocol and sequences data transmission

across the GMSL link. Video data transport across the GMSL link is protected by line CRCs that are part of the GMSL protocol.

The deserializer receives the GMSL packets and verifies the GMSL2 line CRCs. A CSI-2 interface at the deserializer output encapsulates each video line using CSI-2 protocol and outputs it in CSI-2 format across a CSI-2 interface to the SoC (see Figure 15).

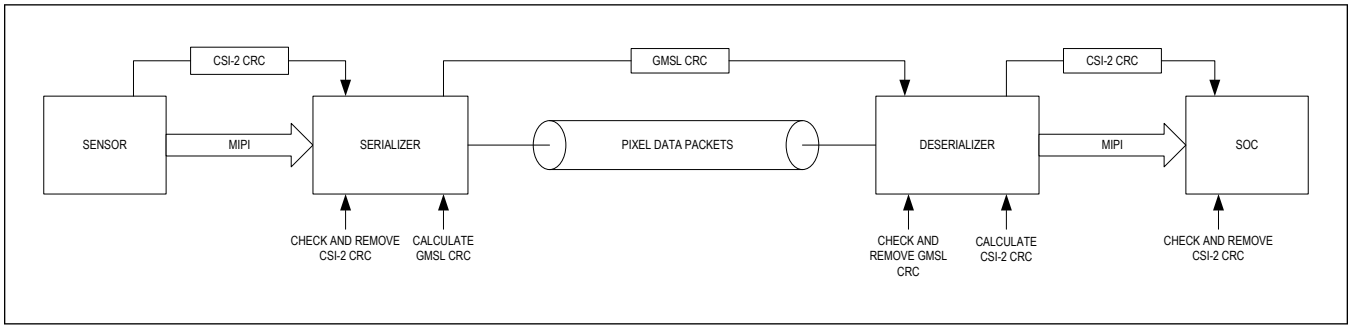


Figure 15. Pixel Mode

In Tunneling mode, the received CSI-2 ECC byte and CRC bytes are checked at the serializer input. These, as well as routing and pixel data, are received as a byte stream. The byte stream is split into smaller packets that are encapsulated using GMSL2 protocol.

The serializer adds a line CRC, protecting transmission across the GMSL channel. This CRC covers the entire GMSL2 packetized byte stream for a video line (see Figure 16). The deserializer receives the transmitted GMSL2 packets and control channel packets, checks and removes the GMSL CRC, separates the video data from control data, and reconstructs each received CSI-2 packet that is output to the SoC on a CSI-2 interface. A CRC is calculated on the video data output on the CSI-2 interface. This CRC is compared by the deserializer to the original CRC received from the video source. This comparison guarantees that the entire data packet output on the standard MIPI interface is identical to that received at the serializer input. Tunneling mode is more bandwidth-efficient if multiple data types are being sent. Because data received at the serializer input and data output from the deserializer are verified to be identical, Tunneling mode does not allow for the processing of video data, such as watermarking or lossy data compression. Different data rates and lane counts on the serializer and deserializer are still possible.

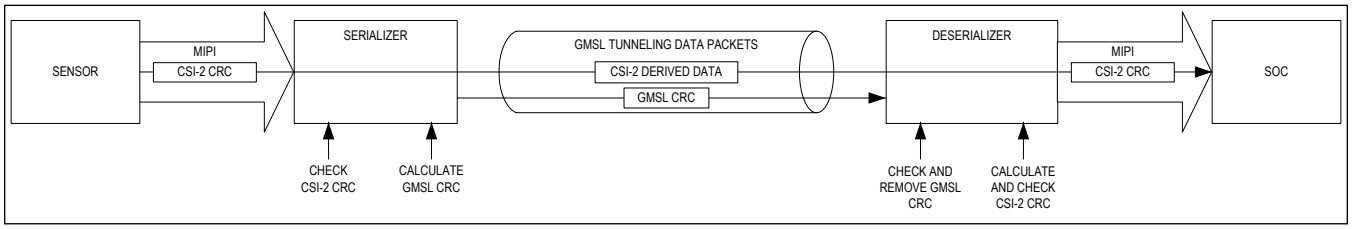


Figure 16. Tunneling Mode

Video Pipeline

The video channel is designed to transmit video data received from the CSI-2 interface to the deserializer side of the link. The following data types are supported: RGB888, RGB666, RGB565, YUV422-8, YUV422-10, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20, User-Defined, Embedded, and Null. By default, the bits per pixel (bpp) of the video stream is automatically detected by inspecting the data type of the CSI-2 packets. If a video stream with a different bpp is sent through the same video pipe in Pixel mode, disable the auto-detect through a register write. Video input data consists of color, HS, and VS synchronous to the pixel clock (PCLK). Reception of video is detected using the PCLKDET function. Video flows through the design as described in the following sections.

Video Pipes in Pixel Mode

Video data transport in GMSL2 Pixel mode is based on the concept of video pipes. Carrying data in pipes allows GMSL2 to bridge different digital video interfaces and perform watermark generation and detection. (Note: Watermark generation is not supported by this device.) A pipe carries video stream(s) and video synchronization data and operates in one of the following modes:

- Mode 1: Streams with constant bits per pixel (bpp) of up to 24bpp. The bpp of the streams must be the same.
- Mode 2: Streams with 16, 14, 12, 10, or 8bpp. Streams less than 16bpp are padded with zeros.
- Mode 3: Streams with two different bpp rates. The bpp of one stream must be twice the bpp of the other stream. The higher bpp stream maximum is 24bpp.

In all modes, a pipe can carry multiple concurrent video streams, with each stream having different virtual channels and data types.

Modes 1 and 3 carry data at full bandwidth, but put more restrictions on bpp than Mode 2. Mode 2 allows streams with different bpp rates, but streams of less than 16bpp are carried using more bandwidth than necessary on the GMSL2 link because of zero-padding. Mode 1 or 3 are sufficient for most applications. Mode 2 requires less programming and is more convenient if the application does not require maximum link bandwidth.

The MAX96717R has a single input port and one video pipe. The pipe in the MAX96717R has a dedicated MIPI receiver buffer. The retiming buffer has the capacity to buffer 96 24-bit pixels. This allows sufficient memory for transmission of a line to start, and not overflow or underflow. The number of pipes used by a deserializer is equal to the number of pipes used by all connected serializers.

After data exits a retiming buffer, it goes through a crosspoint switch and a data type (DT) and virtual channel (VC) reassignment stage. If the video source has a CSI-2 output, packet DT and VC can each be left as-is or reassigned by register programming. Up to four DT/VC incoming pairs can be mapped to four DT/VC outgoing pairs.

Video-Timing Generator

The MAX96717R includes a programmable video-timing generator (VTG) to generate or retime input video sync signals. The timing generator can modify source (i.e., sensor or image signal processor (ISP)) input timing, filter out glitches in the sync signals, or reduce the number of input sync signals. Each sync signal can be individually retimed or left unmodified. Several registers determine the length of the timing parameters in pixel clock cycles. Timing parameters include high/low period length, line count, and delay from the input VS signal. The parameters of the VTG are set in the REF_VTG registers.

The timing generator uses three different trigger modes: tracking, single trigger, and auto run.

- Tracking locks once three consecutive identical VS signals are received. The tracker then outputs the same VS signal, filtering any glitches on the input VS. It attempts to relock if three consecutive VS input waveforms do not match the locked signal.
- Single trigger generates one frame for each VS.
- Auto run generates a new frame at the rate determined by the VS high/low period. If a new VS signal appears before a frame is complete in either single-trigger or auto-run modes, a new frame immediately starts, cutting the previous frame short.

VS, HS, and PCLK signals can be output on MFP pins 0, 1, 2, 3, 4, 7, or 8, as defined in registers REF_VTG1, REF_VTG2, and REF_VTG3.

RGB888 Video-Pattern Generator

The RGB888 video-pattern generator (VPG) is an auxiliary block that can be used for a variety of purposes, such as replacing video from the peripheral with the video pattern generated by the VPG. Various patterns can be generated when configured using the configuration registers. The VPG creates a checker board pattern and gradient using RGB888 data.

Note: The VPG is only for use in Pixel mode.

Tx Crossbar

Data from the video input is captured and optionally multiplexed with the generated patterns from the VPG. Final data goes into a crossbar multiplexer that allows any input bit to be mapped to any output bit using the configuration registers.

The crossbar should only be used in Pixel mode.

GMSL2 Packet Protocol

Packet Protocol

GMSL2 is a fixed-rate, packet-base transmission protocol that is designed to efficiently and dynamically carry multiple types of communication channels concurrently. Link bandwidth is only used by a channel when data is being sent. The link bit rate is based on a constant-frequency link clock generated from the 25MHz crystal oscillator. The link clock does not have any relation to the video-pixel clock.

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic, so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. Maximum packet size is limited to prevent a single channel from utilizing the link bandwidth for an extended time. In most cases, available link bandwidth exceeds the bandwidth requirement. Idle packets are used to fill in the unused link bandwidth.

The same data protocol is used on forward and reverse channels, and for both video and control-channel data.

Tunneling Mode

Tunneling mode transmits all MIPI CSI-2 content, without modification, over the serial link. Unlike Pixel mode, the received CSI-2 payload is not decoded. Unchanged CSI-2 bytes are split into smaller GMSL packets that are encapsulated and protected with GMSL CRCs, and are transported across the link. This means the CSI-2 headers and footers generated by the video source, including ECC and CRC, are preserved through the GMSL link, and can be decoded by the host connected to the deserializer. This provides end-to-end data integrity critical for ADAS vehicles.

Pixel mode checks the ECC and CRC packets for errors at the serializer, and then removes them prior to converting the payload to pixels and transmitting over the GMSL2 link. In Pixel mode, the deserializer recalculates and inserts the CSI-2 ECC and CRC packets. Both Tunneling and Pixel modes have CRC protection of the serial-link payload so any GMSL link errors are detected. However, an error in recalculating the ECC/CRC packets in the deserializer is not detected by the SerDes, but is detected by the MIPI video sink device.

CRC Generation and Checking

Every packet (excluding Idle and Acknowledge packets) can be protected by a 16-bit packet CRC. Each packet type can be individually configured to enable or disable packet CRC. By default, all low-bandwidth channels have packet CRC. Note that since Acknowledge packets contain no data and the header is repeated, CRC is unnecessary. Although the video channel disables packet CRC in default settings in order to maximize usable bandwidth, video-line CRC (a 32-bit code at the end of each DE or HS pulse) is enabled by default to provide data protection.

The 16-bit packet CRC generator polynomial is: $x^{16} + x^{15} + x^2 + 1$.

Control-Channel Retransmission on Error

Automatic Repeat Request/Automatic Retransmission (ARQ)

Communications channels with control data (e.g., I^2C, GPIO) are relatively low bandwidth, but require the highest data integrity protection. An optional automatic packet retransmission method, automatic repeat request (ARQ), is employed here. ARQ works in conjunction with 16-bit packet CRC to detect whether packets are received with or without error.

Packets are appended with a 2-bit sequence number at the transmit side, and an acknowledge is sent from the receiver side upon successful receipt of each data packet. These packets are stored on the transmit side until acknowledged. If the acknowledge does not arrive in a predetermined interval or the sequence number of the acknowledge does not match the expected value, the packet waiting at the top of the queue is automatically retransmitted.

The Acknowledge packet uses the same header field as low-bandwidth packets, but begins with a different special symbol to distinguish it from regular data packets. This simplified format keeps retransmission exchanges independent from the communication channel. Note that this smaller packet format contains no data, obviating the need for full 16-bit CRC. Instead, the header symbol is sent twice in the packet and checked against each other to ensure a match. The Acknowledge packets also include a 2-bit sequence number that is the same sequence number of the correctly received data packet. The data packet transmitter keeps track of which packets are acknowledged.

Scheduler/Arbiter

A scheduler transmits packets with high-priority values before lower priority values. Each communication transmit adapter sets a priority for the packet request before transmitting data to the remote side. The priority value is 2 bits, allowing for four different settings: 0 = Low, 1 = Normal, 2 = High, and 3 = Urgent. The scheduler, provided there is sufficient link bandwidth, chooses to transmit the packet with the highest priority among the pending active requests. Priority levels become more important as link bandwidth becomes scarce. Prioritization should be assigned accordingly.

In most cases, each transmitter adapter should use the normal priority setting (priority = 1) to allow the scheduler to choose the transmission schedule based on recent bandwidth usage. Packet priority can be increased if packets require low latency or have waited for a length of time. For example, packets with maximum latency requirements can have increased priority if the packet request has not been serviced until half of the maximum latency requirement has elapsed. This can also be used for communications channels with continuous data flow (e.g., video). Priority is increased when the transmit adapter data buffer approaches overflow. Conversely, register configuration allows overriding the priority settings of each channel. This option is useful if the host µC wants to prioritize one channel over the others.

Note: Communications channels with very relaxed latency requirements can use the low-priority setting (priority = 0). These low-priority packets are not serviced by the scheduler if there are any pending requests of a higher priority setting. In this arrangement, link bandwidth assignment can reach the theoretical maximum for video. Low-priority packets can then be transmitted during video horizontal blanking time, during which the video channel bandwidth usage drops considerably.

Bandwidth Sharing

The GMSL2 link bandwidth is shared flexibly between different communication channels including video/data, I^2C control channel, and GPIOs, as well as various protocol-specific data exchanges including information frames, sync, and acknowledgments. Each channel must request the link for packet transmissions. This flexibility comes from packet-based transmission format and dynamic bandwidth allocation. If a certain channel is not active, it does not consume any link bandwidth, leaving the full link bandwidth available for all active communication channels to share. The packet-based protocol allows fulfilling this sharing requirement. The maximum packet size is limited to 64 20-bit words to prevent one single channel from monopolizing the link bandwidth and to ensure other channels are served. The total-link bandwidth used by all communication channels cannot exceed the fixed available link bandwidth or errors occur.

The data and control-channel packets can be assigned a priority level. There are four priority levels: low, normal, high, and urgent. The scheduler transmits the packet with the highest priority among the pending requests. Packets with maximum latency requirements can be assigned an increased priority.

A bandwidth sharing scheme is employed in cases of multiple pending requests of the same priority setting to avoid creating buffer overflows. Without bandwidth sharing, a burst data request from a channel can cause buffer overflow in other communications channels on the link. Bandwidth sharing, however, considers predefined bandwidth share ratios and recent bandwidth usage averages of each type of communication channel to avoid buffer overflows and ensure all channels are served.

An arbiter continuously measures the bandwidth usage of each channel and filters the data according to the analysis of the moving averages. This data is then compared to assigned bandwidth share ratios. In order to ensure link bandwidth parity, the arbiter takes this recent bandwidth usage information in order to decide which channel is allocated to use the link for each new packet transmission request.

GMSL2 Physical Interface

Adaptive Equalization (AEQ)

The GMSL2 devices automatically adapt the receiver's characteristics to compensate for the insertion and return loss characteristics of the channel that consist of the cables, connectors, and PCBs. This approach optimizes performance on any channel that meets the GMSL2 channel specification. The equalizer architecture makes GMSL2 links robust against noise, crosstalk, and reflections. Initial adaptation is performed during link lock and is then invoked at a rate of approximately 1Hz to track temperature and voltage variations. The adaptation process optimizes the equalizer coefficients to minimize the intersymbol interference observed at the output of the equalizer.

Echo Cancellation

The GMSL2 link includes an echo cancellation circuit in both the serializer and deserializer to enable simultaneous transmission of high-speed video data and bidirectional control data.

Spread-Spectrum

Spread spectrum is used to reduce electromagnetic interference (EMI). Optional spread-spectrum clocking (SSC) is available to mitigate electromagnetic interference emitted from the device and interconnections and provides additional margin. SSC reduces peaks in the frequency spectrum by spreading the energy over a wider bandwidth. The forward-channel, spread-spectrum frequency is programmable in the range of 10kHz to 40kHz, and the frequency deviation is programmable in the range of 0% to ±0.125%. If no forward-channel, spread spectrum is programmed, up to 0.5% frequency deviation can be tolerated.

Link Lock

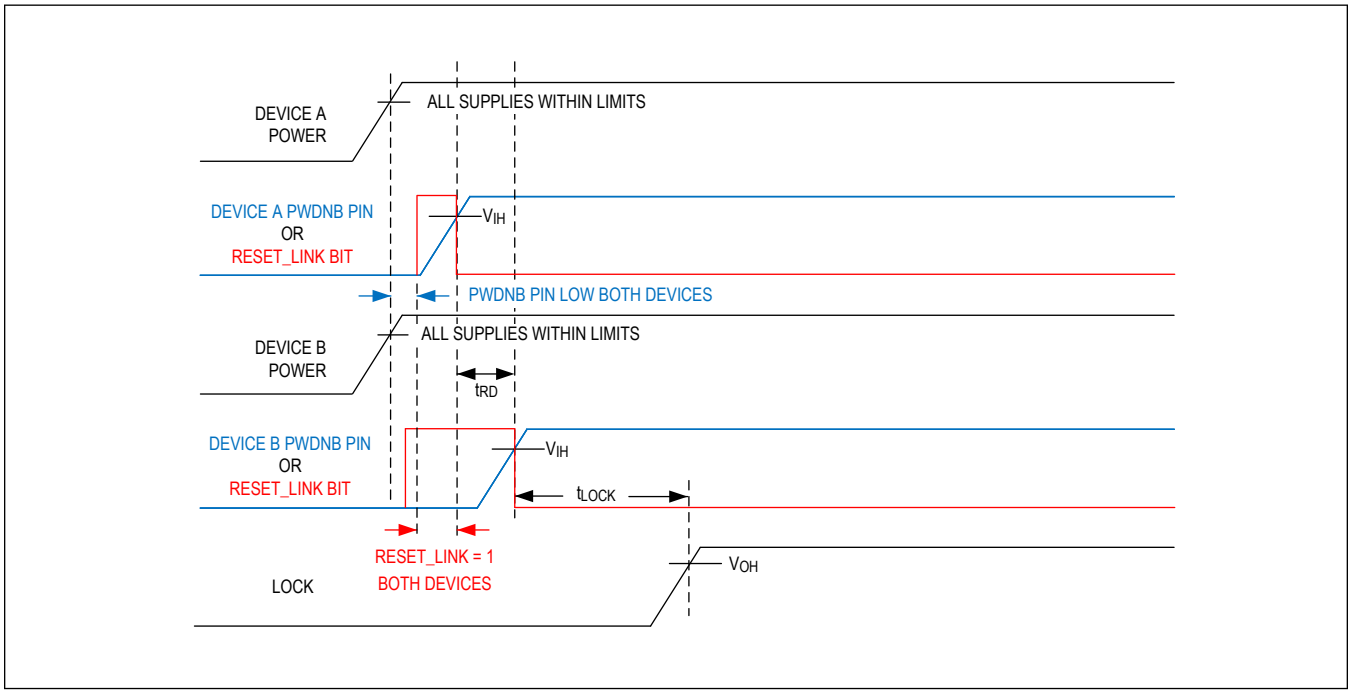


Figure 17. GMSL2 Lock Time

Figure 17 illustrates the sequence that is used to characterize GMSL2 link lock time. Device A is the first device (serializer or deserializer) to power up or resume operation from a RESET_LINK state. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

Link lock indicates that the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I^2C, GPIO) can be used immediately after link lock is asserted.

The device establishes single-link GMSL2 connectivity and link lock automatically following power-up. This is an indication that the cable is plugged in, and the system is up and running. Lock is obtained with no interaction between the µC and GMSL devices. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

The MAX96717R has only one link; therefore, it does not support dual-link and splitter configurations.

The GMSL2 link uses the crystal as the reference clock for GMSL2 links, so a valid video input (PCLK) is not needed for the GMSL2 link to lock.

Notes:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.

2. The lock time is measured from the PWDNB or the RESET_LINK release, whichever is later, on either the serializer or the deserializer to the lock being asserted.

3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both the devices are in PWDNB/RESET_LINK mode prior to the lock process starting.

4. If RESET_LINK is used to initiate the lock, PWDNB is assumed to be high after power-up (normal operation).

5. If PWDNB is used to initiate the lock, RESET_LINK is assumed to be low after power-up (normal operation).

6. Device A is the first device (serializer or deserializer) to be powered up. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

7. To achieve the specified lock time, time delay t_{RD} (delay between the release of the PWDNB/RESET_LINK on the two devices) must be less than 90ms. If this timing cannot be guaranteed, contact the factory for guidance.

8. Lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. Similarly, the maximum permitted t_{RD} for a specific link can be estimated as the smaller of the values specified in each device data sheet. For further guidance, contact the factory.

9. If there is an instantaneous interruption to link lock, a period of 100ms following loss of lock should be provided to enable the link to automatically recover prior to any ECU initiated resets being issued. This will minimize any disruptions caused by a transient loss in connectivity.

GMSL2 Bandwidth Calculations

The GMSL2 forward link has a fixed link rate of 3Gbps for the MAX96717R. The reverse-link rate is also fixed at 187.5Mbps. The GMSL2 protocol and channel coding overhead is roughly 16%. This leaves approximately 2.6Gbps of video payload data throughput in the forward direction and 162Mbps in the reverse direction.

Users must ensure that worst-case use cases do not exceed the available throughput of the forward and reverse links. Analog Devices' evaluation kit (EV kit) GUI includes a bandwidth (BW) calculator that can be used for initial bandwidth requirement estimates. Analog Devices also has other tools to calculate link-bandwidth utilization. Consult the factory for high-bandwidth use cases to ensure error-free performance.

Table 5 provides rough estimates of the bandwidth utilization for each communication channel.

Table 5. Forward- and Reverse-Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Video (Forward Path Only)	Bandwidth = PCLK x (bpp + 1 + video_pixel_CRC) x 10/9 x 2048/2047 Pixel mode PCLK calculations: PCLK = MIPI data rate/bpp PCLK = MIPI data rate/(2 x bpp) for double pixel mode PCLK = MIPI data rate/(3 x bpp) for triple pixel mode Tunnel mode PCLK calculations: PCLK = MIPI data rate/24 Bandwidth Notes: 1. The link bandwidth calculation uses the bpp value of the video pipe with highest bpp value of the transmitted datatype(s). (Pixel mode only) 2. Maximum bandwidth is limited by pixel clock rate PCLK. 3. video_pixel_CRC=0.5 (when video pixel CRC is enabled) PCLK Notes: 1. The PCLK calculation uses a datatype with the lowest bpp value (Pixel mode only) 2. Maximum PCLK is 300MHz for a 3Gbps link rate. 3. MIPI data rate includes horizontal and vertical blanking times
I^2C	13 to 40 x I^2C clock rate, depending on available link bandwidth
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled

Definitions:

H = Horizontal resolution (active pixels)

V = Vertical resolution (active video lines)

fps = frames per second

bpp = bits per pixel

MIPI data rate = Aggregate data rate of all lanes in the Mobile Industry Processor Interface (MIPI).

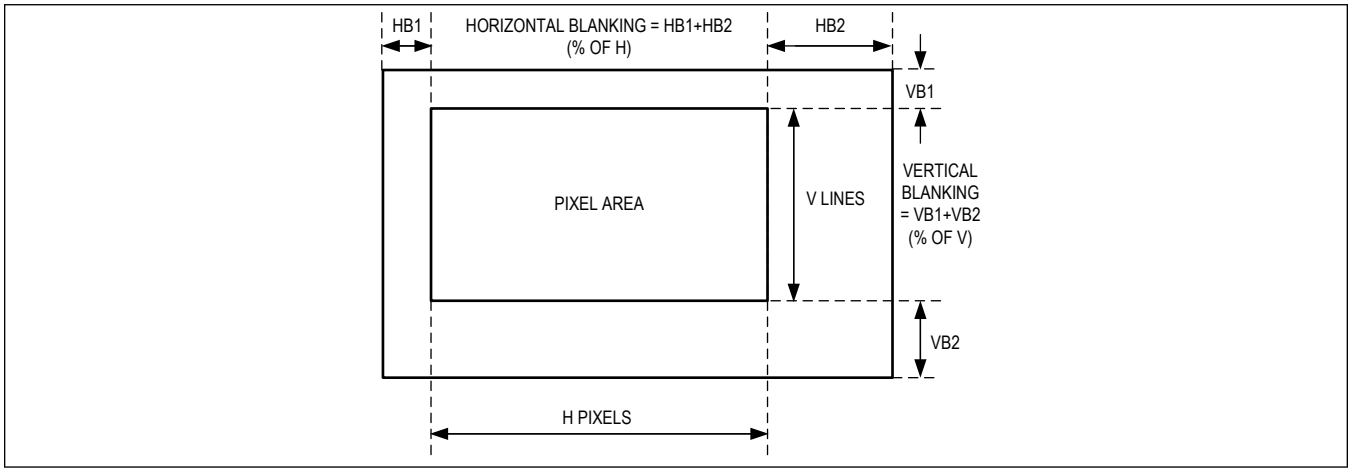


Figure 18. Video Frame Format for Bandwidth Calculation

Control Channel and Side Channels

A µC or other controller can send and receive control and side-channel data over the GMSL2 serial link simultaneously with high-speed video data. The MAX96717R supports I²C (register access) and GPIO. Both can pass data through the GMSL2 link. The GMSL2 device registers can be accessed and configured only through the I²C interface or remotely through the GMSL link.

The side channel, with its various interfaces, is accessed using multifunction pins. Multifunction pins have a default function and can be programmed to an alternate function after power-up. Due to a practical limit in the number of pins available on a given device, not all interfaces can be simultaneously supported. See *Pin Descriptions* and Table 9 for default and alternate multifunction pin functions, as well as available combinations of interfaces.

I²C

The main I²C is located on the SDA and SCL pins of each GMSL2 device. The I²C (SDA, SCL) interface is selected by the CFG0 pin voltage at power-up (see Table 7). The selected interface provides master access to both GMSL2 registers and device registers from either end of the link.

The master microcontroller (µC) can reside on either end of the link (usually the serializer side for display applications and the deserializer side for camera applications). The MAX96717R supports dual master microcontrollers, provided that software arbitration, such as token passing, is used to prevent packet collisions. The control channel allows only one master µC to communicate at a time. I²C outputs are open-drain and require appropriately sized external pullup resistors for proper operation.

For detailed main channel programming information, see the *Control-Channel Programming* section under Applications Information.

General Purpose Input and Output (GPIO)

The MAX96717R provides up to 13 GPIO/GPO/GPI, dependent on device feature utilization. GPIOs are typically used to tunnel low-speed (< 100Kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward or reverse direction. MFP pins can be programmed as GPI, GPO (push-pull output), or ODO (open-drain output).

Each GPIO pin can be configured as an input, output, or input/output by programming the GPIO_TX_EN and GPIO_RX_EN register bits of each GPIO pin. Unwanted loop behavior is avoided for pins configured as input/output (e.g., when the pin is driven by a transition received from the remote side, the driven GPIO transition is not transmitted back). GPIO pins may alternately be controlled and read solely from registers.

Most GPIO pins can be programmed for 1MΩ or 40kΩ pullup or pulldown (or none).

When a GPIO is programmed as GPO, the GPO can generally be programmed for open-drain or push-pull output.

A GPIO packet has 32 possible GPIO channel IDs. Each GPI is mapped to a channel ID according to the GPIO_TX_ID register. On the receiving end, each GPO outputs the received data with a programmed GPIO channel ID corresponding to the GPIO_RX_ID register for that pin. This provides flexibility in determining which GPIO input drives which GPIO output.

GPIO transmissions are transition based; a GPIO packet is created and transmitted on the GMSL2 link when a rising- or falling-edge transition is detected at a GPIO pin. Several GPIO transitions at different GPIO pins can be grouped into a single packet. These pin transitions can be transmitted in two different modes: regular and delay-compensated.

The GPIO channel is not bandwidth efficient and should be used for low-speed signals only. Each GPIO transition uses 40 to 80 bits on the GMSL2 link for transmit and 40 to 60 bits on the reverse (due to received ACK packets). Bandwidth usage values vary based on channel configuration: ARQ enable, CRC enable, and double-header enable all impact channel bandwidth usage.

The state of each GPIO can be read or written by register, either locally or remotely, over the GMSL2 link by a µC using the control-channel I²C interface. In non-delay-compensated mode, channel latency is not fixed. The GPI transition is sent as soon as possible, based on priority and available link bandwidth. This variable delay is a result of multiple communication channels sharing the link. Non-compensated mode should be used with signals tolerant to delay variation (i.e. µC interrupts). Priority can be set for GPI pins using registers. If no priority is set, GPI transitions are transmitted in the order they occur. However, when priority is set, transitions on GPI with higher priority are transmitter sooner.

Typical GMSL2 device delays for forward-link and reverse-link rates are shown in Table 6.

Table 6. Typical GPIO Delays for Forward-Link and Reverse-Link Transmission

DIRECTION	DELAY COMPENSATION	DELAY (µs)
GPIO forwarding from serializer to deserializer	0	1
	1	3.5
GPIO forwarding from deserializer to serializer	0	6
	1	15

Delay in Non-Compensated Mode

In non-compensated mode, the value of the transition is transmitted along with the GPIO channel ID. Note that GPIO channel latency is not fixed; the GMSL2 link has variable delay as a result of multiple communication channels sharing the link. A maximum latency limit is established by the GMSL2 bandwidth-sharing scheme, but significant fluctuation remains. Non-compensated GPIO mode should be used with signals invariant to the delay variations (e.g., µC interrupts).

Delay-Compensated Mode

In delay-compensated mode, a timestamp value is transmitted in addition to the value of the transition and the GPIO channel ID. This timestamp is a high-resolution value sampled by an internal 600MHz clock that records when the GPIO transition is detected at the input. The remote-side chip uses the timestamp value to wait and output the GPIO transition after a total fixed delay from the GPIO input transition. This method mitigates possible variable latency issues by making the total GPIO input-to-output delay a precise, fixed value. Delay-compensated GPIO mode should be used for signals for which the relative timing of rising and falling edges are important (e.g., PWM, camera frame sync, radar ramp trigger, low-speed UART signals).

Frame Sync

In surround-view camera applications a frame-sync signal is usually required by the sensors to synchronize the output of a frame with the other cameras in the system. Most GPIOs can be configured as GPI and linked to a frame-sync signal generated by a surround-view camera electronic control unit (ECU).

Eye-Opening Monitor

The eye-opening monitor (EOM) enables GMSL2 parts to monitor the link margin on an active link and generate an interrupt if it falls below an acceptable level. For example, if a cable is damaged, the link can run error-free, but have less link margin than desired. This allows the customer to react proactively to deteriorating cable performance before any link errors occur. GMSL2 parts can measure the horizontal or vertical eye-opening of the equalizer's output. The measurement is activated automatically at a rate of approximately 1Hz once a link is active. The EOM block compares the data sampled at the center of the eye with a sample offset in phase (for the horizontal EOM) or offset in voltage (for the vertical EOM). An eye-opening figure of merit is then reported. The EOM can trigger an interrupt or a reset if the opening falls below user-defined thresholds.

Other Functions

The MAX96717R serializer has a main I^2C control-channel interface that a µC uses to access serializer and deserializer registers, as well as peripheral devices from either end of the link.

The MAX96717R provides up to 10 GPIOs, dependent on device feature utilization. GPIOs are typically used to tunnel low-speed (< 100Kbps) signals over the GMSL2 link. A GPIO tunnel can be set up in the forward or reverse direction.

The devices include a video crossbar, which can be used to reorder the color and sync signals. It can also be used for D-PHY lane remapping and phase inversion, if desired.

GMSL2 devices incorporate numerous link margin optimization and monitoring functions to ensure a high link margin. Adaptive equalization periodically (~1Hz) optimizes the link margin to adapt to environmental changes and cable aging. An eye-opening monitor function for continuous link margin diagnosis with various threshold alarm levels is available for run-time alerts of link degradation. A PRBS checking function is available to verify the correct link and video-channel operation.

Video PRBS

The video channel of the serializer includes a PRBS pattern generator that operates with bit error verification in the deserializer to test channel operation. The PRBS generator works with the clock received from the source.

To run the video PRBS test, first enable the PRBS generator on the transmitter side, then enable the checker on the receiver side. The PRBS checker automatically syncs itself to the incoming PRBS pattern. If it is unable to sync within a few cycles, it asserts the PRBS_FAIL register. To stop the PRBS test, first, turn the checker off on the receiver side, then turn the generator off on the transmitter side.

PRBS errors can be read from the VPRBS_ERR register on the deserializer side. Any PRBS error causes the ERRB pin to go low in the deserializer by default (see VPRBS_ERR_OEN and VPRBS_ERR_FLAG register bits).

Note: The video channel shares link bandwidth; it is possible to have a bit error on the link which does not cause a video PRBS error.

MIPI CSI-2 Input Interface

Lane Configurations and Data Rates

Image data is received on a unidirectional MIPI CSI-2 v1.3 input port. The port should be configured to use D-PHY v1.2. The interface offers a high degree of flexibility. When configured as D-PHY, the interface supports four differential lanes. To ease the PCB layout, lane swapping is supported independently of how many lanes are used and can only be swapped within that port. Lane polarity swapping within a lane is also supported. Figure 19 shows the options and default mapping. D-PHY mode supports data rates up to 600Mbps per lane.

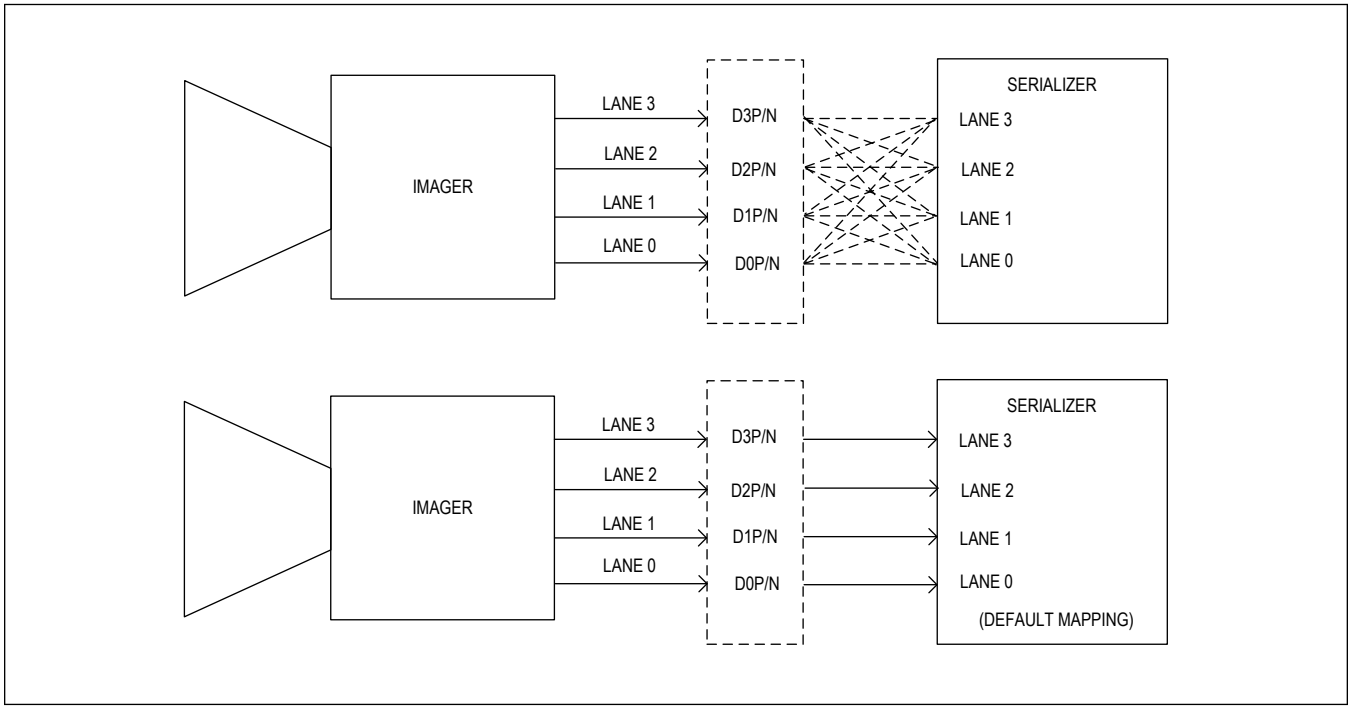


Figure 19. MIPI CSI-2 Lane Mapping Options and Default Settings

Clocking

The device CSI-2 interface supports both continuous and burst-mode clocking in D-PHY mode.

CSI-2 Virtual Channel and Data Type Interleaving

The device supports virtual channels, including virtual channel extension (VCX), introduced in CSI-2 v2.0, enabling up to

4 virtual channels.

If operating in the Pixel mode, the virtual channel and/or data type received from the CSI-2 source can be reassigned (Pixel mode only) or passed through (Pixel and Tunneling modes).

Minimum Blanking

The minimum horizontal blanking period needed by the CSI-2 serializers and deserializers is the maximum of either 40 pixels or 300ns + 370UI (where UI is defined as the period of the CSI-2 lane rate). For most cases, 40 pixels is the larger number. The minimum vertical blanking period is one video line. The minimum vertical front porch is one video line. The recommended vertical back porch is one video line.

The minimum vertical back porch in Pixel mode is the maximum of:

- 40 pixels
- 300ns + 370UI

The minimum vertical back porch in Tunneling mode is the maximum of:

- 40 pixels
- 200 PCLK periods + 233ns, where PCLK = total MIPI data rate/24
- 300ns + 370U

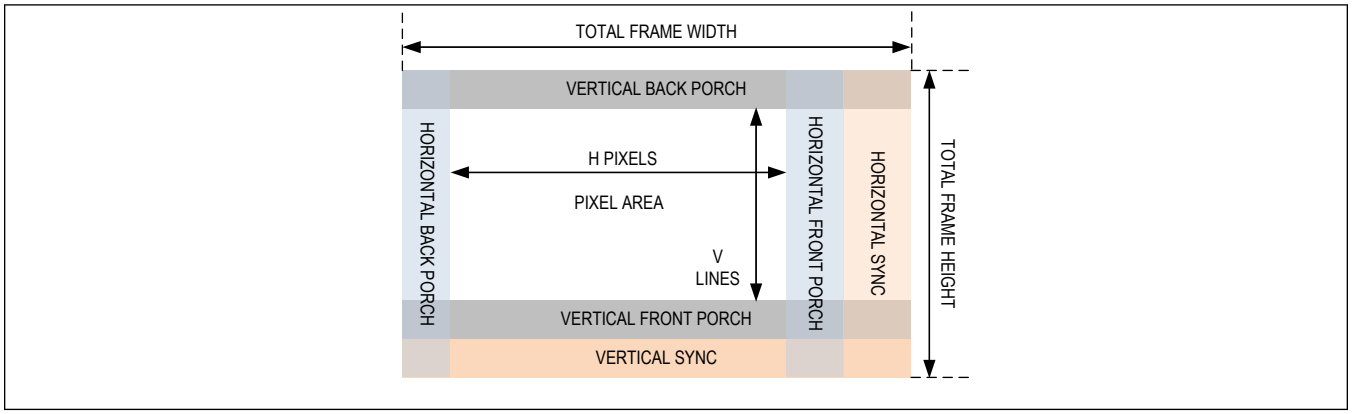


Figure 20. Video Timing

MIPI End-to-End Packet Spacing

When in Tunneling mode, timing requirements must be met to avoid a false line-CRC error flag. As shown in Figure 21, the end-to-end packet spacing (L1, L2, ... LN, LE, LS) must be a minimum of 200 x PCLK cycles + 233ns, where PCLK is the total MIPI data rate/24. This limit is typically a concern for the line-end short packets that follow the last-long data packet of a frame. An alternate solution is to disable the line-CRC check and rely on the MIPI CSI-2 packet CRC, which is a valid verification of error-free data reception.

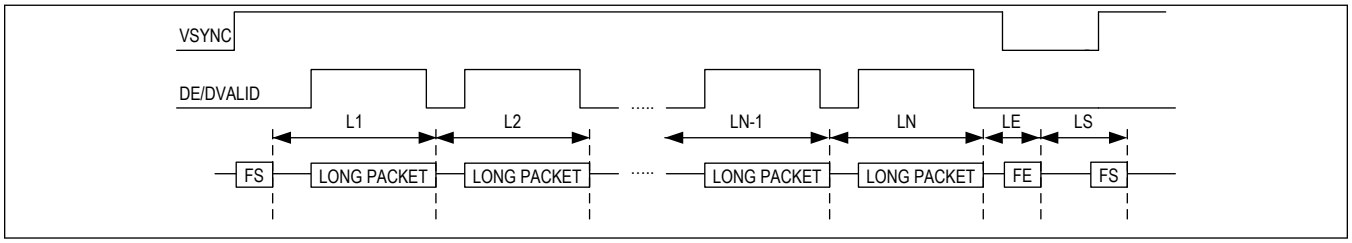


Figure 21. End-to-End Packet Spacing

CFG Latch at Power-up Pins

Voltage levels at the CFG0 and CFG1 pins are latched at power-up or upon a low-to-high transition of PWDNB. These

levels set initial register values and functional modes that may not be easily programmed through I²C after the IC powers up. The CFG pins select I²C address and Tunneling or Pixel mode (see Table 7 and Table 8).

The voltage level for each pin is set by an external precision resistor-divider connected between V_{DD18} and ground or, for some configurations, by a single resistor connected to V_{DD18} or ground. Table 7 and Table 8 show the recommended resistor values to select each configuration. The voltage level at the CFG pins is latched approximately 1ms after all MAX96717R supplies reach the minimum levels required by the POR (power-on-reset) circuit.

If the requirements described in Table 7 and Table 8 are met, the CFG pins can be used as general-purpose outputs or MFP function outputs after the input voltage levels are latched. CFG pins cannot be used as general-purpose inputs.

Table 7. CFG0 Input Map

CFG0 INPUT VOLTAGE SPECIFICATION (% OF V_{DD18}) (NOTES a, b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE) (NOTE c)		MAPPED CONFIGURATION
MIN (%)	TYP (%)	MAX (%)	R1 (kΩ)	R2 (kΩ)	DEVICE ADDRESS
28.8	32.1	35.5	68.1	32.4	0x80
40.7	44.0	47.4	56.2	44.2	0x84

Note a: Resistor divider tolerance, V_{DD18} supply ripple, and external loading must not cause the CFG0 input voltage to exceed the maximum or minimum limits.

Note b: Other than the CFG0 input resistor divider, any load on CFG0 must be ≥ 25 x (R1 + R2).

Note c: Each resistor in the voltage divider must be ≤ 100kΩ.

Table 8. CFG1 Input Map

SPECIFICATION (% OF V_{DD18}) (NOTES a, b)			SUGGESTED RESISTOR VALUES (1% TOLERANCE)		MAPPED CONFIGURATION (NOTE c)
MIN (%)	TYP (%)	MAX (%)	R1 (kΩ)	R2 (kΩ)	TUNNEL/PIXEL MODE
52.6	56.0	59.3	44.2	56.2	Tunnel
88.3	100	100	10	OPEN	Pixel

Note a: Resistor divider tolerance, V_{DD18} supply ripple, and external loading must not cause the CFG1 input voltage to exceed the maximum or minimum limit.

Note b: Other than the CFG1 input resistor divider, any load on CFG1 must be ≥ 25 x (R1 + R2). Each resistor in the voltage-divider must be ≤ 100kΩ.

Multifunction Pin Assignments

Side-channel functions are enabled by programming multifunction pins. Each MFP has several possible functions, but only one can be used at a time.

Some functions require only a single MFP, but most are implemented across a group of MFPs. For example, LOCK is a single MFP, but I²C takes several MFPs. A user selects MFP functions to suit each use case by programming the appropriate registers.

The *Pin Description* table shows default and alternate functions for each MFP, listed in order of priority (highest first). Table 9 also shows priority, left to right, with highest priority on the left. A higher priority function must be disabled before a lower priority function is enabled, both by register writes.

VTG functions represent video-timing generator outputs (VS, HS, PCLK). See the *Video Timing Generator* section and REF_VTG section in the register map for details.

Each MFP defaults to one of four slew rates, with each setting having a default output transition time setting. The transition time default suits the MFP's normal application requirements. Except for ODO__GPI_ functions, whose slew rates are fixed, the transition time of each setting can be changed from the default value through register programming. When the slew rate is changed, the transition time of the MFP is changed.

Transition times depend on the transition time setting. See Table 10 for typical transition times.

Table 9. MFP Pin Function Map

PIN	FUNCTIONS	GPIO	POWER-UP DEFAULT	PIN SLEW DEFAULT (BINARY)
MFP0	VTG0	GPIO0	DISABLED (1MΩ to GND)	10
MFP3	ERRB, LOCK, VTG3	GPIO3	DISABLED (1MΩ to GND)	11
MFP4	RCLKOUT, VTG4	GPIO4	DISABLED (1MΩ to GND)	11
MFP5		ODO5_GPI5	DISABLED (1MΩ to GND)	NA
MFP6		ODO6_GPI6	DISABLED (1MΩ to GND)	NA
MFP7	VTG7	GPIO07	GPI7 (1MΩ to GND)	11
MFP8	ERRB(Alt), VTG8	GPIO08	GPIO8 (BiDir)	11

Table 10. Control- and Side-Channel Typical Rise and Fall Times

PIN SLEW	RISE TIME (ns) (20% to 80%), C_L = 10pF	FALL TIME (ns) (80% to 20%), C_L = 10pF
00	1.0	0.8
01	2.1	2.0
10	4.0	4.3
11	9.0	10.0

Control-Channel Link and Power-Up

GMSL2 ICs are in power-down mode when PWDNB pin is low or when any of the power supplies are down. Register and configurations are set to default reset conditions.

The serializer and deserializer may power up in any order. After all power supplies are up and PWDNB is released, each device starts its power-up sequence and performs the following actions in sequence:

1. Latch at power-up pins register set. Set internal registers according to the selected configuration on CFG0 and CFG1 pins. See Table 7 and Table 8.
2. Control channel (I^2C) is functional on the local side. Device registers are writable and readable.
3. The enabled PHY performs link calibration, equalizer adaptation, and data-channel locking. Once the link is locked, the device sets the LOCK pin high.
4. Control channel is available from remote side.

This entire link up process, from the time the last part's PWDNB input is brought high, takes approximately 35ms for any channels that meet the GMSL2 channel specification.

After the device is linked, it can be configured. This can be done either locally or over the control channel by a µC on either the serializer or deserializer side.

Device Reset

There are three general reset options available through register writes:

- RESET_ALL resets all blocks, including all registers, digital and analog blocks. This is similar to driving the PWDNB pin low and then high.
- Setting RESET_LINK resets all GMSL2 PHY-related digital logic and all data pipelines. After this bit is set, all control registers are still accessible through the local control channel. The link remains in RESET until RESET_LINK is

cleared.

- RESET_ONESHOT resets all GMSL2 PHY-related digital logic and data pipelines, and then automatically clears itself. This is similar to setting and clearing RESET_LINK. (**Note:** For the purposes of achieving predictable and expected link lock time, it is recommended that RESET_ONESHOT is not used while link lock operation is in progress. This includes the initial link lock attempt immediately following power-up. If link lock operation must be interrupted, RESET_LINK should be used instead to hold the link in reset until both SER and DES are ready to establish link lock. RESET_ONESHOT can be used any time after the link has been locked to reset and predictably relock the link.)

Registers that affect GMSL2 link operation (i.e., TX_RATE, RX_RATE, CXTP_A) should be programmed first, followed by RESET_ONESHOT. Alternatively, set these registers when RESET_LINK = 1, and then set RESET_LINK = 0.

Clocking

GMSL Reference Clock

The MAX96717R requires a 25MHz reference clock to generate the 3GHz line-rate clock and associated internal clocks. The MAX96717R can be clocked with an external 25MHz crystal with a frequency accuracy better than ±200ppm.

Reference Clock Generation

The MAX96717R can share a 25MHz crystal by providing a reference clock output. RCLKOUT can be used as a reference clock by another serializer or sensor in close proximity, eliminating the need for an additional external crystal or oscillator in a camera module. A programmable divider divides the reference clock RCLKOUT to be output at 25MHz, 12.5MHz or 6.25MHz. The reference clock is output on the MFP4 pin.

Spread-Spectrum Clocking (SSC)

Analog Devices' GMSL2 links provide exceptional EMI performance. Optional spread-spectrum clocking (SSC) is available to further mitigate EMI caused by the emissions. SSC reduces peaks in the frequency spectrum by spreading the signal over a wider bandwidth. The spread has a 25kHz sawtooth modulation profile, programmable to deviate up to ±1250ppm from the center frequency.

Error and Fault-Condition Monitoring

Both the serializer and deserializer have an open-drain, multipurpose error reporting and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers. So, the reason for assertion of ERRB can be determined by reading the register status.

When relying on the ERRB pin to convey the occurrence of an undervoltage event, connect an external 1MΩ resistor between the ERRB pin and the ground, because ERRB is not a power-up default MFP function. As a result, following a reset that is triggered by an undervoltage event, the ERRB MFP pin transitions through high-impedance states. During an error state, the host device expects ERRB to drive logic-low, and the presence of the external 1MΩ resistor enables the appropriate logic level to be maintained following the reset, alerting the host device that attention is required.

Power Supplies

The supply voltages for the MAX96717R can be brought up in any order. An on-chip power manager ensures that all supply rails are within limits before enabling device startup.

The serializer core runs on a regulated 1.0V supply (CAP_VDD) that is supplied from a built-in LDO that regulates the voltage received on the V_{DD} pin down to 1.0V. CAP_VDD also powers the output driver for the GMSL forward channel.

V_{DD18} is the analog and I/O supply. Connect to 1.8V. Power supply ramp time recommendation is 20µs < ramp time < 2ms. The power supply ramp should be monotonic. Once the supply has reached the minimum supply voltage limit, it should not be allowed to drop below the specification.

Proper bypassing of power supplies is essential for high-frequency circuit performance. See Table 3 and Table 2 for power supply tolerances and noise requirements. Contact the factory for guidance on sharing supplies and optimizing supply decoupling.

Analog Devices provides power management ICs (PMICs) optimized for supporting serial link devices. Contact the factory for information.

PCB Layout Guidelines for GMSL

Proper circuit board design techniques are required for optimal GMSL link performance. This includes having at least a four-layer board to provide a proper ground plane reference, low thermal impedance, DC supply pin bypassing, PoC design, and high-speed GMSL trace impedance matching.

Ground Plane

A consistent ground plane, generally the second layer, is recommended to provide isolation from the high-speed GMSL traces and other traces and components that can couple noise onto the GMSL signals. This also simplifies the design of impedance-matched transmission lines. The ground plane is also key to provide a low thermal impedance to the device's exposed paddle.

High-Speed GMSL Traces

Proper transmission line design techniques are needed to achieve optimal GMSL link performance. The characteristic impedance must be closely matched to the desired impedance (50Ω single-ended). Any mismatch increases insertion loss and causes reflections (degrade return-loss). Use the following suggested layout practices:

- Use only 50Ω single-ended traces.
- Minimize length of high-speed traces.
- Minimize pad stubs by placing component pads directly on the signal trace.
- Use ground cutouts under pads as required (1.3x area of pad).
- Follow vendor layout recommendations for components, including connectors.
- Avoid sharp bends on high-speed traces.
- Place AC coupling capacitors within 500 mils (12mm) of the SIOx pins.
- Place the GMSL device as close to the serial-link connector as possible to minimize insertion loss.
- Stitch ground layers together with vias near high-speed traces.

Power-over-Coax (PoC) Layout

When used, the PoC circuit needs to provide a low DC series resistance to the power supply while minimizing the loading of the GMSL forward and reverse signals. The PoC circuit behaves as a bias-tee and requires proper layout techniques for optimal GMSL link performance, including:

- Placing the smallest valued inductor (highest self resonant frequency) on the GMSL signal trace.
- Placing the next smallest valued inductor after the smallest.
- Using ground cutouts as needed under the first two inductors and resistors. See Figure 22.
- Placing the PoC within 1/2 UI of the device, particularly for the deserializer.

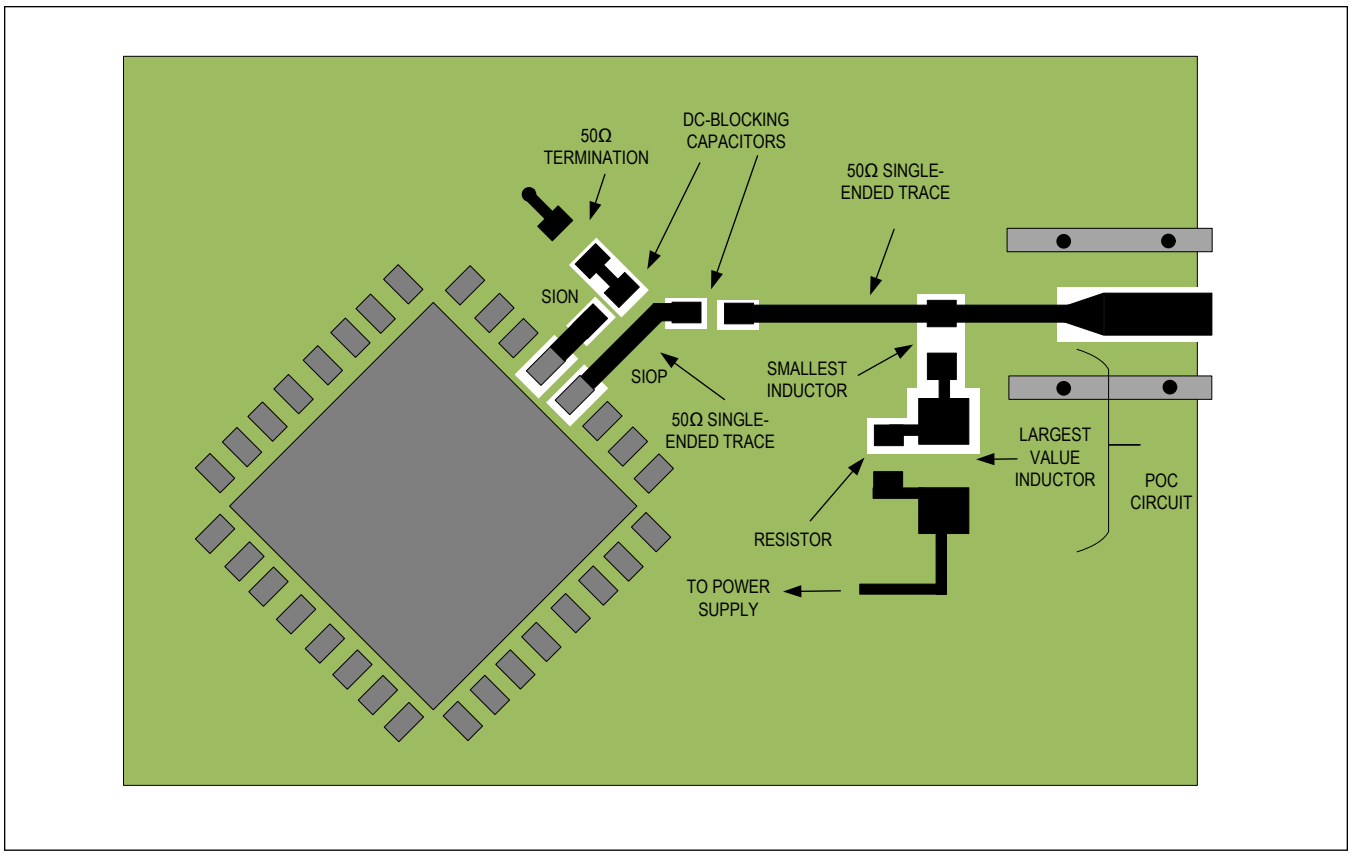


Figure 22. Coax PoC Layout Example

Thermal Management

Power consumption of GMSL2 devices varies based on use case. The user must take care to provide sufficient heat dissipation with proper board and cooling design techniques. The exposed pad of the package must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below +125°C to avoid impacting device reliability.

Refer to *Thermal Characterization of IC Packages* for further guidance.

Applications Information

Software Programming Model

Analog Devices' automotive serializers and deserializers are designed to follow a general software programming model. Except for features that require in-operation control channel accesses, such as the ASIL safety measures and interrupt handling, use the following programming model:

1. Set the impacted functional blocks to disabled or reset mode. A general method used to place the part in IDLE state is to stop all side-channel and video traffic, followed by a register write (RESET_LINK = 1) to stop the GMSL link.
2. The settings for each feature must be fully configured before it is enabled.
3. Establish the link by setting RESET_LINK = 0. Wait for the link to lock.
4. Start video and side-channel traffic.

If changing the configuration of a feature is required during the operation of other features, disable the feature that will be reconfigured, change its settings, and reenable it.

Programming Notes

The MAX96717R has no mandatory register writes on startup.

Control Channel Programming

GMSL device registers can only be accessed and configured through the I^2C interface. By default, the I^2C control channel is also sent to the remote side device and any peripheral connections. This allows control of the GMSL devices from either end of the link. For multimaster configurations, with microcontrollers connected to both the serializer and deserializer, disabling the remote control channel through register settings is recommended to prevent bus contention.

The I^2C interface uses clock stretching (holding SCL low) to account for timing differences between master and slave. It also allows time for data to be forwarded and received across the serial link. All local side I^2C devices must support clock stretching by the GMSL2 device. Remote side I^2C devices are not required to support clock stretching.

SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL.

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address, plus a R/W bit, register address bytes, 1 or more data bytes, and a STOP condition.

Register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address autoincrements).

Device Address

Each device on the I^2C control channel must have a unique address. The GMSL2 device address is set to one of several 7-bit addresses according to the voltage level of the CFG pins at power-up (see Table 7 and Table 8). Note that a device address can be changed after power-up by writing to the DEV_ADDR register.

I^2C Programming

Each device has an internal I^2C slave for register access. The internal registers can be written and read according to the I^2C protocol using the packet formats below.

I^2C Write Packet Format

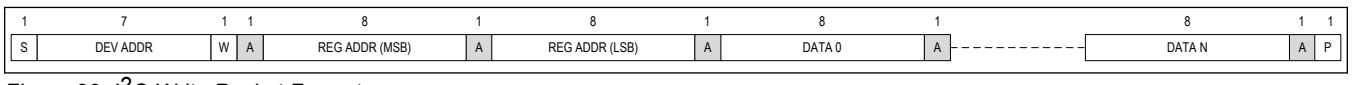


Figure 23. I^2C Write Packet Format

I²C Read Packet Format

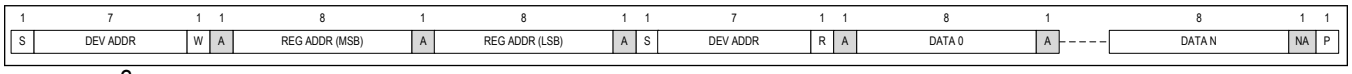
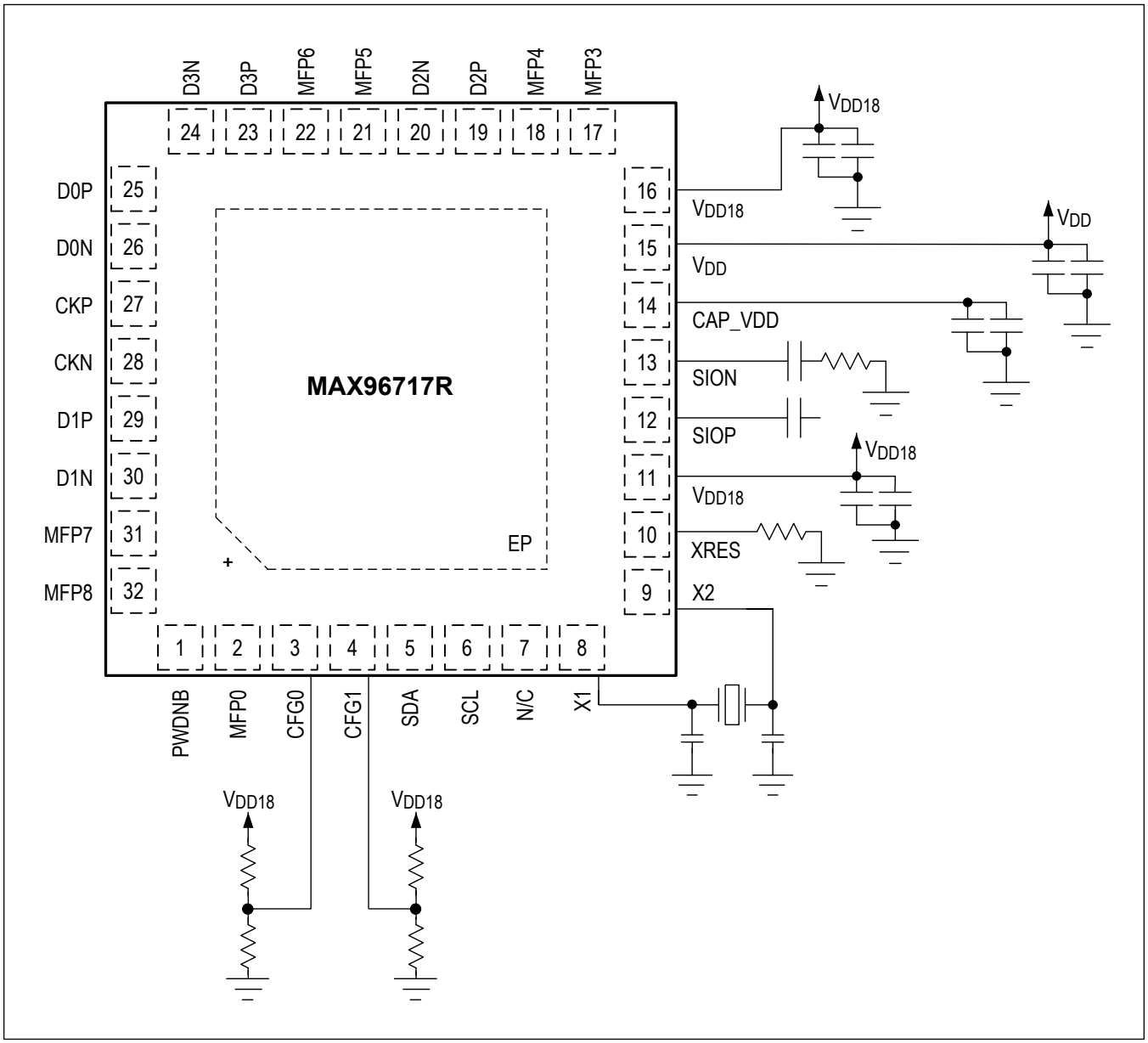


Figure 24. I²C Read Packet Format

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX96717RGTJ/V+	-40°C to +105°C	32 TQFN-EP	MAXIM
MAX96717RGTJ/V+T	-40°C to +105°C	32 TQFN-EP	MAXIM

+ Denotes a lead(Pb)-free/RoHS-compliant package.

/V Denotes automotive qualified.

T Denotes tape-and-reel.

Register Map

MAX96717R

Not all register bits in the register space are shown in the register table. Any bit not explicitly defined in the register table should be treated as reserved and not modified. When a write is required to a register with both defined and undefined register bits, first read the register's contents, then create a new register value by only changing the defined bits. Finally, write the new byte to the register (Read/Replace/Write).

Default values are provided for read-only register bits. Read-only bit states are changed at power-up according to the actual state of the device. To avoid overwriting these bits, treat read-only bits as undefined.

Note: See the Programming Notes section for mandatory register writes on startup.

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x80	REG0[7:0]	DEV_ADDR[6:0]							CFG_BLOCK
0x01	0x08	REG1[7:0]	RSVD	RSVD	DIS_LOCAL_CC	DIS_REM_CC	RSVD[1:0]		RSVD[1:0]	
0x02	0x43	REG2[7:0]	–	VID_TX_EN_Z	–	–	–	–	RSVD	RSVD
0x05	0x00	REG5[7:0]	LOCK_EN	ERRB_EN	ALT_LOCK_EN	ALT_ERRB_EN	RSVD	RSVD	RSVD	RSVD
0x06	0x80	REG6[7:0]	RSVD	–	RCLKEN	RSVD	–	–	–	RSVD
0x0D	0xB7	REG13[7:0]	DEV_ID[7:0]							
0x0E	0x04	REG14[7:0]	RSVD[3:0]				DEV_REV[3:0]			
OVERLAP										
TCTRL										
0x0C	0x15	PWR4[7:0]	RSVD	DIS_LOCAL_WAKE	–	WAKE_EN_A	RSVD[3:0]			
0x10	0x01	CTRL0[7:0]	RESET_ALL	RESET_LINK	RESET_ONESHOT	RSVD	RSVD	–	RSVD[1:0]	
0x12	0x04	CTRL2[7:0]	RSVD	RSVD	–	LDO_BYPASS	RSVD[1:0]		RSVD[1:0]	
0x13	0x10	CTRL3[7:0]	RSVD	RSVD	RSVD[1:0]		LOCKED	ERROR	CMU_LOCKED	–
0x18	0xA0	INTR0[7:0]	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
0x19	0x00	INTR1[7:0]	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	RSVD[2:0]		
0x1A	0x09	INTR2[7:0]	RSVD	RSVD	REM_ERR_OEN	–	RSVD	IDLE_ERR_OEN	–	DEC_ERR_OEN_A
0x1B	0x00	INTR3[7:0]	RSVD	RSVD	REM_ERR_FLAG	–	RSVD	IDLE_ERR_FLAG	–	DEC_ERR_FLAG_A

ADDRESS	RESET	NAME	MSB							LSB
0x1C	0x08	INTR4[7:0]	RSVD	EOM_ERR_OEN_A	RSVD	RSVD	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	–
0x1D	0x00	INTR5[7:0]	RSVD	EOM_ERR_FLAG_A	RSVD	RSVD	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	–
0x1E	0xFB	INTR6[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	MIPI_ERR_OEN
0x1F	0x00	INTR7[7:0]	RSVD	RSVD	RSVD	EFUSE_CRC_ERR	RSVD	RSVD	RSVD	MIPI_ERR_FLAG
0x20	0x9F	INTR8[7:0]	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x21	0xDF	INTR9[7:0]	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
0x22	0x00	CNT0[7:0]	DEC_ERR_A[7:0]							
0x24	0x00	CNT2[7:0]	IDLE_ERR[7:0]							
0x25	0x00	CNT3[7:0]	PKT_CNT[7:0]							
GMSL										
0x29	0x08	TX1[7:0]	LINK_PRBS_GEN	RSVD	–	ERRG_EN_A	RSVD	–	DIS_SCR	DIS_ENC
0x2A	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x2D	0x28	RX1[7:0]	LINK_PRBS_CHK	–	RSVD[1:0]		RSVD[1:0]		RSVD	RSVD
0x30	0x41	GPIOA[7:0]	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
0x31	0x88	GPIOB[7:0]	RSVD[1:0]		GPIO_REV_CDLY[5:0]					
CC										
0x40	0x26	I2C_0[7:0]	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
0x41	0x56	I2C_1[7:0]	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
0x42	0x00	I2C_2[7:0]	SRC_A[6:0]							–
0x43	0x00	I2C_3[7:0]	DST_A[6:0]							–
0x44	0x00	I2C_4[7:0]	SRC_B[6:0]							–
0x45	0x00	I2C_5[7:0]	DST_B[6:0]							–
CFGV VIDEO_Z										
0x58	0x30	TX0[7:0]	TX_CRC_EN	–	RSVD[1:0]		RSVD[1:0]		RSVD[1:0]	
0x5B	0x02	TX3[7:0]	–	–	–	–	–	–	TX_STR_SEL[1:0]	
CFGI INFOFR										
0x78	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		RSVD[1:0]		RSVD[1:0]	
0x7B	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x7C	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
CFGL GPIO										
0x90	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		RSVD[1:0]		RSVD[1:0]	
0x93	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		

ADDRESS	RESET	NAME	MSB							LSB
0x94	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0x95	0x98	ARQ0[7:0]	RSVD	RSVD	RSVD	RSVD	ARQ0_EN	DIS_DBL_ACK_RETX	–	–
0x96	0x72	ARQ1[7:0]	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
0x97	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
VID_TX Z										
0x110	0x68	VIDEO_TX0[7:0]	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		AUTO_BPP	CLKDET_BYP	RSVD[1:0]	
0x111	0x58	VIDEO_TX1[7:0]	RSVD[1:0]		BPP[5:0]					
0x112	0x0A	VIDEO_TX2[7:0]	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
VTX Z										
0x236	0x00	CROSS_0[7:0]	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
0x237	0x01	CROSS_1[7:0]	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
0x238	0x02	CROSS_2[7:0]	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
0x239	0x03	CROSS_3[7:0]	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
0x23A	0x04	CROSS_4[7:0]	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
0x23B	0x05	CROSS_5[7:0]	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
0x23C	0x06	CROSS_6[7:0]	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
0x23D	0x07	CROSS_7[7:0]	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
0x23E	0x08	CROSS_8[7:0]	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
0x23F	0x09	CROSS_9[7:0]	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
0x240	0x0A	CROSS_10[7:0]	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
0x241	0x0B	CROSS_11[7:0]	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
0x242	0x0C	CROSS_12[7:0]	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
0x243	0x0D	CROSS_13[7:0]	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
0x244	0x0E	CROSS_14[7:0]	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
0x245	0x0F	CROSS_15[7:0]	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x246	0x10	CROSS_16[7:0]	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
0x247	0x11	CROSS_17[7:0]	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
0x248	0x12	CROSS_18[7:0]	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
0x249	0x13	CROSS_19[7:0]	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
0x24A	0x14	CROSS_20[7:0]	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
0x24B	0x15	CROSS_21[7:0]	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
0x24C	0x16	CROSS_22[7:0]	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
0x24D	0x17	CROSS_23[7:0]	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
0x24E	0x03	VTX0[7:0]	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
0x24F	0x01	VTX1[7:0]	–	–	PCLKDET_VTX	–	PATGEN_CLK_SRC[2:0]			VS_TRIG
0x250	0x00	VTX2[7:0]	VS_DLY_2[7:0]							
0x251	0x00	VTX3[7:0]	VS_DLY_1[7:0]							
0x252	0x00	VTX4[7:0]	VS_DLY_0[7:0]							
0x253	0x00	VTX5[7:0]	VS_HIGH_2[7:0]							
0x254	0x00	VTX6[7:0]	VS_HIGH_1[7:0]							
0x255	0x00	VTX7[7:0]	VS_HIGH_0[7:0]							
0x256	0x00	VTX8[7:0]	VS_LOW_2[7:0]							
0x257	0x00	VTX9[7:0]	VS_LOW_1[7:0]							
0x258	0x00	VTX10[7:0]	VS_LOW_0[7:0]							
0x259	0x00	VTX11[7:0]	V2H_2[7:0]							
0x25A	0x00	VTX12[7:0]	V2H_1[7:0]							
0x25B	0x00	VTX13[7:0]	V2H_0[7:0]							
0x25C	0x00	VTX14[7:0]	HS_HIGH_1[7:0]							
0x25D	0x00	VTX15[7:0]	HS_HIGH_0[7:0]							
0x25E	0x00	VTX16[7:0]	HS_LOW_1[7:0]							
0x25F	0x00	VTX17[7:0]	HS_LOW_0[7:0]							
0x260	0x00	VTX18[7:0]	HS_CNT_1[7:0]							
0x261	0x00	VTX19[7:0]	HS_CNT_0[7:0]							
0x262	0x00	VTX20[7:0]	V2D_2[7:0]							
0x263	0x00	VTX21[7:0]	V2D_1[7:0]							
0x264	0x00	VTX22[7:0]	V2D_0[7:0]							
0x265	0x00	VTX23[7:0]	DE_HIGH_1[7:0]							
0x266	0x00	VTX24[7:0]	DE_HIGH_0[7:0]							
0x267	0x00	VTX25[7:0]	DE_LOW_1[7:0]							
0x268	0x00	VTX26[7:0]	DE_LOW_0[7:0]							
0x269	0x00	VTX27[7:0]	DE_CNT_1[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x26A	0x00	VTX28[7:0]	DE_CNT_0[7:0]							
0x26B	0x00	VTX29[7:0]	VID_PRBS_EN	RSVD	VPRBS_FAIL	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
0x26C	0x04	VTX30[7:0]	GRAD_INC[7:0]							
0x26D	0x00	VTX31[7:0]	CHKR_A_L[7:0]							
0x26E	0x00	VTX32[7:0]	CHKR_A_M[7:0]							
0x26F	0x00	VTX33[7:0]	CHKR_A_H[7:0]							
0x270	0x00	VTX34[7:0]	CHKR_B_L[7:0]							
0x271	0x00	VTX35[7:0]	CHKR_B_M[7:0]							
0x272	0x00	VTX36[7:0]	CHKR_B_H[7:0]							
0x273	0x00	VTX37[7:0]	CHKR_RPT_A[7:0]							
0x274	0x00	VTX38[7:0]	CHKR_RPT_B[7:0]							
0x275	0x00	VTX39[7:0]	CHKR_ALT[7:0]							
0x276	0x18	VTX40[7:0]	RSVD	CROSSHS_I	CROSSHS_F	CROSSHS[4:0]				
0x277	0x19	VTX41[7:0]	–	CROSSVS_I	CROSSVS_F	CROSSVS[4:0]				
0x278	0x1A	VTX42[7:0]	–	CROSSDE_I	CROSSDE_F	CROSSDE[4:0]				
GPIO0 0										
0x2BE	0x99	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2BF	0xA0	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C0	0x40	GPIO_C[7:0]	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO3 3										
0x2C7	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2C8	0xA3	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2C9	0x43	GPIO_C[7:0]	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO4 4										
0x2CA	0x99	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2CB	0xA4	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2CC	0x44	GPIO_C[7:0]	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO5 5										
0x2CD	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2CE	0xA5	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
0x2CF	0x45	GPIO_C[7:0]	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
GPIO6 6										
0x2D0	0x99	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D1	0xA6	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
0x2D2	0x46	GPIO_C[7:0]	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO7 7										
0x2D3	0x83	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D4	0xA7	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D5	0x47	GPIO_C[7:0]	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
GPIO8 8										
0x2D6	0x9C	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x2D7	0x28	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x2D8	0x48	GPIO_C[7:0]	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
FRONTTOP										
0x308	0x64	FRONTTOP_0[7:0]	RSVD	enable_line_info	START_PORTB	–	–	RSVD	–	–
0x30D	0xFF	FRONTTOP_5[7:0]	VC_SELZ_L[7:0]							
0x30E	0xFF	FRONTTOP_6[7:0]	VC_SELZ_H[7:0]							
0x311	0x40	FRONTTOP_9[7:0]	–	START_PORTBZ	–	–	–	–	–	–
0x312	0x00	FRONTTOP_10[7:0]	–	RSVD	–	–	–	bpp8dblz	–	–
0x313	0x00	FRONTTOP_11[7:0]	–	bpp12dblz	–	–	–	bpp10dblz	–	–
0x318	0x00	FRONTTOP_16[7:0]	–	mem_dt1_selz[6:0]						
0x319	0x00	FRONTTOP_17[7:0]	–	mem_dt2_selz[6:0]						
0x31E	0x18	FRONTTOP_22[7:0]	soft_dtz_en	soft_vcz_en	soft_bppz_en	soft_bppz[4:0]				
0x320	0x00	FRONTTOP_24[7:0]	–	–	soft_vcz[1:0]		–	–	–	–
0x323	0x30	FRONTTOP_27[7:0]	–	–	soft_dtz[5:0]					
0x325	0x00	FRONTTOP_29[7:0]	FORCE_START_MIPI_FRONTTOP	–	–	–	–	–	–	–

ADDRESS	RESET	NAME	MSB							LSB
MIPI_RX										
0x330	0x00	MIPI_RX0[7:0]	–	mipi_noncontclk_en	ctrl1_vc_map_en	–	mipi_rx_reset	RSVD[2:0]		
0x331	0x30	MIPI_RX1[7:0]	RSVD	RSVD	ctrl1_num_lanes[1:0]		–	–	–	–
0x332	0xE0	MIPI_RX2[7:0]	phy1_lane_map[3:0]				–	–	–	–
0x333	0x04	MIPI_RX3[7:0]	–	–	–	–	phy2_lane_map[3:0]			
0x334	0x00	MIPI_RX4[7:0]	–	phy1_pol_map[2:0]			–	–	–	–
0x335	0x00	MIPI_RX5[7:0]	–	–	–	–	–	phy2_pol_map[2:0]		
0x337	0x00	MIPI_RX7[7:0]	–	–	RSVD	RSVD[4:0]				
0x338	0x55	MIPI_RX8[7:0]	RSVD[1:0]		t_hs_settle[1:0]		RSVD[1:0]	t_clk_settle[1:0]		
0x33B	0x00	MIPI_RX11[7:0]	–	–	–	phy1_lp_err[4:0]				
0x33C	0x00	MIPI_RX12[7:0]	phy1_hs_err[7:0]							
0x33D	0x00	MIPI_RX13[7:0]	–	–	–	phy2_lp_err[4:0]				
0x33E	0x00	MIPI_RX14[7:0]	phy2_hs_err[7:0]							
0x343	0x00	MIPI_RX19[7:0]	ctrl1_csi_err_l[7:0]							
0x344	0x00	MIPI_RX20[7:0]	–	–	–	–	–	ctrl1_csi_err_h[2:0]		
0x345	0x00	MIPI_RX21[7:0]	ctrl1_vc_map0[3:0]				–	–	–	–
0x346	0x00	MIPI_RX22[7:0]	ctrl1_vc_map1[3:0]				–	–	–	–
0x347	0x00	MIPI_RX23[7:0]	ctrl1_vc_map2[3:0]				–	–	–	–
0x36C	0x00	MIPI_RX60[7:0]	ctrl1_vc_map3[3:0]				–	–	–	–
MIPI_RX_EXT										
0x383	0x80	EXT11[7:0]	Tun_Mode	RSVD	–	–	RSVD	RSVD	RSVD[1:0]	
0x38D	0x00	EXT21[7:0]	phy1_pkt_cnt[7:0]							
0x38E	0x00	EXT22[7:0]	csi1_pkt_cnt[7:0]							
0x38F	0x00	EXT23[7:0]	tun_pkt_cnt[7:0]							
0x390	0x00	EXT24[7:0]	phy_clk_cnt[7:0]							
FRONTTOP_EXT										
0x3C8	0x00	FRONTTOP_EXT8[7:0]	mem_dt3_selz[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x3C9	0x00	FRONTTOP_EXT9[7:0]	mem_dt4_selz[7:0]							
0x3CA	0x00	FRONTTOP_EXT10[7:0]	mem_dt5_selz[7:0]							
0x3CB	0x00	FRONTTOP_EXT11[7:0]	mem_dt6_selz[7:0]							
0x3D1	0x00	FRONTTOP_EXT17[7:0]	–	–	–	–	mem_dt6_selz_en	mem_dt5_selz_en	mem_dt4_selz_en	mem_dt3_selz_en
MIPI_RX_EXT2										
0x3DC	0x00	EXTA[7:0]	–	mem_dt7_selz[6:0]						
0x3DD	0x00	EXTB[7:0]	–	mem_dt8_selz[6:0]						
REF_VTG										
0x3E0	0x70	VTX0[7:0]	–	VS_TRIG	REF_VTG_MODE[1:0]		HS_INV	GEN_HS	VS_INV	GEN_VS
0x3E1	0x00	VTX1[7:0]	VS_HIGH_2[7:0]							
0x3E2	0x00	VTX2[7:0]	VS_HIGH_1[7:0]							
0x3E3	0x00	VTX3[7:0]	VS_HIGH_0[7:0]							
0x3E4	0x00	VTX4[7:0]	VS_LOW_2[7:0]							
0x3E5	0x00	VTX5[7:0]	VS_LOW_1[7:0]							
0x3E6	0x00	VTX6[7:0]	VS_LOW_0[7:0]							
0x3E7	0x00	VTX7[7:0]	V2H_2[7:0]							
0x3E8	0x00	VTX8[7:0]	V2H_1[7:0]							
0x3E9	0x00	VTX9[7:0]	V2H_0[7:0]							
0x3EA	0x00	VTX10[7:0]	HS_HIGH_1[7:0]							
0x3EB	0x00	VTX11[7:0]	HS_HIGH_0[7:0]							
0x3EC	0x00	VTX12[7:0]	HS_LOW_1[7:0]							
0x3ED	0x00	VTX13[7:0]	HS_LOW_0[7:0]							
0x3EE	0x00	VTX14[7:0]	HS_CNT_1[7:0]							
0x3EF	0x00	VTX15[7:0]	HS_CNT_0[7:0]							
0x3F1	0x00	REF_VTG1[7:0]	RCLKEN_Y	–	PCLK_GPIO[4:0]					PCLKEN
0x3F2	0x00	REF_VTG2[7:0]	–	–	HS_GPIO[4:0]					HSEN
0x3F3	0x00	REF_VTG3[7:0]	–	–	VS_GPIO[4:0]					VSEN
0x3F6	0x00	REF_VTG6[7:0]	VS_DLY_2[7:0]							
0x3F7	0x00	REF_VTG7[7:0]	VS_DLY_1[7:0]							
0x3F8	0x00	REF_VTG8[7:0]	VS_DLY_0[7:0]							
0x3F9	0x1E	REF_VTG9[7:0]	REF_VTG_TRIG_EN	–	–	REF_VTG_TRIG_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
MISC										
0x55F	0x00	HS_VS_Z[7:0]	–	DE_DET_Z	VS_DET_Z	HS_DET_Z	–	–	VS_POL_Z	HS_POL_Z
0x56F	0x3E	PIO_SLEW_0[7:0]	–	–	PIO02_SLEW[1:0]		PIO01_SLEW[1:0]		PIO00_SLEW[1:0]	
0x570	0x3C	PIO_SLEW_1[7:0]	–	–	PIO06_SLEW[1:0]		PIO05_SLEW[1:0]		–	–
0x571	0xFC	PIO_SLEW_2[7:0]	PIO011_SLEW[1:0]		PIO010_SLEW[1:0]		RSVD[1:0]		–	–
MIPI_RX_EXT3										
0x584	0x00	EXT4[7:0]	ctrl1_fs_cnt_l[7:0]							
0x585	0x00	EXT5[7:0]	ctrl1_fs_cnt_h[7:0]							
0x586	0x00	EXT6[7:0]	ctrl1_fe_cnt_l[7:0]							
0x587	0x00	EXT7[7:0]	ctrl1_fe_cnt_h[7:0]							
0x588	0x00	EXT8[7:0]	–	–	–	–	ctrl1_fs_vc_sel[3:0]			
RLMS A										
0x1404	0x4B	RLMS4[7:0]	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
0x1405	0x10	RLMS5[7:0]	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
0x1406	0x80	RLMS6[7:0]	EOM_PV_MODE	RSVD[6:0]						
0x1407	0x00	RLMS7[7:0]	EOM_DONE	EOM[6:0]						
0x143A	0x00	RLMS3A[7:0]	EyeMonValCntL[7:0]							
0x143B	0x00	RLMS3B[7:0]	EyeMonValCntH[7:0]							
0x1464	0x90	RLMS64[7:0]	RSVD[3:0]				–	RSVD	TxSSCMode[1:0]	
0x1470	0x01	RLMS70[7:0]	–	TxSSCFrqCtrl[6:0]						
0x1471	0x02	RLMS71[7:0]	–	TxSSCCenSprSt[5:0]						TxSSCEn
0x1472	0xCF	RLMS72[7:0]	TxSSCPreSclL[7:0]							
0x1473	0x00	RLMS73[7:0]	–	–	–	–	–	TxSSCPreSclH[2:0]		
0x1474	0x00	RLMS74[7:0]	TxSSCPhL[7:0]							
0x1475	0x00	RLMS75[7:0]	–	TxSSCPhH[6:0]						
0x1476	0x00	RLMS76[7:0]	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
0x14A8	0x00	RLMSA8[7:0]	FW_PHY_CTRL	FW_PHY_PU_TX	FW_PHY_RSTB	RSVD	RSVD	RSVD	RSVD	RSVD
0x14A9	0x00	RLMSA9[7:0]	FW_REPCAL_RSTB	RSVD	FW_TXD_SQUELCH	FW_TXD_EN	FW_RXD_EN	RSVD	RSVD	RSVD
EFUSE										
0x1C50	0x00	EFUSE80[7:0]	SERIAL_NUMBER_0[7:0]							
0x1C51	0x00	EFUSE81[7:0]	SERIAL_NUMBER_1[7:0]							
0x1C52	0x00	EFUSE82[7:0]	SERIAL_NUMBER_2[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x1C53	0x00	EFUSE83[7:0]	SERIAL_NUMBER_3[7:0]							
0x1C54	0x00	EFUSE84[7:0]	SERIAL_NUMBER_4[7:0]							
0x1C55	0x00	EFUSE85[7:0]	SERIAL_NUMBER_5[7:0]							
0x1C56	0x00	EFUSE86[7:0]	SERIAL_NUMBER_6[7:0]							
0x1C57	0x00	EFUSE87[7:0]	SERIAL_NUMBER_7[7:0]							
0x1C58	0x00	EFUSE88[7:0]	SERIAL_NUMBER_8[7:0]							
0x1C59	0x00	EFUSE89[7:0]	SERIAL_NUMBER_9[7:0]							
0x1C5A	0x00	EFUSE90[7:0]	SERIAL_NUMBER_10[7:0]							
0x1C5B	0x00	EFUSE91[7:0]	SERIAL_NUMBER_11[7:0]							
0x1C5C	0x00	EFUSE92[7:0]	SERIAL_NUMBER_12[7:0]							
0x1C5D	0x00	EFUSE93[7:0]	SERIAL_NUMBER_13[7:0]							
0x1C5E	0x00	EFUSE94[7:0]	SERIAL_NUMBER_14[7:0]							
0x1C5F	0x00	EFUSE95[7:0]	SERIAL_NUMBER_15[7:0]							
0x1C60	0x00	EFUSE96[7:0]	SERIAL_NUMBER_16[7:0]							
0x1C61	0x00	EFUSE97[7:0]	SERIAL_NUMBER_17[7:0]							
0x1C62	0x00	EFUSE98[7:0]	SERIAL_NUMBER_18[7:0]							
0x1C63	0x00	EFUSE99[7:0]	SERIAL_NUMBER_19[7:0]							
0x1C64	0x00	EFUSE100[7:0]	SERIAL_NUMBER_20[7:0]							
0x1C65	0x00	EFUSE101[7:0]	SERIAL_NUMBER_21[7:0]							
0x1C66	0x00	EFUSE102[7:0]	SERIAL_NUMBER_22[7:0]							
0x1C67	0x00	EFUSE103[7:0]	SERIAL_NUMBER_23[7:0]							

Register Details

REG0 (0x0)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b1000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	Device Address Default value is set by the CFG0 pin as follows: CFG0 Device Address 000 0b1000000 001 0b1000010 010 0b1000000 011 0b1000010 100 0b1000010 101 0b1000000 110 0b1000010 111 0b1000000	0b0000000: I2C write/read address is 0x00/0x01 0b0000001: I2C write/read address is 0x02/0x03 ... ... 0b1000000: I2C write/read address is 0x80/0x81 0b1000010: I2C write/read address is 0x84/0x85 0b1000100: I2C write/read address is 0x88/0x89 0b1100000: I2C write/read address is 0xC0/0xC1 0b1100010: I2C write/read address is 0xC4/0xC5 0b1100100: I2C write/read address is 0xC8/0xC9 0b0100000: I2C write/read address is 0x40/0x41 0b0100010: I2C write/read address is 0x44/0x45 ... ... 0b1111111: I2C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block When set, all registers become non-writable (read-only). This bit can be used to freeze the chip configuration. The only way to clear this register and regain write access is with a power cycle or toggling the PWDNB pin.	0b0: Not Blocked 0b1: Blocked

REG1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	DIS_LOCAL_CC	DIS_REM_CC	RSVD[1:0]		RSVD[1:0]	
Reset	0b0	0b0	0b0	0b0	0b10		0b00	
Access Type			Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_CC	5	Disable control-channel connection to RX/SDA and TX/SCL pins	0b0: RX/SDA and TX/XCL connected to control channel 0b1: RX/SDA and TX/SCL disconnected from control channel
DIS_REM_CC	4	Disable access to remote device control-channel over GMSL connection	0b0: Remote control channel enabled 0b1: Remote control channel disabled

REG2 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	–	VID_TX_EN_Z	–	–	–	–	RSVD	RSVD
Reset	–	0b1	–	–	–	–	0b1	0b1
Access Type	–	Write, Read	–	–	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
VID_TX_EN_Z	6	Video Transmit Enable for Video Pipe Z	0b0: Video transmit Pipe Z disabled 0b1: Video transmit Pipe Z enabled

REG5 (0x5)

BIT	7	6	5	4	3	2	1	0
Field	LOCK_EN	ERRB_EN	ALT_LOCK_EN	ALT_ERRB_EN	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_EN	7	Enable LOCK Output	0b0: LOCK output disabled 0b1: LOCK output enabled
ERRB_EN	6	Enable ERRB Output	0b0: ERRB output disabled 0b1: ERRB output enabled
ALT_LOCK_EN	5	Enable LOCK output on alternate output	0b0: LOCK output disabled 0b1: LOCK output enabled
ALT_ERRB_EN	4	Enable ERRB output on alternate output	0b0: ERRB output disabled 0b1: ERRB output enabled

REG6 (0x6)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	RCLKEN	RSVD	–	–	–	RSVD
Reset	0b1	–	0b0	0b0	–	–	–	0b0
Access Type		–	Write, Read		–	–	–	

BITFIELD	BITS	DESCRIPTION	DECODE
RCLKEN	5	Enable/disable RCLK Output.	0b0: RCLK output is disabled 0b1: RCLK output is enabled

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0xB7							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device Identifier	0xC8: MAX96717R

REG14 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				DEV_REV[3:0]			
Reset	0x0				0x4			
Access Type					Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision	0xX: Device revision number (RevID)

PWR4 (0xC)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	DIS_LOCAL_WAKE	–	WAKE_EN_A	RSVD[3:0]			
Reset	0b0	0b0	–	0b1	0x5			
Access Type		Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOCAL_WAKE	6	Disable wake-up by local µC from SDA_RX pin	0b0: Local wake-up enabled 0b1: Local wake-up disabled
WAKE_EN_A	4	Enable wake-up by remote chip connected to GMSL Link	0b0: GMSL Link remote wake-up disabled 0b1: GMSL Link remote wake-up enabled

CTRL0 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	RESET_ALL	RESET_LINK	RESET_ONESHOT	RSVD	RSVD	–	RSVD[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	–	0b01	
Access Type	Write, Read	Write, Read	Write Clears All, Read			–		

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	7	Writing 1 to this bit resets the device, including all blocks. Registers are reset to defaults. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset
RESET_LINK	6	Reset data path (keep register settings). Write 1 to activate reset. Write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONESHOT	5	Reset data path (keep register settings). Write 1 to activate reset, bit self clears and automatically releases reset.	0b0: No action 0b1: Reset data path

CTRL2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	LDO_BYPASS	RSVD[1:0]		RSVD[1:0]	
Reset	0b0	0b0	–	0b0	0b01		0b00	
Access Type			–	Write, Read				

BITFIELD	BITS	DESCRIPTION
LDO_BYPASS	4	Enable LDO bypass

CTRL3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD[1:0]		LOCKED	ERROR	CMU_LOCKED	–
Reset	0b0	0b0	0b01		0b0	0b0	0b0	–
Access Type					Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED	3	GMSL Link Locked (bidirectional)	0b0: GMSL link not locked 0b1: GMSL link locked
ERROR	2	Reflects global error status	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock Multiplier Unit (CMU) Locked	0b0: CMU not locked 0b1: CMU locked

INTR0 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	–	AUTO_ERR_RST_EN	DEC_ERR_THR[2:0]		
Reset	0b1	0b0	0b1	–	0b0	0b000		
Access Type				–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_ERR_RST_EN	3	Automatically resets DEC_ERR_A (0x22) and IDLE_ERR (0x24) bitfields after ERRB pin is asserted for 1µs.	0b0: Auto reset disabled 0b1: Auto reset enabled
DEC_ERR_THR	2:0	Decoding and idle-error reporting threshold. Threshold controls the number of errors that can happen before the error flags assert. DEC_ERR_FLAG_A is asserted when DEC_ERR_A ≥ DEC_ERR_THR IDLE_ERR_FLAG is asserted when IDLE_ERR ≥ DEC_ERR_THR	0b000: 1 0b001: 2 0b010: 4 0b011: 8 0b100: 16 0b101: 32 0b110: 64 0b111: 128

INTR1 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_EXP[3:0]				AUTO_CNT_RST_EN	RSVD[2:0]		
Reset	0x0				0b0	0b000		
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_EXP	7:4	Packet Count Multiplier Exponent See the description of PKT_CNT (0x25) bitfield.	0bXXX: PKT_CNT exponent

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_CNT_RST_EN	3	Automatically reset PKT_CNT (0x25) bitfield after ERRB pin is asserted for 1µs.	0b0: Auto reset disabled 0b1: Auto reset enabled

INTR2 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_OEN	–	RSVD	IDLE_ERR_OEN	–	DEC_ERR_OEN_A
Reset	0b0	0b0	0b0	–	0b1	0b0	–	0b1
Access Type			Write, Read	–		Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_OEN	5	Enable reporting of remote error status (REM_ERR - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
IDLE_ERR_OEN	2	Enable reporting of idle-word errors (IDLE_ERR_FLAG - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
DEC_ERR_OEN_A	0	Enable reporting of decoding errors (DEC_ERR_FLAG_A - 0x1B) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR3 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	REM_ERR_FLAG	–	RSVD	IDLE_ERR_FLAG	–	DEC_ERR_FLAG_A
Reset	0b0	0b0	0b0	–	0b0	0b0	–	0b0
Access Type			Read Only	–		Read Only	–	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
REM_ERR_FLAG	5	Received remote side error status (inverse of remote side ERRB pin level)	0b0: No remote side error 0b1: Remote side error
IDLE_ERR_FLAG	2	Idle-Word Error Flag Asserted when IDLE_ERR (0x24) ≥ DEC_ERR_THR (0x18).	0b0: Flag not asserted 0b1: Flag asserted
DEC_ERR_FLAG_A	0	GMSL Packet Decoding Error Flag Asserted when DEC_ERR_A (at addr 0x22) ≥ DEC_ERR_THR (at addr 0x18).	0b0: Error flag not asserted 0b1: Error flag asserted

INTR4 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	EOM_ERR_OEN_A	RSVD	RSVD	MAX_RT_OEN	RT_CNT_OEN	PKT_CNT_OEN	–
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b0	–
Access Type		Write, Read			Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_A	6	Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_A - 0x1D) for GMSL Link at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
MAX_RT_OEN	3	Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG - 0x1D) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
RT_CNT_OEN	2	Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG _0x1C) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled
PKT_CNT_OEN	1	Enable reporting of packet count flag (PKT_CNT_FLAG - 0x1E) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR5 (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	EOM_ERR_FLAG_A	RSVD	RSVD	MAX_RT_FLAG	RT_CNT_FLAG	PKT_CNT_FLAG	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type		Read Only			Read Only	Read Only	Read Only	–

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_A	6	Eye-opening is below the configured threshold set by EOM_MIN_THR[6:0]. This bit is sticky. It is cleared when read.	0b0: Flag not asserted 0b1: Flag asserted
MAX_RT_FLAG	3	Combined ARQ maximum retransmission limit error flag Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN (0x1C) bitfield.	0b0: Flag not asserted 0b1: Flag asserted
RT_CNT_FLAG	2	Combined ARQ retransmission event flag Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN (0x1C) bitfield.	0b0: Flag not asserted 0b1: Flag asserted
PKT_CNT_FLAG	1	Packet Count Flag Asserted when PKT_CNT (0x25) ≥ PKT_CNT_THR (0x19)	0b0: Flag not asserted 0b1: Flag asserted

INTR6 (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	MIPI_ERR_OEN
Reset	0b1	0b1	0b1	0b1	0b1	0b0	0b1	0b1
Access Type								Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_ERR_OEN	0	Enable reporting of MIPI RX errors (MIPI_ERR_FLAG) at ERRB pin	0b0: Reporting disabled 0b1: Reporting enabled

INTR7 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	EFUSE_CRC_ERR	RSVD	RSVD	RSVD	MIPI_ERR_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type				Read Only				Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
EFUSE_CRC_ERR	4	efuse CRC error indicator	0b0: Flag not asserted 0b1: Flag asserted
MIPI_ERR_FLAG	0	MIPI RX error flag, asserted when any of these is asserted: phy1_hs_err [0],[1],[4],[5] phy2_hs_err [0],[1],[4],[5] ctrl1_csi_err_l [0],[1],[7] ctrl1_csi_err_h [0]	0b0: Flag not asserted 0b1: Flag asserted

INTR8 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
Reset	0b1	–	–	0b11111				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmit local error status (inverse of ERRB pin level) to remote side through GPIO channel	0b0: Transmit error status disabled 0b1: Transmit error status enabled
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX. Error status is transmitted to remote side using the GPIO interface, using this value as a special GPIO index. It is not recommended to change this value.	0bXXXXX: Value of GPIO ID for transmitting ERR_TX

INTR9 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN	RSVD	–	ERR_RX_ID[4:0]				
Reset	0b1	0b1	–	0b11111				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN	7	Enable reception of remote error status (inverse of ERRB pin level) through GPIO channel	0b0: Receive error status disabled 0b1: Receive error status enabled
ERR_RX_ID	4:0	GPIO ID used for receiving ERR_RX. Error status is received from remote side using the GPIO interface, using this value as a special GPIO index. It is not recommended to change this value.	0bXXXXX: Value of GPIO ID for receiving ERR_TX

CNT0 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	Number of decoding (disparity) errors detected in packets received over GMSL link. Cleared on read or upon link transitioning from unlock to lock state.	0xXX: Number of detected GMSL link disparity errors

CNT2 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR	7:0	Number of idle-word errors detected. Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle-word errors detected

CNT3 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT	7:0	Number of received packets of a selected type. Packet type is selected with PKT_CNT_SEL (0x2C register). Reported packet count is a scaled value, such that actual packet count is ≥ PKT_CNT x ($2^{PKT\_CNT\_EXP}$) and < (PKT_CNT + 1) x ($2^{PKT\_CNT\_EXP}$). When maximum value is reported, packet count is greater or equal to the reported value.	0xXX: Scaled number of received packets

TX1 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_GEN	RSVD	–	ERRG_EN_A	RSVD	–	DIS_SCR	DIS_ENC
Reset	0b0	0x0	–	0b0	0x1	–	0b0	0b0
Access Type	Write, Read		–	Write, Read		–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_GEN	7	Enable link PRBS-7 generator	0x0: Disabled 0x1: Enabled
ERRG_EN_A	4	Error Generator Enable for GMSL Link. Error injection applies to all data going across the link.	0b0: GMSL Link error generator disabled 0b1: GMSL Link error generator enabled
DIS_SCR	1	Disable scrambler	
DIS_ENC	0	Disable 9b10b encoding	

TX2 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0b00		0b10		0b000			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 0b10: 128 0b11: 1024
ERRG_RATE	5:4	Error generator average bit error rate	0b00: 1 in 5120 bits 0b01: 1 in 81920 bits 0b10: 1 in 1310720 bits 0b11: 1 in 20971520 bits

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_BURST	3:1	Error generator burst error length in bits	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error generator error distribution selection	0b0: Pseudorandom 0b1: Periodic

RX1 (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	LINK_PRBS_CHK	–	RSVD[1:0]		RSVD[1:0]		RSVD	RSVD
Reset	0b0	–	0b10		0b10		0b0	0b0
Access Type	Write, Read	–						

BITFIELD	BITS	DESCRIPTION	DECODE
LINK_PRBS_CHK	7	Enable link PRBS-7 checker	0x0: Disabled 0x1: Enabled

GPIOA (0x30)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0b1	0b000001					
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. This must be the same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs. See the GMSL user guide for further information.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x31)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0b10		0b001000					
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. This must be the same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs. See the GMSL user guide for further information.	0bXXXXXX: Reverse compensation delay multiplier value

I2C_0 (0x40)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH[1:0]		–	SLV_TO[2:0]		
Reset	–	–	0b10		–	0b110		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH	5:4	I^2C-to-I^2C slave-setup and hold-time setting. Configures the interval between SDA and SCL transitions when driven by the internal I^2C slave.	0b00: Set for I^2C Fast-mode Plus speed (1Mbps) 0b01: Set for I^2C Fast-mode speed (400Kbps) 0b10: Set for I^2C Standard-mode speed (100Kbps) 0b11: Reserved
SLV_TO	2:0	I^2C-to-I^2C slave timeout setting. Internal GMSL2 I^2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT[2:0]			–	MST_TO[2:0]		
Reset	0b0	0b101			–	0b110		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT	6:4	I²C-to-I²C master bit rate setting Configures the I²C bit rate used by the internal I²C master (in the device on the remote side from the external I²C master) Set this according to the I²C speed mode.	0b000: 9.92Kbps - Set for I²C Standard mode speed 0b001: 33.2Kbps - Set for I²C Standard mode speed 0b010: 99.2Kbps - Set for I²C Standard or Fast-mode speed 0b011: 123Kbps - Set for I²C Fast-mode speed 0b100: 203Kbps - Set for I²C Fast-mode speed 0b101: 397Kbps - Set for I²C Fast or Fast-mode Plus speed 0b110: 625Kbps - Set for I²C Fast-mode Plus speed 0b111: 980Kbps - Set for I²C Fast-mode Plus speed
MST_TO	2:0	I²C-to-I²C master timeout setting Internal GMSL2 I²C master times out after the configured duration if it does not receive any response while waiting for a packet from remote device.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A	7:1	I²C address translator source A for main control channel. When an I²C transaction across the GMSL link has a device address matching I²C SRC_A, the device address as seen on the remote side is replaced by the device address in I²C DST_A.	0bXXXXXXX: Value of I²C SRC_A

I2C_3 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	DST_A[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A	7:1	I²C address translator destination A for main control channel. See the description of I²C SRC_A.	0bXXXXXXX: Value of I²C DST_A

I2C_4 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B	7:1	I2C address translator source B for main control channel. When an I2C transaction across the GMSL link has a device address matching I2C SRC_B, the device address as seen on the remote side is replaced by the device address in I2C DST_B.	0bXXXXXXX: Value of I2C SRC_B

I2C_5 (0x45)

BIT	7	6	5	4	3	2	1	0
Field	DST_B[6:0]							–
Reset	0b0000000							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B	7:1	I2C address translator destination B for main control channel. See the description of I2C SRC_B.	0bXXXXXXX: Value of I2C DST_B

TX0 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	–	RSVD[1:0]		RSVD[1:0]		RSVD[1:0]	
Reset	0b0	–	0b11		0b00		0b00	
Access Type	Write, Read	–						

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	Transmit CRC Enable	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled

TX3 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TX_STR_SEL[1:0]	
Reset	–	–	–	–	–	–	0b10	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_STR_SEL	1:0	Stream ID used in packets transmitted from this channel	0bXX: Stream ID for packets from this channel

TR0 (0x78)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		RSVD[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled

TR3 (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value is based on the device address set by the CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. This is a one-hot encoding. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received … … 0xFF: Packets from all source IDs received

TR0 (0x90)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		RSVD[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0b11		0b00		0b00	
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculate and append CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC and CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled

TR3 (0x93)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this channel. Default value is based on the device address set by the CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x94)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receive packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. This is a one-hot encoding. For example, when SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 are received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received … … 0xFF: Packets from all source IDs received

ARQ0 (0x95)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	ARQ0_EN	DIS_DBL_ACK_RETX	–	–
Reset	0b1	0b0	0b0	0b1	0b1	0b0	–	–
Access Type					Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ARQ0_EN	3	Enable ARQ. It is not recommended to change this value.	0b0: ARQ disabled 0b1: ARQ enabled
DIS_DBL_ACK_RETX	2	Disable retransmission due to receiving same acknowledge twice	0b0: Enabled 0b1: Disabled

ARQ1 (0x96)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD[2:0]			–	–	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0b111			–	–	0b1	0b0
Access Type	–				–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR) for this channel at ERRB pin.	0b0: ARQ maximum retransmission limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmission limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0x97)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmission limit (MAX_RT) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0xXX: Count of retransmissions for this channel

VIDEO_TX0 (0x110)

BIT	7	6	5	4	3	2	1	0
Field	LINE_CRC_SEL	LINE_CRC_EN	ENC_MODE[1:0]		AUTO_BPP	CLKDET_BYP	RSVD[1:0]	
Reset	0b0	0b1	0b10		0b1	0b0	0b00	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_SEL	7	Line CRC checksum generation with DE or HS	0b0: Use DE for Line CRC 0b1: Use HS for Line CRC
LINE_CRC_EN	6	Line CRC Enable Generates a CRC code for the video line and sends it to the receiver side for comparison.	0b0: Line CRC disabled 0b1: Line CRC enabled
ENC_MODE	5:4	HS, VS, and DE Encoding mode. This Encoding mode is intended to minimize video bandwidth usage on the GMSL link. When the encoding is on, the HS, VS, DE signals are included in video packets across the GMSL link only when they toggle. Additionally, color pixel data may not be transmitted during horizontal or vertical blanking periods. When the encoding is off, the HS, VS, DE signals are included in all video packets, along with the color pixel data, and are sent every 36 pixels.	0b00: HS, VS, DE encoding off 0b01: HS, VS, DE encoding on, color bits always sent 0b10: HS, VS, DE encoding on, color bits sent only when DE is high 0b11: HS, VS, DE encoding on, color bits sent only when HS is high
AUTO_BPP	3	Select bits per pixel (BPP) source. Set to 0 if override of BPP is required.	0b0: Use BPP from BPP register 0b1: Use BPP from MIPI receiver
CLKDET_BYP	2	Bypass PCLK detector	

VIDEO_TX1 (0x111)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		BPP[5:0]					
Reset	0b01		0b011000					
Access Type			Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BPP	5:0	Color bits per pixel (RGB888 = 24)	0bXXXXXX: Number of bits per pixel

VIDEO_TX2 (0x112)

BIT	7	6	5	4	3	2	1	0
Field	PCLKDET	DRIFT_ERR	OVERFLOW	FIFO_WARN	RSVD	LIM_HEART	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b1	0b0
Access Type	Read Only	Read Clears All	Read Clears All	Read Clears All		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PCLKDET	7	PCLK detected. This bit is asserted when a pixel clock can be extracted from the video interface receiver and the extracted frequency is measured to be greater than 4MHz. Valid in all video modes. Can also read the following registers to determine if MIPI data is received: phy1_pkt_cnt, csi1_pkt_cnt. In tunneling mode, can also read tun_pkt_cnt.	0b0: Video received PCLK not detected 0b1: Video received PCLK detected
DRIFT_ERR	6	VID_TX PCLK drift error detected. After the video pipeline starts, PCLK cannot drift more than a certain amount (+/-1.25%) without restarting the subsystem.	0b0: Video transmit PCLK drift error not detected 0b1: Video transmit PCLK drift error detected
OVERFLOW	5	VID_TX FIFO has overflowed, video input throughput may be too high, bandwidth allocation on GMSL link for video may not be enough.	0b0: Video transmit FIFO has not overflowed 0b1: Video transmit FIFO has overflowed
FIFO_WARN	4	VID_TX FIFO is more than half full, video data coming from the video interface receiver is read by the scheduler	0b0: Video transmit FIFO is less than or equal to half full 0b1: Video transmit FIFO is more than half full
LIM_HEART	2	Disable heartbeat during blanking Use together with SEQ_MISS_EN and DIS_PKT_DET bitfields in deserializer.	0b0: Heartbeat enabled during blanking 0b1: Heartbeat disabled during blanking

CROSS_0 (0x236)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS0_I	CROSS0_F	CROSS0[4:0]				
Reset	–	0b0	0b0	0b00000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS0_I	6	Invert outgoing bit 0	0b0: Do not invert bit 0b1: Invert bit
CROSS0_F	5	Force outgoing bit 0 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS0	4:0	Maps incoming bit position set by this field to the outgoing bit position 0	0bXXXXX: Incoming bit position

CROSS_1 (0x237)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS1_I	CROSS1_F	CROSS1[4:0]				
Reset	–	0b0	0b0	0b00001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS1_I	6	Invert outgoing bit 1	0b0: Do not invert bit 0b1: Invert bit
CROSS1_F	5	Force outgoing bit 1 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS1	4:0	Maps incoming bit position set by this field to the outgoing bit position 1	0bXXXXX: Incoming bit position

CROSS_2 (0x238)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS2_I	CROSS2_F	CROSS2[4:0]				
Reset	–	0b0	0b0	0b00010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS2_I	6	Invert outgoing bit 2	0b0: Do not invert bit 0b1: Invert bit
CROSS2_F	5	Force outgoing bit 2 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS2	4:0	Maps incoming bit position set by this field to the outgoing bit position 2	0bXXXXX: Incoming bit position

CROSS_3 (0x239)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS3_I	CROSS3_F	CROSS3[4:0]				
Reset	–	0b0	0b0	0b00011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS3_I	6	Invert outgoing bit 3	0b0: Do not invert bit 0b1: Invert bit
CROSS3_F	5	Force outgoing bit 3 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS3	4:0	Maps incoming bit position set by this field to the outgoing bit position 3	0bXXXXX: Incoming bit position

CROSS_4 (0x23A)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS4_I	CROSS4_F	CROSS4[4:0]				
Reset	–	0b0	0b0	0b00100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS4_I	6	Invert outgoing bit 4	0b0: Do not invert bit 0b1: Invert bit
CROSS4_F	5	Force outgoing bit 4 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS4	4:0	Maps incoming bit position set by this field to the outgoing bit position 4	0bXXXXX: Incoming bit position

CROSS_5 (0x23B)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS5_I	CROSS5_F	CROSS5[4:0]				
Reset	–	0b0	0b0	0b00101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS5_I	6	Invert outgoing bit 5	0b0: Do not invert bit 0b1: Invert bit
CROSS5_F	5	Force outgoing bit 5 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS5	4:0	Maps incoming bit position set by this field to the outgoing bit position 5	0bXXXXX: Incoming bit position

CROSS_6 (0x23C)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS6_I	CROSS6_F	CROSS6[4:0]				
Reset	–	0b0	0b0	0b00110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS6_I	6	Invert outgoing bit 6	0b0: Do not invert bit 0b1: Invert bit
CROSS6_F	5	Force outgoing bit 6 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS6	4:0	Maps incoming bit position set by this field to the outgoing bit position 6	0bXXXXX: Incoming bit position

CROSS_7 (0x23D)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS7_I	CROSS7_F	CROSS7[4:0]				
Reset	–	0b0	0b0	0b00111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS7_I	6	Invert outgoing bit 7	0b0: Do not invert bit 0b1: Invert bit
CROSS7_F	5	Force outgoing bit 7 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS7	4:0	Maps incoming bit position set by this field to the outgoing bit position 7	0bXXXXX: Incoming bit position

CROSS_8 (0x23E)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS8_I	CROSS8_F	CROSS8[4:0]				
Reset	–	0b0	0b0	0b01000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS8_I	6	Invert outgoing bit 8	0b0: Do not invert bit 0b1: Invert bit
CROSS8_F	5	Force outgoing bit 8 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS8	4:0	Maps incoming bit position set by this field to the outgoing bit position 8	0bXXXXX: Incoming bit position

CROSS_9 (0x23F)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS9_I	CROSS9_F	CROSS9[4:0]				
Reset	–	0b0	0b0	0b01001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS9_I	6	Invert outgoing bit 9	0b0: Do not invert bit 0b1: Invert bit
CROSS9_F	5	Force outgoing bit 9 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS9	4:0	Maps incoming bit position set by this field to the outgoing bit position 9	0bXXXXX: Incoming bit position

CROSS_10 (0x240)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS10_I	CROSS10_F	CROSS10[4:0]				
Reset	–	0b0	0b0	0b01010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS10_I	6	Invert outgoing bit 10	0b0: Do not invert bit 0b1: Invert bit
CROSS10_F	5	Force outgoing bit 10 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS10	4:0	Maps incoming bit position set by this field to the outgoing bit position 10	0bXXXXX: Incoming bit position

CROSS_11 (0x241)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS11_I	CROSS11_F	CROSS11[4:0]				
Reset	–	0b0	0b0	0b01011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS11_I	6	Invert outgoing bit 11	0b0: Do not invert bit 0b1: Invert bit
CROSS11_F	5	Force outgoing bit 11 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS11	4:0	Maps incoming bit position set by this field to the outgoing bit position 11	0bXXXXX: Incoming bit position

CROSS_12 (0x242)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS12_I	CROSS12_F	CROSS12[4:0]				
Reset	–	0b0	0b0	0b01100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS12_I	6	Invert outgoing bit 12	0b0: Do not invert bit 0b1: Invert bit
CROSS12_F	5	Force outgoing bit 12 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS12	4:0	Maps incoming bit position set by this field to the outgoing bit position 12	0bXXXXX: Incoming bit position

CROSS_13 (0x243)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS13_I	CROSS13_F	CROSS13[4:0]				
Reset	–	0b0	0b0	0b01101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS13_I	6	Invert outgoing bit 13	0b0: Do not invert bit 0b1: Invert bit
CROSS13_F	5	Force outgoing bit 13 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS13	4:0	Maps incoming bit position set by this field to the outgoing bit position 13	0bXXXXX: Incoming bit position

CROSS_14 (0x244)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS14_I	CROSS14_F	CROSS14[4:0]				
Reset	–	0b0	0b0	0b01110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS14_I	6	Invert outgoing bit 14	0b0: Do not invert bit 0b1: Invert bit
CROSS14_F	5	Force outgoing bit 14 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS14	4:0	Maps incoming bit position set by this field to the outgoing bit position 14	0bXXXXX: Incoming bit position

CROSS_15 (0x245)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS15_I	CROSS15_F	CROSS15[4:0]				
Reset	–	0b0	0b0	0b01111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15_I	6	Invert outgoing bit 15	0b0: Do not invert bit 0b1: Invert bit
CROSS15_F	5	Force outgoing bit 15 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS15	4:0	Maps incoming bit position set by this field to the outgoing bit position 15	0bXXXXX: Incoming bit position

CROSS_16 (0x246)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS16_I	CROSS16_F	CROSS16[4:0]				
Reset	–	0b0	0b0	0b10000				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS16_I	6	Invert outgoing bit 16	0b0: Do not invert bit 0b1: Invert bit
CROSS16_F	5	Force outgoing bit 16 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS16	4:0	Maps incoming bit position set by this field to the outgoing bit position 16	0bXXXXX: Incoming bit position

CROSS_17 (0x247)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS17_I	CROSS17_F	CROSS17[4:0]				
Reset	–	0b0	0b0	0b10001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS17_I	6	Invert outgoing bit 17	0b0: Do not invert bit 0b1: Invert bit
CROSS17_F	5	Force outgoing bit 17 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS17	4:0	Maps incoming bit position set by this field to the outgoing bit position 17	0bXXXXX: Incoming bit position

CROSS_18 (0x248)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS18_I	CROSS18_F	CROSS18[4:0]				
Reset	–	0b0	0b0	0b10010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_I	6	Invert outgoing bit 18	0b0: Do not invert bit 0b1: Invert bit

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS18_F	5	Force outgoing bit 18 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS18	4:0	Maps incoming bit position set by this field to the outgoing bit position 18	0bXXXXX: Incoming bit position

CROSS_19 (0x249)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS19_I	CROSS19_F	CROSS19[4:0]				
Reset	–	0b0	0b0	0b10011				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS19_I	6	Invert outgoing bit 19	0b0: Do not invert bit 0b1: Invert bit
CROSS19_F	5	Force outgoing bit 19 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS19	4:0	Maps incoming bit position set by this field to the outgoing bit position 19	0bXXXXX: Incoming bit position

CROSS_20 (0x24A)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS20_I	CROSS20_F	CROSS20[4:0]				
Reset	–	0b0	0b0	0b10100				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS20_I	6	Invert outgoing bit 20	0b0: Do not invert bit 0b1: Invert bit
CROSS20_F	5	Force outgoing bit 20 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS20	4:0	Maps incoming bit position set by this field to the outgoing bit position 20	0bXXXXX: Incoming bit position

CROSS_21 (0x24B)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS21_I	CROSS21_F	CROSS21[4:0]				
Reset	–	0b0	0b0	0b10101				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS21_I	6	Invert outgoing bit 21	0b0: Do not invert bit 0b1: Invert bit
CROSS21_F	5	Force outgoing bit 21 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS21	4:0	Maps incoming bit position set by this field to the outgoing bit position 21	0bXXXXX: Incoming bit position

CROSS_22 (0x24C)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS22_I	CROSS22_F	CROSS22[4:0]				
Reset	–	0b0	0b0	0b10110				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS22_I	6	Invert outgoing bit 22	0b0: Do not invert bit 0b1: Invert bit
CROSS22_F	5	Force outgoing bit 22 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS22	4:0	Maps incoming bit position set by this field to the outgoing bit position 22	0bXXXXX: Incoming bit position

CROSS_23 (0x24D)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS23_I	CROSS23_F	CROSS23[4:0]				
Reset	–	0b0	0b0	0b10111				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS23_I	6	Invert outgoing bit 23	0b0: Do not invert bit 0b1: Invert bit
CROSS23_F	5	Force outgoing bit 23 to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS23	4:0	Maps incoming bit position set by this field to the outgoing bit position 23	0bXXXXX: Incoming bit position

VTX0 (0x24E)

Used to generate sync signals for the image sensor. Uses reference clock output (derived from XTAL clock) as reference to generate sync signals for the image sensor.

REF_VTG works the same as regular VTG, with the exception of how they are connected internally. VTG uses the input pixel clock as the clock source, and HS, VS, DE signals generated can replace the HS, VS, DE signals received in the input video.

REF_VTG uses the REFGEN_PLL output as the clock source. REFGEN_PLL is a DPLL that uses XTAL clock as the clock source. It can be programmed to generate any PCLK frequency. PCLK generated by REFGEN_PLL (RCLK in pin description) and HS, VS, DE generated by REF_VTG are synchronous to RCLK and output from MFP pins, when enabled. These are then used by the image sensor, which drives the CSI-2 input of the serializer.

BIT	7	6	5	4	3	2	1	0
Field	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b11	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_VS	7	Enable to generate VS output according to the timing definition	0b0: Do not generate VS 0b1: Generate VS
GEN_HS	6	Enable to generate HS output according to the timing definition	0b0: Do not generate HS 0b1: Generate HS
GEN_DE	5	Enable to generate DE output according to the timing definition	0b0: Do not generate DE 0b1: Generate DE
VS_INV	4	Invert V_{SYNC} output of video-timing generator	0b0: Do not invert VS 0b1: Invert VS
HS_INV	3	Invert HSYNC output of video-timing generator	0b0: Do not invert HS 0b1: Invert HS
DE_INV	2	Invert DE output of video-timing generator	0b0: Do not invert DE 0b1: Invert DE

BITFIELD	BITS	DESCRIPTION	DECODE
VTG_MODE	1:0	Video interface timing-generation mode. Used when VTG GEN_VS, GEN_HS, or GEN_DE are enabled. 00 = VS tracking mode. VS input's period (VS_HIGH + VS_LOW) is tracked. After VS tracking is locked, any VS input edge (glitches) not in the expected PCLK cycle is ignored. VS tracking is locked with three consecutive matches and unlocked by three consecutive mismatches. When unlocked or powered up, the next VS input edge is assumed to be the right VS edge. 01 = VS one-trigger mode (default) One VS input edge triggers the generation of one frame of VS/HS/DE output. If the next VS input edge comes earlier or later than expected by VS period, the newly generated frame is correct. The current VS/HS/DE output is cut or extended at the time point of the rising edge of the newly generated VS/HS/DE output. 10 = Auto-repeat mode VS input edge triggers the generation of continuous frames of VS/HS/DE output even if no more VS input edges are seen. If the next VS input edge comes earlier or later than expected by VS period, the newly generated frame is correct. The current VS/HS/DE output is cut or extended at the time point of the rising edge of the newly generated VS/HS/DE output.	0b00: VS tracking mode 0b01: VS one trigger mode 0b10: Auto-repeat mode 0b11: Free running mode

VTX1 (0x24F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCLKDET_VTX	–	PATGEN_CLK_SRC[2:0]			VS_TRIG
Reset	–	–	0b0	–	0b000			0b1
Access Type	–	–	Read Only	–	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PCLKDET_VTX	5	PCLK detected. This bit is asserted when a pixel clock can be extracted from the video interface receiver, and the extracted frequency is measured to be greater than 4MHz. Valid in all video modes. Also read the following registers to determine if MIPI data is received: phy1_pkt_cnt, csi1_pkt_cnt. In tunneling mode, tun_pkt_cnt can be read.	0b0: PCLK not detected 0b1: PCLK detected

BITFIELD	BITS	DESCRIPTION	DECODE
PATGEN_CLK_SRC	3:1	Pattern generator clock source for video PRBS, checkerboard, and gradient patterns.	3'b0XX: Use external clock 3'b100: Use 25MHz internal clock 3'b101: Use 75MHz internal clock 3'b110: Use 150MHz internal clock 3'b111: Use 375MHz internal clock
VS_TRIG	0	Select VS trigger edge (positive vs. negative polarity of VS)	0b0: Falling edge 0b1: Rising edge

VTX2 (0x250)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_2	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DLY cycles from the input VS. (bits [23:16])	0xXX: Most significant byte of VS_DLY

VTX3 (0x251)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_1	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DLY cycles from the input VS. (bits [15:8])	0xXX: Middle significant byte of VS_DLY

VTX4 (0x252)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_0	7:0	VS delay in terms of PCLK cycles The output VS is delayed by VS_DLY cycles from the input VS. (bits [7:0])	0xXX: Least significant byte of VS_DLY

VTX5 (0x253)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_2	7:0	VS high period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS high period

VTX6 (0x254)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_1	7:0	VS high period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS high period

VTX7 (0x255)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_0	7:0	VS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS high period

VTX8 (0x256)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_2	7:0	VS low period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS low period

VTX9 (0x257)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_1	7:0	VS low period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS low period

VTX10 (0x258)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_0	7:0	VS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS low period

VTX11 (0x259)

BIT	7	6	5	4	3	2	1	0
Field	V2H_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_2	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first HS rising edge

VTX12 (0x25A)

BIT	7	6	5	4	3	2	1	0
Field	V2H_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_1	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first HS rising edge

VTX13 (0x25B)

BIT	7	6	5	4	3	2	1	0
Field	V2H_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_0	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS edge to first HS rising edge

VTX14 (0x25C)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_1	7:0	HS high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS high period

VTX15 (0x25D)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_0	7:0	HS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS high period

VTX16 (0x25E)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_1	7:0	HS low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS low period

VTX17 (0x25F)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_0	7:0	HS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS low period

VTX18 (0x260)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_1	7:0	HS pulses per frame (bits [15:8])	0xXX: Most significant byte of HS pulses per frame

VTX19 (0x261)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_0	7:0	HS pulses per frame (bits [7:0])	0xXX: Least significant byte of HS pulses per frame

VTX20 (0x262)

BIT	7	6	5	4	3	2	1	0
Field	V2D_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_2	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first DE

VTX21 (0x263)

BIT	7	6	5	4	3	2	1	0
Field	V2D_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_1	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first DE

VTX22 (0x264)

BIT	7	6	5	4	3	2	1	0
Field	V2D_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_0	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS edge to first DE

VTX23 (0x265)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_1	7:0	DE high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE high period

VTX24 (0x266)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_0	7:0	DE high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE high period

VTX25 (0x267)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_1	7:0	DE low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE low period

VTX26 (0x268)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_0	7:0	DE low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE low period

VTX27 (0x269)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_1	7:0	Active lines per frame (DE pulses) (bits [15:8])	0xXX: Most significant byte of DE pulses per frame

VTX28 (0x26A)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_0	7:0	Active lines per frame (DE pulses) (bits [7:0])	0xXX: Least significant byte of DE pulses per frame

VTX29 (0x26B)

BIT	7	6	5	4	3	2	1	0
Field	VID_PRBS_EN	RSVD	VPRBS_FAIL	–	–	GRAD_MODE	PATGEN_MODE[1:0]	
Reset	0b0	0b0	0b0	–	–	0b0	0b00	
Access Type	Write, Read		Read Only	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PRBS_EN	7	Enable video PRBS generator	0b0: Video PRBS generator disabled 0b1: Video PRBS generator enabled
VPRBS_FAIL	5	Video PRBS check pass/fail	0b0: Video PRBS check passed 0b1: Video PRBS check failed
GRAD_MODE	2	Gradient pattern-generator mode	0b0: Gradient mode increasing. Each gradient color starts from a value of 0x00 and increases to 0xFF 0b1: Gradient mode decreasing. Each gradient color starts from a value of 0xFF and decreases to 0x00
PATGEN_MODE	1:0	Pattern-generator mode	0b00: Pattern generator disabled - use video from the serializer input 0b01: Generate checkerboard pattern 0b10: Generate gradient pattern 0b11: Reserved

VTX30 (0x26C)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_INC[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_INC	7:0	Gradient mode increment amount (increment amount is the register value divided by 4)	0xXX: Gradient increment base

VTX31 (0x26D)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_L	7:0	Checkerboard Mode Color A Low Byte	0xXX: Least significant byte of checkerboard mode color A

VTX32 (0x26E)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_M	7:0	Checkerboard Mode Color A Middle Byte	0xXX: Middle significant byte of checkerboard mode color A

VTX33 (0x26F)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_A_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_A_H	7:0	Checkerboard Mode Color A High Byte	0xXX: Most significant byte of checkerboard mode color A

VTX34 (0x270)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_L	7:0	Checkerboard Mode Color B Low Byte	0xXX: Least significant byte of checkerboard mode color B

VTX35 (0x271)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_M	7:0	Checkerboard Mode Color B Middle Byte	0xXX: Middle significant byte of checkerboard mode color B

VTX36 (0x272)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_B_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_B_H	7:0	Checkerboard Mode Color B High Byte	0xXX: Most significant byte of checkerboard mode color B

VTX37 (0x273)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_A[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_A	7:0	Checkerboard Mode Color A: Dimension of each square in number of pixels	0xXX: Repeat count of checkerboard mode color A

VTX38 (0x274)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_B[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_B	7:0	Checkerboard Mode Color B: Dimension of each square in number of pixels Set equal to CHKR_RPT_A for square checkerboard pattern	0xXX: Repeat count of checkerboard mode color B

VTX39 (0x275)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_ALT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_ALT	7:0	Checkerboard Mode Alternate Line Count: Dimension of each square in number of video lines Set equal to CHKR_RPT_A for square checkerboard pattern	0xXX: Checkerboard mode alternate line count

VTX40 (0x276)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	CROSSHS_I	CROSSHS_F	CROSSHS[4:0]				
Reset	0b0	0b0	0b0	0b11000				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSSHS_I	6	Invert outgoing HS	0b0: Do not invert bit 0b1: Invert bit
CROSSHS_F	5	Force HS to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	
CROSSHS	4:0	Map selected internal signal to HS	0bXXXXX: Incoming bit position

VTX41 (0x277)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSSVS_I	CROSSVS_F	CROSSVS[4:0]				
Reset	–	0b0	0b0	0b11001				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSSVS_I	6	Invert outgoing VS	0b0: Do not invert bit 0b1: Invert bit
CROSSVS_F	5	Force VS to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSSVS	4:0	Map selected internal signal to VS	0bXXXXX: Incoming bit position

VTX42 (0x278)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSSDE_I	CROSSDE_F	CROSSDE[4:0]				
Reset	–	0b0	0b0	0b11010				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSSDE_I	6	Invert outgoing DE	0b0: Do not invert bit 0b1: Invert bit
CROSSDE_F	5	Force DE to 0. Applied before inversion so that if inversion is also set, the outgoing bit is forced to 1.	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSSDE	4:0	Map selected internal signal to DE	0bXXXXX: Incoming bit position

GPIO_A (0x2BE)

GPIO 0

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b1	0b1	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL reception 0b1: This GPIO source enabled for GMSL reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2BF)

GPIO 0

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00000				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C0)

GPIO 0

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00000				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2C7)

GPIO 3

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL reception 0b1: This GPIO source enabled for GMSL reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2C8)

GPIO 3

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00011				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2C9)

GPIO 3

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00011				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2CA)

GPIO 4

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b1	0b1	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL reception 0b1: This GPIO source enabled for GMSL reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2CB)

GPIO 4

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00100				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull up/down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2CC)

GPIO 4

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00100				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	

GPIO_A (0x2CD)

GPIO 5

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pull-up/pull-down strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL reception 0b1: This GPIO source enabled for GMSL reception
GPIO_TX_EN	1	GPIO TX source control	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2CE)

GPIO 5

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00101				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull up/down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2CF)

GPIO 5

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00101				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2D0)

GPIO 6

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b1	0b1	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pull-up/pull-down strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL reception 0b1: This GPIO source enabled for GMSL reception
GPIO_TX_EN	1	GPIO TX source control	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2D1)

GPIO 6

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		RSVD	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00110				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull up/down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D2)

GPIO 6

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00110				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2D3)

GPIO 7

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pull-up/pull-down strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL reception 0b1: This GPIO source enabled for GMSL reception
GPIO_TX_EN	1	GPIO TX source control	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2D4)

GPIO 7

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b10		0b1	0b00111				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull up/down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D5)

GPIO 7

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b00111				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x2D6)

GPIO 8

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0b0	0b0	0b1	0b1	0b1	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pull-up/pull-down strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0. This can be used to drive a value out on an MFP.	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin local MFP input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control. Set to 1 to receive GPIO value from GMSL link. Set GPIO_OUT_DIS to 0 to output the received value on the local MFP.	0b0: This GPIO source disabled for GMSL reception 0b1: This GPIO source enabled for GMSL reception
GPIO_TX_EN	1	GPIO TX source control	0b0: This GPIO source disabled for GMSL transmission 0b1: This GPIO source enabled for GMSL transmission
GPIO_OUT_DIS	0	Disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x2D7)

GPIO 8

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0b00		0b1	0b01000				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pull up/down configuration	0b00: None 0b01: Pull-up 0b10: Pull-down 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x2D8)

GPIO 8

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	RSVD	–	GPIO_RX_ID[4:0]				
Reset	0b0	0b1	–	0b01000				
Access Type	Write, Read		–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG, PULL_UPDN_SEL, OUT_TYPE, and GPIO_OUT_DIS determine IO type for non-GPIO configuration
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

FRONTTOP_0 (0x308)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	enable_line_info	START_PORTB	–	–	RSVD	–	–
Reset	0b0	0b1	0b1	–	–	0b1	–	–
Access Type		Write, Read	Write, Read	–	–		–	–

BITFIELD	BITS	DESCRIPTION	DECODE
enable_line_info	6	Enable sending line start info-frames	0b0: Line start info frames disabled 0x1: Line start info frames enabled
START_PORTB	5	Enable CSI Port	0b0: CSI disabled 0x1: CSI enabled

FRONTTOP_5 (0x30D)

BIT	7	6	5	4	3	2	1	0
Field	VC_SELZ_L[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VC_SELZ_L	7:0	Virtual channel filter bits [7:0]. Each bit represents whether a virtual channel's packets are processed or discarded (bit 0 is virtual channel 0, bit 1 is virtual channel 1, etc.). If the bit is set to 1, the virtual channel packets are processed. If the bit is set to 0, the virtual channel packets are discarded.

FRONTTOP_6 (0x30E)

BIT	7	6	5	4	3	2	1	0
Field	VC_SELZ_H[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VC_SELZ_H	7:0	Virtual channel filter bits [15:8]. Each bit represents whether a virtual channel's packets are processed or discarded (bit 0 is virtual channel 0, bit 1 is virtual channel 1 etc.). If the bit is set to 1, the virtual channel packets are processed. If the bit is set to 0, the virtual channel packets are discarded

FRONTTOP_9 (0x311)

BIT	7	6	5	4	3	2	1	0
Field	–	START_PORTBZ	–	–	–	–	–	–
Reset	–	0b1	–	–	–	–	–	–
Access Type	–	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
START_PORTBZ	6	Start video pipe Z from CSI port	0b0: Video not started 0b1: Start video

FRONTTOP_10 (0x312)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	–	–	–	bpp8dblz	–	–
Reset	–	0b0	–	–	–	0b0	–	–
Access Type	–		–	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dblz	2	Send 8-bit pixels as 16-bit on video pipe Z (double pixel mode). Maximizes GMSL link bandwidth capacity for 8-bit pixels.	0b0: Send as 8-bit pixels 0b1: Send 8-bit pixels as 16-bit

FRONTTOP_11 (0x313)

BIT	7	6	5	4	3	2	1	0
Field	–	bpp12dblz	–	–	–	bpp10dblz	–	–
Reset	–	0b0	–	–	–	0b0	–	–
Access Type	–	Write, Read	–	–	–	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
bpp12dblz	6	Send 12-bit pixels as 24-bit on video pipe Z (double pixel mode). Maximizes GMSL link bandwidth capacity for 12-bit pixels.	0b0: Send as 12-bit pixels 0b1: Send 12-bit pixels as 24-bit

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dblz	2	Send 10-bit pixels as 20-bit on video pipe Z (double pixel mode). Maximizes GMSL link bandwidth capacity for 10-bit pixels.	0b0: Send as 10-bit pixels 0b1: Send 10-bit pixels as 20-bit

FRONTTOP_16 (0x318)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt1_selz[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt1_selz	6:0	Select designated datatype to route to video pipeline Z. Bit 6 is the enable. Bits 5:0 are for the datatype. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt1_selz[6], mem_dt2_selz[6], mem_dt7_selz[6], and mem_dt8_selz[6] are all 0.	0b0XXXXXX: Datatype selection disabled 0b1XXXXXX: Datatype enabled for datatype selected to route to video pipeline

FRONTTOP_17 (0x319)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt2_selz[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt2_selz	6:0	Select designated datatype to route to video pipeline Z. Bit 6 is the enable. Bits 5:0 are for the datatype. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt1_selz[6], mem_dt2_selz[6], mem_dt7_selz[6], and mem_dt8_selz[6] are all 0.	0b0XXXXXX: Datatype selection disabled 0b1XXXXXX: Datatype enabled for datatype selected to route to video pipeline

FRONTTOP_22 (0x31E)

BIT	7	6	5	4	3	2	1	0
Field	soft_dtz_en	soft_vcz_en	soft_bppz_en	soft_bppz[4:0]				
Reset	0b0	0b0	0b0	0b11000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dtz_en	7	Datatype software override enable for video pipeline Z	0b0: Software override disabled 0b1: Software override enabled
soft_vcz_en	6	Virtual channel software override enable for video pipeline Z	0b0: Software override disabled 0b1: Software override enabled
soft_bppz_en	5	BPP software override enable for video pipeline Z	0b0: Software override disabled 0b1: Software override enabled
soft_bppz	4:0	Software override of BPP on video pipeline Z	0bXXXXX: Software override value

FRONTTOP_24 (0x320)

BIT	7	6	5	4	3	2	1	0
Field	–	–	soft_vcz[1:0]		–	–	–	–
Reset	–	–	0b00		–	–	–	–
Access Type	–	–	Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vcz	5:4	Virtual channel software override for video pipeline Z	0bXX: Software override value

FRONTTOP_27 (0x323)

BIT	7	6	5	4	3	2	1	0
Field	–	–	soft_dtz[5:0]					
Reset	–	–	0b110000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dtz	5:0	Datatype software override for video channel Z	0bXXXXXX: Software override value

FRONTTOP_29 (0x325)

BIT	7	6	5	4	3	2	1	0
Field	FORCE_START_MIPI_FRONTTOP	–	–	–	–	–	–	–
Reset	0b0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
FORCE_START_MIPI_FRONTTOP	7	Force the MIPI receiver start without waiting for the GMSL link lock.	0b0: Do not force MIPI receiver to start without waiting for GMSL link lock 0b1: Force MIPI receiver to start without waiting for GMSL link lock

MIPI_RX0 (0x330)

BIT	7	6	5	4	3	2	1	0
Field	–	mipi_noncontclk_en	ctrl1_vc_map_en	–	mipi_rx_reset	RSVD[2:0]		
Reset	–	0b0	0b0	–	0b0	0b000		
Access Type	–	Write, Read	Write, Read	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
mipi_noncontclk_en	6	MIPI non-continuous clock enable	0x0: enable MIPI continuous clock 0x1: enable MIPI non-continuous clock
ctrl1_vc_map_en	5	Virtual channel mapping enable. When enabled, the incoming virtual channel numbers are remapped according to the values in the ctrl1_vc_map0 through ctrl1_vc_map15 register bits.	0x0: Disable virtual channel mapping 0x1: Enable virtual channel mapping
mipi_rx_reset	3	Reset MIPI RX receiver (MIPI PHY). This bit is not self-clearing.	0b0: Do not reset MIPI RX 0b1: Reset MIPI RX

MIPI_RX1 (0x331)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	ctrl1_num_lanes[1:0]		–	–	–	–
Reset	0b0	0b0	0b11		–	–	–	–
Access Type			Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_num_lanes	5:4	Select number of data lanes	0b00: Reserved 0b01: Reserved 0b10: Reserved 0b11: Four data lanes

MIPI_RX2 (0x332)

BIT	7	6	5	4	3	2	1	0
Field	phy1_lane_map[3:0]				–	–	–	–
Reset	0xE				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_lane_map	7:4	Serializer lane mapping for MIPI data lane 2 and 3. Bit[5:4] controls data lane 2. Bit[7:6] controls data lane 3. Works with phy2_lane_map register. Lane maps must be exclusive.	0bXX00: Map Sensor Lane 0 to Serializer Lane 2 0bXX01: Map Sensor Lane 1 to Serializer Lane 2 0bXX10: Map Sensor Lane 2 to Serializer Lane 2 0bXX11: Map Sensor Lane 3 to Serializer Lane 2 0b00XX: Map Sensor Lane 0 to Serializer Lane 3 0b01XX: Map Sensor Lane 1 to Serializer Lane 3 0b10XX: Map Sensor Lane 2 to Serializer Lane 3 0b11XX: Map Sensor Lane 3 to Serializer Lane 3

MIPI_RX3 (0x333)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	phy2_lane_map[3:0]			
Reset	–	–	–	–	0x4			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_lane_map	3:0	Serializer lane mapping for MIPI data lane 0 and 1. Bit[1:0] controls data lane 0, Bit[3:2] controls data lane 1. Works with phy1_lane_map register. Lane maps must be exclusive.	0bXX00: Map Sensor Lane 0 to Serializer Lane 0 0bXX01: Map Sensor Lane 1 to Serializer Lane 0 0bXX10: Map Sensor Lane 2 to Serializer Lane 0 0bXX11: Map Sensor Lane 3 to Serializer Lane 0 0b00XX: Map Sensor Lane 0 to Serializer Lane 1 0b01XX: Map Sensor Lane 1 to Serializer Lane 1 0b10XX: Map Sensor Lane 2 to Serializer Lane 1 0b11XX: Map Sensor Lane 3 to Serializer Lane 1

MIPI_RX4 (0x334)

BIT	7	6	5	4	3	2	1	0
Field	–	phy1_pol_map[2:0]			–	–	–	–
Reset	–	0b000			–	–	–	–
Access Type	–	Write, Read			–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_pol_map	6:4	Serializer lane polarity setting for MIPI data lane 2 and 3	0bXX0: Normal Polarity for data lane 2 0bXX1: Inverse Polarity for data lane 2 0bX0X: Normal Polarity for data lane 3 0bX1X: Inverse Polarity for data lane 3 0b0XX: Reserved 0b1XX: Reserved

MIPI_RX5 (0x335)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	phy2_pol_map[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_pol_map	2:0	Serializer lane polarity setting for MIPI data lane 0, 1 and clock lane	0bXX0: Normal Polarity for data lane 0 0bXX1: Inverse Polarity for data lane 0 0bX0X: Normal Polarity for data lane 1 0bX1X: Inverse Polarity for data lane 1 0b0XX: Normal Polarity for clock lane 0b1XX: Inverse Polarity for clock lane

MIPI_RX7 (0x337)

BIT	7	6	5	4	3	2	1	0
Field	–	–	RSVD	RSVD[4:0]				
Reset	–	–	0b0	0b00000				
Access Type	–	–						

MIPI_RX8 (0x338)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		t_hs_settle[1:0]		RSVD[1:0]		t_clk_settle[1:0]	
Reset	0b01		0b01		0b01		0b01	
Access Type			Write, Read				Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_hs_settle	5:4	DPHY Mode: Set typical DPHY hs_settle timing in ns (at 2.5Gbps)	Value / Enumeration / Decode: 0b00 / / 132 (DPHY) 0b01 / / 139 (DPHY) 0b10 / / 153 (DPHY) 0b11 / / 166 (DPHY)
t_clk_settle	1:0	Set typical DPHY Tclk_settle timing in ns	0b00: 160 0b01: 220 0b10: 286 0b11: 352

MIPI_RX11 (0x33B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	phy1_lp_err[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_lp_err	4:0	Phy1 LP status (DPHY only)	0bXXXX1: Unrecognized Escape command received from data lane D0 0bXXX1X: Unrecognized Escape command received from CLK lane 0bXX1XX: Invalid line sequence detected from data lane D0 0bX1XXX: Invalid line sequence detected from data lane D1 0b1XXXX: Invalid line sequence detected from CLK lane

MIPI_RX12 (0x33C)

BIT	7	6	5	4	3	2	1	0
Field	phy1_hs_err[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_hs_err	7:0	PHY1 high-speed status (DPHY only)	0bXXXXXXX1: HS sync pattern with one bit error detected on data lane D0 0bXXXXXX1X: HS sync pattern with one bit error detected on data lane D1 0bXXXXX1XX: HS sync pattern with two or more bit errors detected on data lane D0 0bXXXX1XXX: HS sync pattern with two or more bit errors detected on data lane D1 0bXXX1XXXX: High speed receiver skew calibration failed on data lane D1 0bXX1XXXXX: High speed receiver skew calibration failed on data lane D0 0bX1XXXXXX: High speed receiver skew calibration run on data lane D1 0b1XXXXXXX: High speed receiver skew calibration run on data lane D0

MIPI_RX13 (0x33D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	phy2_lp_err[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_lp_err	4:0	Phy2 LP status (DPHY only)	0bXXXX1: Unrecognized Escape command received from data lane D0 0bXXX1X: Unrecognized Escape command received from CLK lane 0bXX1XX: Invalid line sequence detected from data lane D0 0bX1XXX: Invalid line sequence detected from data lane D1 0b1XXXX: Invalid line sequence detected from CLK lane

MIPI_RX14 (0x33E)

BIT	7	6	5	4	3	2	1	0
Field	phy2_hs_err[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_hs_err	7:0	PHY2 high-speed status (DPHY only)	0bXXXXXXX1: HS sync pattern with 2 or more bit errors detected on data lane D0 0bXXXXXX1X: HS sync pattern with 2 or more bit errors detected on data lane D1 0bXXXXX1XX: HS sync pattern with 1 bit error detected on data lane D0 0bXXXX1XXX: HS sync pattern with 1 bit error detected on data lane D1 0bXXX1XXXX: High speed receiver skew calibration failed on data lane D1 0bXX1XXXXX: High speed receiver skew calibration failed on data lane D0 0bX1XXXXXX: High speed receiver skew calibration run on data lane D1 0b1XXXXXXX: High speed receiver skew calibration run on data lane D0

MIPI_RX19 (0x343)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_csi_err_l[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_csi_err_l	7:0	CSI-2 Controller Status, low byte	0bXXXXXXX1: 1-bit ECC error detected 0bXXXXXX1X: 2-bit ECC error detected 0bXYYYYYXX: YYYYY = bit position of the 1-bit error 0b1XXXXXXX: CRC error detected

MIPI_RX20 (0x344)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ctrl1_csi_err_h[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Read Clears All		

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_csi_err_h	2:0	CSI-2 Controller Status, high bits	0bX1: Packets terminated early 0b1X: Frame count error detected

MIPI_RX21 (0x345)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_vc_map0[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_vc_map0	7:4	New virtual channel for VC=0. If ctrl_vc_map_en is set to 1, any time VC=0 is seen, the virtual channel number is replaced with the value in this register.	0xX: New virtual channel

MIPI_RX22 (0x346)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_vc_map1[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_vc_map1	7:4	New virtual channel for VC=1. If ctrl_vc_map_en is set to 1, any time VC=1 is seen, the virtual channel number is replaced with the value in this register.	0xX: New virtual channel

MIPI_RX23 (0x347)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_vc_map2[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_vc_map2	7:4	New virtual channel for VC=2. If ctrl_vc_map_en is set to 1, any time VC=2 is seen, the virtual channel number is replaced with the value in this register.	0xX: New virtual channel

MIPI_RX60 (0x36C)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_vc_map3[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Write, Read				–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ctrl1_vc_map3	7:4	New virtual channel for VC=3. If ctrl_vc_map_en is set to 1, any time VC=3 is seen, the virtual channel number is replaced with the value in this register.	0xX: New virtual channel

EXT11 (0x383)

BIT	7	6	5	4	3	2	1	0
Field	Tun_Mode	RSVD	–	–	RSVD	RSVD	RSVD[1:0]	
Reset	0x1	0x0	–	–	0x0	0x0	0x0	
Access Type	Write, Read		–	–				

BITFIELD	BITS	DESCRIPTION	DECODE
Tun_Mode	7	Select Tunnel mode	0x0: Select Pixel mode 0x1: Select Tunnel mode

EXT21 (0x38D)

BIT	7	6	5	4	3	2	1	0
Field	phy1_pkt_cnt[7:0]							
Reset	0b0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_pkt_cnt	7:0	MIPI PHY1 Packets Received	0xXX: Packets Received

EXT22 (0x38E)

BIT	7	6	5	4	3	2	1	0
Field	csi1_pkt_cnt[7:0]							
Reset	0b0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
csi1_pkt_cnt	7:0	MIPI Controller 1 Packets Processed	0xXX: Packets Processed

EXT23 (0x38F)

BIT	7	6	5	4	3	2	1	0
Field	tun_pkt_cnt[7:0]							
Reset	0b0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
tun_pkt_cnt	7:0	MIPI Tunnel Packets Processed	0xXX: Packets Processed

EXT24 (0x390)

BIT	7	6	5	4	3	2	1	0
Field	phy_clk_cnt[7:0]							
Reset	0b0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
phy_clk_cnt	7:0	MIPI RX Clock Received. The changing value indicates MIPI clock lane is running.	0xXX: MIPI RX Clock Count

FRONTTOP_EXT8 (0x3C8)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt3_selz[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt3_selz	7:0	Select a designated datatype to route to video pipeline Z for VS. Bits 7:6 are for selecting the two LSBs of the virtual channel. Bits 5:0 are for the datatype. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt3_selz_en and mem_dt4_selz_en are 0.	0b00XXXXXX: VC0,4,8,12, Designated datatype 0b01XXXXXX: VC1,5,9,13, Designated datatype 0b10XXXXXX: VC2,6,10,14, Designated datatype 0b11XXXXXX: VC3,7,11,15, Designated datatype

FRONTTOP_EXT9 (0x3C9)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt4_selz[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt4_selz	7:0	Select a designated datatype to route to video pipeline Z for VS. Bits 7:6 are for selecting the two LSBs of the virtual channel. Bits 5:0 are for the datatype. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt3_selz_en and mem_dt4_selz_en are 0.	0b00XXXXXX: VC0,4,8,12, Designated datatype 0b01XXXXXX: VC1,5,9,13, Designated datatype 0b10XXXXXX: VC2,6,10,14, Designated datatype 0b11XXXXXX: VC3,7,11,15, Designated datatype

FRONTTOP_EXT10 (0x3CA)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt5_selz[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt5_selz	7:0	Select a designated datatype to route to video pipeline Z for HS/DE. Bits 7:6 are for selecting the two LSBs of the virtual channel. Bits 5:0 are for the datatype. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt5_selz_en and mem_dt6_selz_en are 0.	0b00XXXXXX: VC0,4,8,12, Designated datatype 0b01XXXXXX: VC1,5,9,13, Designated datatype 0b10XXXXXX: VC2,6,10,14, Designated datatype 0b11XXXXXX: VC3,7,11,15, Designated datatype

FRONTTOP_EXT11 (0x3CB)

BIT	7	6	5	4	3	2	1	0
Field	mem_dt6_selz[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt6_selz	7:0	Select a designated datatype to route to video pipeline Z for HS/DE. Bits 7:6 are for selecting the two LSBs of the virtual channel. Bits 5:0 are for the datatype. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt5_selz_en and mem_dt6_selz_en are 0.	0b00XXXXXX: VC0,4,8,12, Designated datatype 0b01XXXXXX: VC1,5,9,13, Designated datatype 0b10XXXXXX: VC2,6,10,14, Designated datatype 0b11XXXXXX: VC3,7,11,15, Designated datatype

FRONTTOP_EXT17 (0x3D1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	mem_dt6_selz_en	mem_dt5_selz_en	mem_dt4_selz_en	mem_dt3_selz_en
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt6_selz_en	3	Enable datatype designated in mem_dt6_selz to route to video pipeline Z. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt5_selz_en and mem_dt6_selz_en are 0.	0b0: Disable 0b1: Enable
mem_dt5_selz_en	2	Enable datatype designated in mem_dt5_selz to route to video pipeline Z. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt5_selz_en and mem_dt6_selz_en are 0.	0b0: Disable 0b1: Enable
mem_dt4_selz_en	1	Enable datatype designated in mem_dt4_selz to route to video pipeline Z. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt3_selz_en and mem_dt4_selz_en are 0.	0b0: Disable 0b1: Enable
mem_dt3_selz_en	0	Enable datatype designated in mem_dt3_selz to route to video pipeline Z. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt3_selz_en and mem_dt4_selz_en are 0.	0b0: Disable 0b1: Enable

EXTA (0x3DC)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt7_selz[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt7_selz	6:0	Select designated datatype to route to video pipeline Z. Bit 6 is the enable. Bits 5:0 are for the datatype. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt1_selz[6], mem_dt2_selz[6], mem_dt7_selz[6], and mem_dt8_selz[6] are all 0.	0b0XXXXXX: Datatype selection disabled 0b1XXXXXX: Datatype enabled for datatype selected to route to video pipeline

EXTB (0x3DD)

BIT	7	6	5	4	3	2	1	0
Field	–	mem_dt8_selz[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
mem_dt8_selz	6:0	Select designated datatype to route to video pipeline Z. Bit 6 is the enable. Bits 5:0 are for the datatype. Used for filtering which datatypes are routed to video pipeline Z. If no filtering is enabled, then all datatypes are routed. This happens when mem_dt1_selz[6], mem_dt2_selz[6], mem_dt7_selz[6], and mem_dt8_selz[6] are all 0.	0b0XXXXXX: Datatype selection disabled 0b1XXXXXX: Datatype enabled for datatype selected to route to video pipeline

VTX0 (0x3E0)

BIT	7	6	5	4	3	2	1	0
Field	–	VS_TRIG	REF_VTG_MODE[1:0]		HS_INV	GEN_HS	VS_INV	GEN_VS
Reset	–	0b1	0b11		0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VS_TRIG	6	Select VS trigger edge (positive vs. negative polarity of VS)	0b0: Falling edge is VS trigger 0b1: Rising edge is VS trigger

BITFIELD	BITS	DESCRIPTION	DECODE
REF_VTG_MODE	5:4	Selects one of the following modes for video interface timing generation. Used when REF_VTG GEN_HS or GEN_VS are enabled. VS tracking mode. VS input's period (VS_HIGH + VS_LOW) is tracked. After VS tracking is locked, any VS input edge (glitches) not in the expected PCLK cycle is ignored. VS tracking is locked with three consecutive matches and unlocked by three consecutive mismatches. When unlocked or power-up, the next VS input edge is assumed to be the right VS edge. VS one-trigger mode. One VS input edge triggers the generation of one frame of VSO/HSO/DEO. If the next VS input edge comes earlier or later than expected by VS period, the newly generated frame is correct. The current VSO/HSO/DEO is cut or extended at the point of the rising edge of the newly generated VSO/HSO/DEO. Auto-repeat mode. VS input edge triggers the generation of continuous frames of VSO/HSO/DEO even if there are no more VS input edges. If next VS input edge comes earlier or later than expected by VS period, the newly generated frame is correct. The current VSO/HSO/DEO is cut or extended at the point of the rising edge of the newly generated VSO/HSO/DEO.	0b00: VS tracking mode 0b01: VS one trigger mode 0b10: Auto repeat mode 0b11: VS tracking mode
HS_INV	3	Invert HS output of video timing generator	0b0: Do not invert HS 0b1: Invert HS
GEN_HS	2	Enable generation of HS output	0b0: Disable generation of HS 0b1: Enable generation of HS
VS_INV	1	Invert VS output of video timing generator	0b0: Do not invert VS 0b1: Invert VS
GEN_VS	0	Enable generation of VS output	0b0: Disable generation of VS 0b1: Enable generation of VS

VTX1 (0x3E1)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_2	7:0	VS High Period in terms of PCLK cycles (Bits [23:16])	0xXX: VS high period high byte

VTX2 (0x3E2)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_1	7:0	VS High Period in terms of PCLK cycles (Bits [15:8])	0xXX: VS high period middle byte

VTX3 (0x3E3)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_0	7:0	VS High Period in terms of PCLK cycles (Bits [7:0])	0xXX: VS high period low byte

VTX4 (0x3E4)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_2	7:0	VS Low Period in terms of PCLK cycles (Bits [23:16])	0xXX: VS low period high byte

VTX5 (0x3E5)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_1	7:0	VS Low Period in terms of PCLK cycles (Bits [15:8])	0xXX: VS low period middle byte

VTX6 (0x3E6)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_0	7:0	VS Low Period in terms of PCLK cycles (Bits [7:0])	0xXX: VS low period low byte

VTX7 (0x3E7)

BIT	7	6	5	4	3	2	1	0
Field	V2H_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_2	7:0	Horizontal sync delay. VS edge to the rising edge of the first HS in terms of PCLK cycles (Bits [23:16])	0xXX: HS delay high byte

VTX8 (0x3E8)

BIT	7	6	5	4	3	2	1	0
Field	V2H_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_1	7:0	Horizontal sync delay. VS edge to the rising edge of the first HS in terms of PCLK cycles (Bits [15:8])	0xXX: HS delay middle byte

VTX9 (0x3E9)

BIT	7	6	5	4	3	2	1	0
Field	V2H_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_0	7:0	Horizontal sync delay. VS edge to the rising edge of the first HS in terms of PCLK cycles (Bits [7:0])	0xXX: HS delay low byte

VTX10 (0x3EA)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_1	7:0	HS High Period in terms of PCLK cycles (Bits [15:8])	0xXX: HS high period high byte

VTX11 (0x3EB)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_0	7:0	HS High Period in terms of PCLK cycles (Bits [7:0])	0xXX: HS high period low byte

VTX12 (0x3EC)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_1	7:0	HS Low Period in terms of PCLK cycles (Bits [15:8])	0xXX: HS low period high byte

VTX13 (0x3ED)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_0	7:0	HS Low Period in terms of PCLK cycles (Bits [7:0])	0xXX: HS low period low byte

VTX14 (0x3EE)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_1	7:0	Number of HS pulses per frame (Bits [15:8])	0xXX: HS pulses per frame high byte

VTX15 (0x3EF)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_0	7:0	Number of HS pulses per frame (Bits [7:0])	0xXX: HS pulses per frame low byte

REF_VTG1 (0x3F1)

BIT	7	6	5	4	3	2	1	0
Field	RCLKEN_Y	–	PCLK_GPIO[4:0]					PCLKEN
Reset	0b0	–	0b00000					0b0
Access Type	Write, Read	–	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RCLKEN_Y	7	Select between REFGEN_PLL output and RCLK to be the PCLK output specified in the PCLK_GPIO register	0b0: Select REFGEN_PLL output for PCLK output on MFP 0b1: Select RCLK output for PCLK output on MFP
PCLK_GPIO	5:1	Select which local MFP PCLK is outputted on. Possible MFPs are 0, 1, 2, 3, 4, 7, 8. Must have PCLKEN set to 1 to enable output.	0bXXXXX: MFP pin selected for PCLK output
PCLKEN	0	Enable output of PCLK on local MFP selected by PCLK_GPIO	0b0: Disable PCLK output on MFP 0b1: Enable PCLK output on MFP selected by PCLK_GPIO

REF_VTG2 (0x3F2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	HS_GPIO[4:0]					HSEN
Reset	–	–	0b00000					0b0
Access Type	–	–	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HS_GPIO	5:1	Select which local MFP HS is outputted on. Possible MFPs are 0,1, 2, 3, 4, 7, 8. Must have HSEN set to 1 to enable output.	0bXXXXX: MFP pin selected for HS output
HSEN	0	Enable output of HS on local MFP selected by HS_GPIO	0b0: Disable HS output on MFP 0b1: Enable HS output on MFP selected by HS_GPIO

REF_VTG3 (0x3F3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VS_GPIO[4:0]					VSEN
Reset	–	–	0b00000					0b0
Access Type	–	–	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VS_GPIO	5:1	Select which local MFP VS is outputted on. Possible MFPs are 0,1, 2, 3, 4, 7, 8. Must have VSEN set to 1 to enable output.	0bXXXXX: MFP pin selected for VS output
VSEN	0	Enable output of VS on local MFP selected by VS_GPIO	0b0: Disable VS output on MFP 0b1: Enable VS output on MFP selected by VS_GPIO

REF_VTG6 (0x3F6)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_2	7:0	VS Delay in terms of pixel clock cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (Bits [23:16])	0xXX: VS delay high byte

REF_VTG7 (0x3F7)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_1	7:0	VS Delay in terms of pixel clock cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (Bits [15:8])	0xXX: VS delay middle byte

REF_VTG8 (0x3F8)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_0	7:0	VS Delay in terms of pixel clock cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (Bits [7:0])	0xXX: VS delay low byte

REF_VTG9 (0x3F9)

BIT	7	6	5	4	3	2	1	0
Field	REF_VTG_TRIG_EN	–	–	REF_VTG_TRIG_ID[4:0]				
Reset	0b0	–	–	0b11110				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
REF_VTG_TRIG_EN	7	Enable receiving REF VTG trigger signal	0b0: Disable reception of REF VTG input signal 0b1: Enable reception of REF VTG input signal
REF_VTG_TRIG_ID	4:0	GPIO ID used for receiving REF_VTG_TRIG	0bXXXXX: GPIO ID selected for receiving REF_VTG_TRIG

HS_VS_Z (0x55F)

BIT	7	6	5	4	3	2	1	0
Field	–	DE_DET_Z	VS_DET_Z	HS_DET_Z	–	–	VS_POL_Z	HS_POL_Z
Reset	–	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET_Z	6	DE activity is detected on video pipeline Z	0x0: DE is not detected 0x1: DE is detected
VS_DET_Z	5	VS activity is detected on video pipeline Z	0x0: VS is not detected 0x1: VS is detected
HS_DET_Z	4	HS activity is detected on video pipeline Z	0x0: HS is not detected 0x1: HS is detected
VS_POL_Z	1	Detected VS polarity on video pipeline Z	0x0: Active low 0x1: Active high
HS_POL_Z	0	Detected HS polarity on video pipeline Z	0x0: Active low 0x1: Active high

PIO_SLEW_0 (0x56F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PIO02_SLEW[1:0]		PIO01_SLEW[1:0]		PIO00_SLEW[1:0]	
Reset	–	–	0b11		0b11		0b10	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
PIO02_SLEW	5:4	Slew rate setting for MFP2 pin. 00 value is the fastest rise and fall time, and 11 value is the slowest.
PIO01_SLEW	3:2	Slew rate setting for MFP1 pin. 00 value is the fastest rise and fall time, and 11 value is the slowest.
PIO00_SLEW	1:0	Slew rate setting for MFP0 pin. 00 value is the fastest rise and fall time, and 11 value is the slowest.

PIO_SLEW_1 (0x570)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PIO06_SLEW[1:0]		PIO05_SLEW[1:0]		–	–
Reset	–	–	0b11		0b11		–	–
Access Type	–	–	Write, Read		Write, Read		–	–

BITFIELD	BITS	DESCRIPTION
PIO06_SLEW	5:4	Slew rate setting for MFP4 pin. 00 value is the fastest rise and fall time, and 11 value is the slowest.
PIO05_SLEW	3:2	Slew rate setting for MFP3 pin. 00 value is the fastest rise and fall time, and 11 value is the slowest.

PIO_SLEW_2 (0x571)

BIT	7	6	5	4	3	2	1	0
Field	PIO011_SLEW[1:0]		PIO010_SLEW[1:0]		RSVD[1:0]		–	–
Reset	0b11		0b11		0b11		–	–
Access Type	Write, Read		Write, Read				–	–

BITFIELD	BITS	DESCRIPTION
PIO011_SLEW	7:6	Slew rate setting for MFP8 pin. 00 value is the fastest rise and fall time, and 11 value is the slowest.
PIO010_SLEW	5:4	Slew rate setting for MFP7 pin. 00 value is the fastest rise and fall time, and 11 value is the slowest.

EXT4 (0x584)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_fs_cnt_l[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ctrl1_fs_cnt_l	7:0	Frame start counter value of the virtual channel selected by FS_VC_SEL (low byte)

EXT5 (0x585)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_fs_cnt_h[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ctrl1_fs_cnt_h	7:0	Frame start counter value of the virtual channel selected by FS_VC_SEL (high byte)

EXT6 (0x586)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_fe_cnt_l[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ctrl1_fe_cnt_l	7:0	Frame end counter value of the virtual channel selected by FS_VC_SEL (low byte)

EXT7 (0x587)

BIT	7	6	5	4	3	2	1	0
Field	ctrl1_fe_cnt_h[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
ctrl1_fe_cnt_h	7:0	Frame end counter value of the virtual channel selected by FS_VC_SEL (high byte)

EXT8 (0x588)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ctrl1_fs_vc_sel[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
ctrl1_fs_vc_sel	3:0	Selected virtual channel for frame start/end count monitoring

RLMS4 (0x1404)

BIT	7	6	5	4	3	2	1	0
Field	EOM_CHK_AMOUNT[3:0]				EOM_CHK_THR[1:0]		EOM_PER_MODE	EOM_EN
Reset	0x4				0b10		0b1	0b1
Access Type	Write, Read				Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_CHK_AMOUNT	7:4	A factor (N) used to select the order of number of observations in each eye opening monitor window. N is used in the equation: Observations = 6.29 x 10^ (N + 2)	0xX: N factor
EOM_CHK_THR	3:2	Eye opening monitor number of error bits to allow in a measurement window	0b00: Allow no errors 0b01: Allow 1 error 0b10: Allow 2 errors 0b11: Allow 3 errors
EOM_PER_MODE	1	Eye opening monitor periodic mode enable	0b0: Eye opening monitor periodic mode disabled 0b1: Eye opening monitor periodic mode enabled
EOM_EN	0	Eye opening monitor enable	0b0: Eye opening monitor disabled 0b1: Eye opening monitor enabled

RLMS5 (0x1405)

BIT	7	6	5	4	3	2	1	0
Field	EOM_MAN_TRG_REQ	EOM_MIN_THR[6:0]						
Reset	0b0	0b0010000						
Access Type	Write Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MAN_TRG_REQ	7	Eye opening monitor manual trigger. For use when periodic mode is disabled.	0b0: No action 0b1: EOM manual trigger request
EOM_MIN_THR	6:0	The EOM minimum threshold as defined by the equation: % eye opening = EOM_MIN_THR/64. If measured, eye opening falls below this threshold, ERRB is triggered if enabled by EOM_ERR_FLAG_*. If the value is zero, the EOM is disabled.	0bXXXXXXX: EOM minimum threshold factor

RLMS6 (0x1406)

BIT	7	6	5	4	3	2	1	0
Field	EOM_PV_MODE	RSVD[6:0]						
Reset	0b1	0b0000000						
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_PV_MODE	7	Eye opening is measured vertically or horizontally	0b0: Vertical opening mode 0b1: Horizontal opening mode

RLMS7 (0x1407)

BIT	7	6	5	4	3	2	1	0
Field	EOM_DONE	EOM[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_DONE	7	Eye opening monitor measurement done	0b0: EOM not complete 0b1: EOM complete
EOM	6:0	Last completed EOM observation For horizontal eye opening measurement, eye opening is 2 x EOM/127 UI For vertical eye opening measurement, eye opening is EOM/127 UI	0bXXXXXXX: EOM measurement result

RLMS3A (0x143A)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntL[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
EyeMonValCntL	7:0	Eye monitor valid (hit) count (read-only)

RLMS3B (0x143B)

BIT	7	6	5	4	3	2	1	0
Field	EyeMonValCntH[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
EyeMonValCntH	7:0	Eye monitor valid (hit) count (read-only)

RLMS64 (0x1464)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[3:0]				–	RSVD	TxSSCMode[1:0]	
Reset	0x9				–	0b0	0b00	
Access Type					–		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCMode	1:0	Tx spread-spectrum mode	00: Manual phase mode (SSC disabled) 01: Reserved 10: Reserved 11: SSC enabled

RLMS70 (0x1470)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCFrqCtrl[6:0]						
Reset	–	0b0000001						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCFrqCtrl	6:0	Tx SSC modulation frequency deviation control (pp)	0x07: SSC 268 PPM 0x06: SSC 580 PPM 0x03: SSC 970 PPM 0x01: SSC 1750 PPM 0x01: SSC 2530 PPM others: Reserved

RLMS71 (0x1471)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCCenSprSt[5:0]						TxSSCEn
Reset	–	0b000001						0b0
Access Type	–	Write, Read						Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCCenSprSt	6:1	Tx SSC center spread starting phase	0x02: SSC 268 PPM 0x02: SSC 580 PPM 0x02: SSC 970 PPM 0x02: SSC 1750 PPM 0x02: SSC 2530 PPM others: Reserved
TxSSCEn	0	Tx spread spectrum enable	0b0: Tx spread spectrum disabled 0b1: Tx spread spectrum enabled

RLMS72 (0x1472)

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPreSclL[7:0]							
Reset	0xCF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclL	7:0	Tx SSC frequency prescaler bits 7:0. Decode values are for bits 7:0, concatenate with TXSSCPreSclH for final value.	0xC9: SSC 268 PPM 0xAB: SSC 580 PPM 0xAB: SSC 970 PPM 0xF9: SSC 1750 PPM 0xAB: SSC 2530 PPM others: Reserved

RLMS73 (0x1473)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TxSSCPreSclH[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPreSclH	2:0	Tx SSC frequency prescaler bits 10:8. Decode values are for bits 10:8, concatenate with TXSSCPreSclL for final value.	0x02: SSC 268 PPM 0x00: SSC 580 PPM 0x00: SSC 970 PPM 0x00: SSC 1750 PPM 0x00: SSC 2530 PPM others: Reserved

RLMS74 (0x1474)

BIT	7	6	5	4	3	2	1	0
Field	TxSSCPhL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhL	7:0	Tx SSC phase accumulator increment bits 7:0. Decode values are for bits 7:0, concatenate with TXSSCPhH for final value.	0xF9: SSC 268 PPM 0x63: SSC 580 PPM 0x63: SSC 970 PPM 0x2C: SSC 1750 PPM 0x63: SSC 2530 PPM others: Reserved

RLMS75 (0x1475)

BIT	7	6	5	4	3	2	1	0
Field	–	TxSSCPhH[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhH	6:0	Tx SSC phase accumulator increment bits 14:8. Decode values are for bits 14:8, concatenate with TXSSCPhL for final value.	0x01: SSC 268 PPM 0x07: SSC 580 PPM 0x07: SSC 970 PPM 0x05: SSC 1750 PPM 0x07: SSC 2530 PPM others: Reserved

RLMS76 (0x1476)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	TxSSCPhQuad[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TxSSCPhQuad	1:0	Tx SSC phase starting phase quadrant	0x00: SSC 268 PPM 0x00: SSC 580 PPM 0x00: SSC 970 PPM 0x00: SSC 1750 PPM 0x00: SSC 2530 PPM others: Reserved

RLMSA8 (0x14A8)

BIT	7	6	5	4	3	2	1	0
Field	FW_PHY_CTRL	FW_PHY_PU_TX	FW_PHY_RSTB	RSVD	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
FW_PHY_CTRL	7	PHY controller firmware mode enable. Other FW_* bits only take effect when this is set to 1.	0b0: Disabled 0b1: Enabled
FW_PHY_PU_TX	6	Override PHY controller output	0b0: Disabled 0b1: Enabled
FW_PHY_RSTB	5	Override PHY controller output	0b0: Reset asserted 0b1: Reset not asserted

RLMSA9 (0x14A9)

BIT	7	6	5	4	3	2	1	0
Field	FW_REPCAL_RSTB	RSVD	FW_TXD_SQUELCH	FW_TXD_EN	FW_RXD_EN	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
FW_REPCAL_RSTB	7	Override PHY controller output	0b0: Reset asserted 0b1: Reset not asserted
FW_TXD_SQUELCH	5	Override PHY controller output	0b0: Disabled 0b1: Enabled
FW_TXD_EN	4	Override PHY controller output	0b0: Disabled 0b1: Enabled
FW_RXD_EN	3	Override PHY controller output	0b0: Disabled 0b1: Enabled

EFUSE80 (0x1C50)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_0	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE81 (0x1C51)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_1	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE82 (0x1C52)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_2	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE83 (0x1C53)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_3	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE84 (0x1C54)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_4	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE85 (0x1C55)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_5[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_5	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE86 (0x1C56)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_6[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_6	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE87 (0x1C57)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_7[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_7	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE88 (0x1C58)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_8[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_8	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE89 (0x1C59)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_9[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_9	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE90 (0x1C5A)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_10[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_10	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE91 (0x1C5B)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_11[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_11	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE92 (0x1C5C)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_12[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_12	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE93 (0x1C5D)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_13[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_13	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE94 (0x1C5E)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_14[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_14	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE95 (0x1C5F)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_15[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_15	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE96 (0x1C60)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_16[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_16	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE97 (0x1C61)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_17[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_17	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE98 (0x1C62)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_18[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_18	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE99 (0x1C63)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_19[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_19	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE100 (0x1C64)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_20[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_20	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE101 (0x1C65)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_21[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_21	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE102 (0x1C66)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_22[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_22	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

EFUSE103 (0x1C67)

BIT	7	6	5	4	3	2	1	0
Field	SERIAL_NUMBER_23[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SERIAL_NUMBER_23	7:0	Serial Number. Can only be read through the deserializer across the GMSL link.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/21	Initial release	—
1	3/23	Added maximum supply noise specs for VDD	19
		Updated bandwidth calculations equation	33
		Hid OUT_TYPE for dedicated I2C pins in register map	101, 103
		Removed line fault register decode	59
		Updated TYP lock time spec to 45ms, updated link lock section	11, 32-33
		Updated device reset section. Added a note about one shot reset and removed sleep mode note	38-39
		Updated verbiage in tunneling and pixel mode section	41-42
		Removed sleep mode from the body of DS and register map	38, 60
		Added comment about using a 1M Ohm resistor to GND on ERRB pin	39
		Removed comment about supporting GPIO transitions of 1MHz.	35-36
		Unhid DIS_LOCAL_CC & DIS_REM_CC register bitfields	58
		Added comment about ADI supplying PMIC devices to pair with MAX96717R	39
		Updated verbiage on Note 2 under EC table	14
		Moved ESD table out of the EC table	20
		Updated thermal guidance verbiage "in still air"	8
		Added "*" to some default MFP pin functions	17
		Updated MIPI speed verbiage to stay consistent to 600Mbps max	26, 42
		Updated DS verbiage and register decode to state only 4 lanes is supported	42, 110
		Updated SION pin description verbiage	16
		Removed external clock EC table	13

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