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Product Change Notification / SYST-01PBDY542

Date:

02-May-2023

Product Category:

Motor Drivers

PCN Type:

Document Change

Notification Subject:

ERRATA - MCP8025A/6 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-01PBDY542_Affected_CPN_05022023.pdf
SYST-01PBDY542_Affected_CPN_05022023.csv

Notification Text:

SYST-01PBDY542

Microchip has released a new Errata for the MCP8025A/6 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at MCP8025A/6 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: Initial release of this document.

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 02 May 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

MCP8025A/6 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

MCP8025A-115E/MP
MCP8025A-115E/PT
MCP8025A-115H/MP
MCP8025A-115H/MPVAO
MCP8025A-115H/PT
MCP8025AT-115E/MP
MCP8025AT-115E/PT
MCP8025AT-115H/MP
MCP8025AT-115H/MPV05
MCP8025AT-115H/MPVAO
MCP8025AT-115H/PT
MCP8026-115E/MP
MCP8026-115E/MPB3
MCP8026-115E/PT
MCP8026-115E/PTVB3
MCP8026-115H/MP
MCP8026-115H/PT
MCP8026T-115E/MP
MCP8026T-115E/MPB3
MCP8026T-115E/PT
MCP8026T-115E/PTVB3
MCP8026T-115H/MP
MCP8026T-115H/PT
MCP8026T-115H/PTVAO

MCP8025A/6

MCP8025A/6
Silicon Errata and Data Sheet Clarification

The functionality of the MCP8025A/6 devices is described in the Device Data Sheet (DS20005905), except for the anomalies described below.

1. Module: V_{BOOT} Not Ready

When CE toggles from a logic '0' to a logic '1', V_{BOOT} must attain 10.8V before the driver outputs will be enabled. If the PWM inputs change state before V_{BOOT} attains 10.8V, the driver outputs will not change and no driver Fault will be issued.

Fix/Work Around:

When setting CE = 1 from Standby mode, allow time for the V_{BOOT} capacitor to charge up to 10.8V. Typical time is 250 μs.

Devices:

All

2. Module: PWM Pulse Width = Driver Dead-Time Pulse Width

When the PWM input pulse width is the same as the driver programmed dead time, a dead-time race condition may occur that forces both driver outputs to go low until both PWM inputs go low again. Normally, the PWM pulse width is longer than the dead time in order to generate an output pulse equal to PWM_PULSEWIDTH – DEAD TIME. However, some systems allow the PWM pulse width to be smaller than the driver dead time, knowing that there will be no driver output.

Fix/Work Around:

Set up host minimum PWM pulse width to be at least 50 ns larger or smaller than driver dead-time setting.

Devices:

All

3. Module: Motor Driver Lock

It has been detected that the motor driver may be locked after a momentary drop of V_{DD} below the minimum operating voltage or after enabling the driver output when using low V_{GS} threshold MOSFETs (V_{GS} < 1.1V). The issue was traced back to the high-side driver operation at voltages below the minimum operating voltage.

Fix/Work Around:

None.

Devices:

MCP8026 – Date codes prior to YYWW = 1635

4. Module: External MOSFET DUVLO and OCP Detection

These detection functions could flag an inexistent motor driver undervoltage or power MOSFET overcurrent Fault when a DE2 message was sent to enable the functions while the motor was running.

Fix/Work Around:

Stop the motor before enabling the external MOSFET UVLO and OCP protection, and try to keep the blanking time as long as the motor application allows.

Devices:

MCP8025A – All date codes
MCP8026 – Date codes prior to YYWW = 1635

5. Module: External MOSFET DUVLO and OCP Fault

When a resistor is used in series with the VBx bootstrap pins, an external MOSFET undervoltage Fault and/or Overcurrent Protection Fault may occur. This is caused by the voltage drop across the resistor when the complementary driver transistors switch state. The switching overlap may draw enough current to lower the voltage long enough to trigger the Fault. Increasing the bootstrap capacitance and charge time will provide more energy storage.

Fix/Work Around:

When a series VBx bootstrap resistor is used with short duration OFF time duty cycles (< 8%), the value should be kept below 4 ohms.

Devices:

All

MCP8025A/6

6. Module: Buck Overvoltage

It has been observed that the buck output voltage may exceed the target voltage for less than 1.5 ms, after power-up, under certain power-up scenarios. The issue is caused by an unintended current that may flow into the FB pin, causing an additional voltage drop across the resistor R1 (high-side of resistor divider), from the buck output to the FB pin. The overvoltage has only been observed on an application with no resistive load on the +5V LDO output to discharge the 5V LDO capacitor to 0V before the system is powered up again, but it cannot be excluded that other applications may also be affected.

Fix/Work Around:

The overvoltage will be minimized if the resistor selection for the low-side of the resistor voltage divider (R2) is 620 ohms or less. More information on R2 may be found in Section 5.1.3.3 "Setting the Buck Output Voltage" of the MCP8025A/6 Device Data Sheet (DS20005905).

Devices:

MCP8025A – Date codes prior to YYWW = 2240
MCP8026 – Date codes prior to YYWW = 2240

7. Module: Minimum Fault Clearing Pulse Width

It is detected that the minimum Fault clearing pulse-width parameter is too narrow for the CE pin input filter. The correct minimum Fault clearing pulse width is 4 μs.

Fix/Work Around:

The host should generate a minimum Fault clearing pulse width of 4 μs.

Devices:

All

8. Module: Start-up DE2 Message

A STAT1 message with the BORW bit set is sent one time by the MCP802X device upon start-up. The message is immediately sent when either the CE pin goes high or when the DE2 pin goes low. This may cause a collision with a host message.

Fix/Work Around:

Pulse the CE pin low-high-low at start-up before sending any messages to the MCP802X device. This triggers the MCP802X to send the BORW message and prevent any collision.

Devices:

All

9. Module: Buck Start-up Issue

It has been detected that when V_{DD} rises faster than 0.083 [V/μs], the driver could enter Sleep mode.

Fix/Work Around:

Keep V_{DD} slew rate slower than 0.083 [V/μs]. If this is not possible, the device could leave Sleep mode via the CE or LIN signals.

Devices:

All

10. Module: POR Triggered on Standby and V_{DD} Step-down

It has been detected that when having V_{DD} over the charge pump activation threshold – and then reducing V_{DD} back to below this value during standby mode – at the next CE activation the part will trigger a POR. This is caused by the CP capacitor charging with a voltage greater than the actual V_{DD} and in the next startup the part is trying to start the CP circuit. The CP2 pin is connected to V_{DD} before the CP1 connection to GND and the negative voltage applied may affect the internal circuitry. After 1-3 trials, the driver will start successfully.

Fix/Work Around:

Keep the V_{DD} constant during Standby mode (or an additional discharging circuit may be added on CP2 pin if it is required by the system).

It is recommended to keep the CP capacitor lower than 220 nF.

Devices:

MCP8025A – Date codes prior to YYWW = 2240
MCP8026 – Date codes prior to YYWW = 2240

APPENDIX A: REVISION HISTORY

Revision A (May 2023)

- Initial release of this document.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.

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