Product Change Notification / SYST-08DHBJ472

Date:

10-May-2023

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18F26/46/56Q84 Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-08DHBJ472_Affected_CPN_05102023.pdf
SYST-08DHBJ472_Affected_CPN_05102023.csv

Notification Text:

SYST-08DHBJ472

Microchip has released a new Errata for the PIC18F26/46/56Q84 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC18F26/46/56Q84 Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change: Added silicon issue 1.1.4 to UTMR module as well as new errata 1.2.1-1.10.1 . Added new errata entry to UTMR module. Added data sheet clarifications 2.2, 2.3, 2.4, 2.5, and 2.6

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 10 May 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18F26/46/56Q84 Silicon Errata and Data Sheet Clarifications

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Affected Catalog Part Numbers (CPN)

PIC18F26Q84-E/5N
PIC18F26Q84-E/SO
PIC18F26Q84-E/SP
PIC18F26Q84-E/SS
PIC18F26Q84-I/5N
PIC18F26Q84-I/SO
PIC18F26Q84-I/SP
PIC18F26Q84-I/SS
PIC18F26Q84T-E/SS
PIC18F46Q84-E/NHX
PIC18F46Q84-E/P
PIC18F46Q84-E/PT
PIC18F46Q84-I/NHX
PIC18F46Q84-I/P
PIC18F46Q84-I/PT
PIC18F56Q84-E/6MX
PIC18F56Q84-E/PT
PIC18F56Q84-I/6MX
PIC18F56Q84-I/PT
PIC18F56Q84T-I/PT

PIC18F26/46/56Q84 Silicon Errata and Data Sheet Clarifications

PIC18F26/46/56Q84

The PIC18F26/46/56Q84 devices that you have received conform functionally to the current device data sheet (DS40002259C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F26/46/56Q84 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		A1	A2
PIC18F26Q84	0xA300	0xA001	0xA002
PIC18F46Q84	0xA301	0xA001	0xA002
PIC18F56Q84	0xA302	0xA001	0xA002

Important: Refer to the **Device/Revision ID** section in the current **"PIC18FXXQ84 Family Programming Specification"** (DS40002137C) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A1	A2
UTMR	Level-triggered ERS Start/Reset condition	1.1.1	Dead zone exists in level-triggered Start/Reset condition when ERS signal is generated due to an SFR access	X	X
	Hardware Reset condition	1.1.2	Reset does not happen at period match when the prescaler > 0 and the Timer Stops at Period Match (includes One Shot mode)	X	X
	Output Pulse	1.1.3	Pulse output does not occur at Period Match when the Prescaler = 1	X	X
	Clear Command	1.1.4	Clear Command May Not Work Properly	X	X
I^2C	Start and Stop Interrupt Function	1.2.1	The I^2C Start and/or Stop flags may be set when I^2C is enabled	X	X
SMT	Reset Bit	1.3.1	SMT Stops working if RST is set while prescaler setting is not zero	X	X
ADCC with Context	Double Sample Conversions	1.4.1	An unexpected acquisition time is added between the first and second conversion	X	X
PIC18 Core	FSR Shadow Registers	1.5.1	FSR shadow registers are not writable	X	X
UART	Stop bit	1.6.1	TXDE signal may go low before the STOP bit has been entirely transmitted	X	X
ICD	Single-Step Function (SSTEP)	1.7.1	Single Step function does not execute at Software Breakpoint.	X	X
PWM	PWM Mode	1.8.1	Wrong Duty Cycle for CCP Module	X	X
ICSP™	Low-Voltage Programming (LVP)	1.9.1	Low Voltage Programming is not possible when VDD is below BORV while BOR is enabled.	X	X
CAN FD	Masks/Filters	1.10.1	Filters 8-11 will erroneously accept incoming messages with SID of 0x000	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

CAUTION **Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Universal Timer (UTMR) Module

1.1.1 Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = 'b11 or RESET = 'b01) is triggered by an ERS signal generated by an SFR access such as TUxyPRL_Write or TUxyTMRL_Read or TUxyCRL_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

Work around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

Affected Silicon Revisions

A1	A2
X	X

1.1.2 Reset Does Not Happen at Period Match When the Prescaler > 0 and the Timer Stops at Period Match

When the prescaler > 0 and the timer is configured to reset at a hardware-based event (RESET = 'b01 or 'b10 or 'b11) and stop at period match (STOP = `b11), the timer stops at period match but does not reset (no pulse output occurs and ZIF interrupt is not generated).

Work around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

Affected Silicon Revisions

A1	A2
X	X

1.1.3 Pulse Output Does Not Occur at Period Match When the Prescaler = 1

The timer output pulse will not occur at period match when prescaler = 1.

Work around

Use prescaler = 0 or prescaler > 1 when a pulse output is desired.

Affected Silicon Revisions

A1	A2
X	X

1.1.4 Clear Command May Not Work Properly in Asynchronous Mode

When operating in asynchronous mode (CSYNC = 0), setting the Clear Command bit (CLR= 1) may not clear the Timer Counter register value.

Work around

Use the Universal Timer module in synchronous mode (CSYNC = 1) when Clear Command bit (CLR) is being used.

Affected Silicon Revisions

A1	A2
X	X

1.2 Module: Inter-Integrated Circuit (I^2C)

1.2.1 The I^2C Start and/or Stop Flags May Be Set When I^2C Is Enabled

When I^2C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I^2C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I^2C module.
3. Wait 250 ns + six instructions cycles ($F_{OSC}/4$).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;         // Disable Start condition interrupt
I2CxPIEbits.PCIE = 0;         // Disable Stop condition interrupt
I2CxCON0bits.EN = 1;          // Enable I2C
Delay();                      // Wait for 250 ns + 6 instruction cycles (FOSC/4)
I2CxPIRbits.SCIF = 0;         // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0;         // Clear the Stop condition interrupt flags
I2CxPIEbits.SCIE = 1;         // Enable Start condition interrupt if used
I2CxPIEbits.PCIE = 1;         // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

A1	A2
X	X

1.3 Module: Signal Measurement Timer (SMT)

1.3.1 Reset Bit

If the SMT clock prescaler is set to any value other than '00', setting the RST bit will cause the module to stop working. The RST bit will remain at the value '1', the counter will not increment, and no interrupts will be generated. The problem is cleared by turning the module off and on, or by a device reset.

Work around

Method 1:

Do not set the RST bit; manual reset is usually not required for typical operation because the measurement logic will reset the counter automatically.

Method 2:

Write zero to the counter manually. The module enable or the clock should be disabled when using this method.

Method 3:

Use 1:1 prescaler (PS = 00).

Method 4:

Use the CLKREF subsystem to provide a prescaled clock and set PS = 00.

Affected Silicon Revisions

A1	A2
X	X

1.4 Module: Analog-to-Digital Converter with Computation and Context Switching (ADC)

1.4.1 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1) with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion. The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

Method 1:

Disable Double Sample Conversion (DSEN = 0) and perform two single conversions back to back.

Method 2:

If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

A1	A2
X	X

1.5 Module: PIC18 Core

1.5.1 FSR Shadow Registers Are Not Writable

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM.
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below).
3. Write the shadow FSRxL (data doesn't matter), this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 (IR[6:0]).
5. Write FSRxH.

6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

Affected Silicon Revisions

A1	A2
X	X

1.6 Module: Universal Asynchronous Receiver Transmitter (UART)

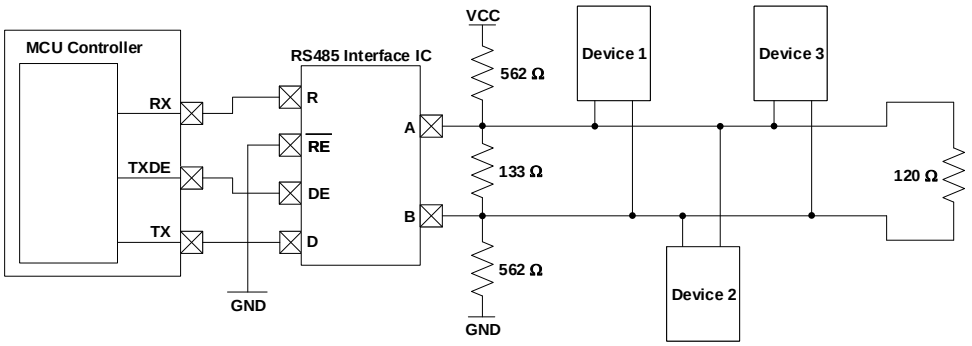
1.6.1 UART TXDE Signal May Go Low Before the STOP Bit Has Been Entirely Transmitted

The UART Transmit Drive Enable (TXDE) signal could potentially transition into a low state before the UART STOP bit has been entirely transmitted due to the effects of parasitic capacitance on the TX line. In some applications, this could result in communication being prematurely terminated due to the TXDE bit going low before the STOP bit has had enough time to settle.

Work around

To ensure that the STOP bit settles into its final logic state before the TXDE signal transitions low, a biasing circuit can be implemented. A biasing circuit allows the TX line to either be driven high or low, rather than being left in a floating tri-state mode where prolonged rise or fall times could lead to communication being disrupted. This bias circuit should only be implemented on one end of the serial bus, and a termination resistor should be used on the other end. The figure below show an example of a bias circuit that can be used to achieve this.

Please note that the resistor values used in this circuit are recommendations, and that the actual resistor values required may vary based on the application.



Affected Silicon Revisions

A1	A2
X	X

1.7 Module: In-Circuit Debug

1.7.1 Single Step Function Does Not Execute at SW Breakpoint

The SW breakpoint occurs, but the SSTEP function does not execute at the breakpoint.

Work around

None.

Affected Silicon Revisions

A1	A2
X	X

1.8 Module: Pulse-Width Modulation (PWM)

1.8.1 Wrong Duty Cycle for CCP Module

While in PWM mode and the Timer2 prescaler is configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1 while T2PR = 0 (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

Table 1-1. Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:4...1:128	75%	75%	75%	75%	100%

Work around

None.

Affected Silicon Revisions

A1	A2
X	X

1.9 Module: Low-Voltage In-Circuit Serial Programming™ (LVP)

1.9.1 Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V_{DD} is below the selected BORV voltage level while BOR is enabled.

Work around

Method 1:

Disable BOR to use Low-Voltage Programming.

Method 2:

Raise V_{DD} above the selected BORV level while using Low-Voltage Programming.

Affected Silicon Revisions

A1	A2
X	X

1.10 Module: Controller Area Network Flexible Data-Rate (CAN FD) Module

1.10.1 Filters 8-11 Will Erroneously Accept Incoming Messages With SID of 0x000

When using the CAN RX filters 8-11, any messages where the incoming message after masking is SID 0x000 will trigger a filter match, regardless of the filter ID settings. For example: an incoming message with ID of 0x350 and a mask setting of 0x00F will trigger a filter match regardless of other mask/filter settings. This will occur even if the filter is set to only accept extended IDs.

Work around

If using CAN RX filters 8-11, check the FILHIT bits of C1VECH (or the received message object) upon message reception. If the value of FILHIT is greater than 11, then this error has occurred and the message can be ignored and discarded.

Affected Silicon Revisions

A1	A2

X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40002259C):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 Memory Programming Specifications

The flash memory cell endurance specification is reduced to **1k** minimum. The corresponding parameter (E_P) will be updated in the next revision of datasheet (DS40002259).

Table 2-1. Memory Programming

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions
Data EEPROM Memory Specifications							
MEM20	E_D	DataEE Byte Endurance	100k	—	—	E/W	-40°C ≤ T_A ≤ +85°C
MEM21	T_{D_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM22	N_{D_REF}	Total Erase/Write Cycles before Refresh	1M	4M	—	E/W	-40°C ≤ T_A ≤ +85°C
MEM23	V_{D_RW}	V_{DD} for Read or Erase/Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM24	T_{D_BEW}	Byte Erase and Write Cycle Time	—	—	11	ms	
Program Flash Memory Specifications							
MEM30	**E_P**	**Flash Memory Cell Endurance**	**1k**	—	—	**E/W**	**-40°C ≤ T_A ≤ +85°C (Note 1)**
MEM32	T_{P_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM33	V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM34	V_{P_REW}	V_{DD} for Row Erase or Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM35	T_{P_REW}	Self-Timed Page Write	—	—	10	ms	
MEM36	T_{SE}	Self-Timed Page Erase	—	—	11	ms	
MEM37	T_{P_WRD}	Self-Timed Word Write	—	—	75	µs	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. Flash Memory Cell Endurance for the Flash memory is defined as: One Row Erase operation and one Self-Timed Write.

2.2 Packages

Table 1-1: Packages lists incorrect dimensions for the 28-pin VQFN package. The corrected table is below.

Table 2-2. Packages

Device	28-pin SPDIP	28-pin SOIC	28-pin SSOP	28-pin VQFN **6x6x1**	40-pin PDIP	40-pin VQFN 5x5x0.9	44-pin TQFP	48-pin TQFP 7x7x1	48-pin VQFN 6x6x0.9
PIC18F26Q84	•	•	•	•					
PIC18F46Q84					•	•	•		
PIC18F56Q84								•	•

2.3 Incorrectly listed maximum data rate

The maximum data rate listed in the **General** section of the CAN FD chapter is incorrect. The corrected list item in the **General** section is below

- Data bit rate up to **8** Mbps (dependent on oscillator selection)

2.4 Bit Time Configuration Example

Tables 38-3 through 38-5 have incorrect example values in them. Corrected values are listed below

Table 2-3. Step-by-Step Nominal Bit Rate Configuration

Parameter	Constraint	Value	Unit
NBT	NBT ≥ µs	2	µs
F_{SYSCLK}	F_{SYSCLK} ≤ 40 MHz	40	MHz
NBRP	1 to 256	1	-
NTQ	NBT, F_{SYSCLK}	**25**	ns
NBT/NTQ	4 to 385	**80**	-
NSYNC	Fixed	1	NTQ
NPRSEG	NPRSEG > T_{PROP}	**47**	NTQ
NTSEG1	2 to 256 NTQ	**64**	NTQ
NTSEG2	1 to 128 NTQ	**16**	NTQ
NSJW	1 to 128 NTQ; SJW ≤ min(NPHSEG1, NPHSEG2)	**16**	NTQ

Table 2-4. Step-by-Step Data Bit Rate Configuration

Parameter	Constraint	Value	Unit
DBT	DBT ≥ 125 ns	500	ns
DBRP	1 to 256	1	-
DTQ	DBT, F_{SYSCLK}	**25**	ns
DBT/DTQ	3 to 49	**20**	-
DSYNC	Fixed	1	DTQ
DTSEG1	1 to 32 DTQ	**16**	DTQ
DTSEG2	1 to 16 DTQ	**4**	DTQ
DSJW	1 to 16 DTQ; SJW≤min (DPHSEG1, DPHSEG2)	**4**	DTQ
Oscillator Tolerance Conditions 1-5	Minimum of Conditions 1-5	.78	%

Table 2-5. Bit Time Register Initialization (500k/2M)

CxNBTCFG	Value	CxDBTCFG	Value	CxTDC	Value
BRP[7:0]	0	BRP[7:0]	0	TDCMOD[1:0]	2
TSEG[7:0]	63	TSEG[7:0]	15	TDCO[6:0]	31
TSEG2[6:0]	15	TSEG2[6:0]	3	TDCV[5:0]	0
SJW[6:0]	15	SJW[6:0]	3	-	-

2.5 Reading a TEF Object

The address given in the note after equation 38-21 is incorrect. The corrected note is below.

Note: CxFIFOBAH/L needs to be set to a value between **0x2600** and the end of RAM, leaving enough room to allow the TEF and Transmit Queue (if enabled) as well as the FIFOs.

2.6 Auto-Load I2CxCNT

The Auto-Load I2CxCNT data sheet segment text incorrectly describes the auto-load feature as loading both the low and high bytes of I2CxCNT, when it actually only loads I2CxCNTL. Corrected text is below.

The **I2CxCNTL** register can be automatically loaded. Auto-loading of the I2CxCNTL register is enabled when the Auto-Load I^2C Count Register Enable (ACNT) bit is set (ACNT=1).

In Host Transmit mode, the first **byte** following either the 7-bit or 10-bit client address **is** transferred from I2CxTXB into both **I2CxCNTL** and the transmit shift register.

In Host Reception mode, the first **byte** received from the client is loaded into both **I2CxCNTL** and I2CxRXB. The value of the Acknowledge Data (ACKDT) bit is used as the host's acknowledgement response to prevent a false NACK from being generated before the **I2CxCNTL** register is updated with the new count value.

In Client Reception mode, the first **byte** received after a receiving a matching 7-bit or 10-bit address are loaded into both **I2CxCNTL** and I2CxRXB, and the value of the ACKDT bit is used as the client's acknowledgement response.

In Client Transmit mode, the first **byte** loaded into I2CxTXB following the reception of a matching 7-bit or 10-bit address is transferred into both **I2CxCNTL** and the transmit shift register.

Important: It is not necessary to preload the I2CxCNT register when using the auto-load feature. If no value is loaded by the 9th falling SCL edge following an address transmission or reception, the Byte Count Interrupt Flag (CNTIF) will be set by module hardware, and must be cleared by software to prevent an interrupt event before **I2CxCNTL** is updated. Alternatively, **I2CxCNTL** can be preloaded with a nonzero value to prevent the CNTIF from being set. In this case, the preloaded value will be overwritten once the new count value has been loaded into **I2CxCNTL**.

3. Appendix A: Revision History

Doc. Rev.	Date	Comments
C	5/2023	Added silicon issue 1.1.4 to UTMR module as well as new errata 1.2.1-1.10.1 . Added new errata entry to UTMR module. Added data sheet clarifications 2.2, 2.3, 2.4, 2.5, and 2.6
B	06/2022	Added data sheet clarification 2.1.
A	2/2021	Initial document release.

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