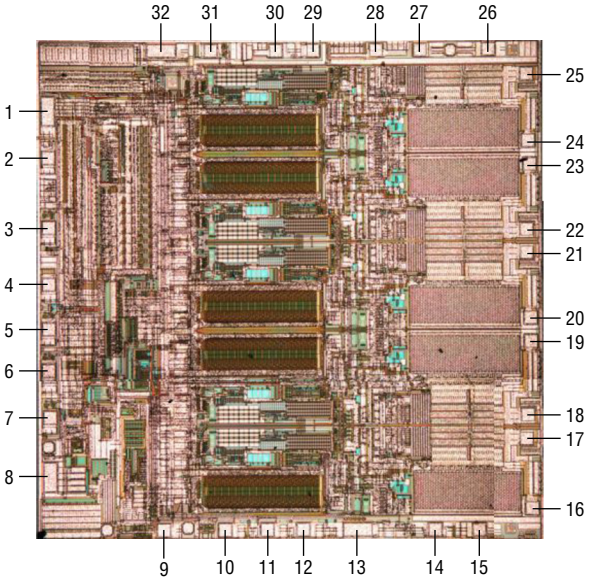
ANALOG DEVICES

# DICE/DWF SPECIFICATION

# LTC2662-16
# 5-Channel, 300mA Current-Source-Output 16-Bit SoftSpan™ DACs




140mils × 138mils
Backside metal: None
Backside potential: GND

## PAD FUNCTION

1. GND
2. TGP
3. SDI
4. SDO
5. SCK
6. $\overline{CS}$/LD
7. $\overline{LDAC}$
8. GND
9. REFLO
10. REF
11. REFCOMP
12. FSADJ
13. $V_{CC}$
14. GND
15. $V^-$
16. OUT4
17. $V_{DD4}$
18. $V_{DD3}$
19. OUT3
20. OUT2
21. $V_{DD2}$
22. $V_{DD1}$
23. OUT1
24. OUT0
25. $V_{DD0}$
26. $V^-$
27. $V^+$
28. MUX
29. $IOV_{CC}$
30. $\overline{FAULT}$
31. $\overline{CLR}$
32. GND

## DIE CROSS REFERENCE

| LTC Finished Part Number | Order Part Number |
|---|---|
| **LTC2662-16** | **LTC2662-16DWF#6AJ**<br>**LTC2662-16DICE#6AJ** |

**Please refer to LTC2662-16 standard product data sheet for other applicable product information.**

***DWF = DICE in wafer form.**



## DICE/DWF ELECTRICAL TEST LIMITS

**$T_J$ = 25°C. $V_{CC}$ = $IOV_{CC}$ = 5V; $V^-$ = –5V; $V_{DD0-4}$ = 5V; $V^+$ = 5V; FSADJ = $V_{CC}$, $V_{REF}$ = 1.25V External, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC Performance All Ranges (Note 2)** | | | | | | |
| | Resolution | | 16 | | | Bits |
| | Monotonicity | (Note 1) | 16 | | | Bits |
| DNL | Differential Nonlinearity | (Note 1) | | ±0.2 | ±1 | LSB |
| INL | Integral Nonlinearity | (Note 1) | | ±12 | ±64 | LSB |
| IOS | Offset Error Current | (Note 1) | | ±0.1 | ±0.4 | %FSR |
| GE | Gain Error (Note 2) | 300mA, 200mA, 100mA Ranges | | 0.3 | 0.9 | %FSR |
| | | 50mA, 25mA Ranges | | 0.4 | 1.2 | %FSR |
| | | 12.5mA, 6.25mA, 3.125mA Ranges | | 0.7 | 1.5 | %FSR |
| TUE | Total Unadjusted Error (Note 2) | 300mA, 200mA, 100mA Ranges | | 0.4 | 1.4 | %FSR |
| | | 50mA, 25mA Ranges | | 0.5 | 1.7 | %FSR |
| | | 12.5mA, 6.25mA, 3.125mA Ranges | | 0.8 | 2 | %FSR |
| **DC Performance** | | | | | | |
| $V_{DROPOUT}$ | Dropout Voltage ($V_{DDX}$ – $V_{OUTX}$) (Notes 2, 3) | $I_{OUTX}$ ≤ 200mA, ($V_{DDX}$ – $V^-$) = 4.75V | | 0.7 | 1 | V |
| | Hi-Z Output Leakage Current | $I_{OUTX}$ = Hi-Z, ($V_{DDX}$ – $V^-$) = 4.75V | | 0.1 | 1 | µA |
| $R_{PULL-DOWN}$ | OUTX Pull-Down Switch Resistance to $V^-$ Supply | Span Code = 1000b, Sinking 50mA | | 8 | 12 | Ω |
| **Reference** | | | | | | |
| $V_{REF}$ | Reference Output Voltage | Internal Reference | 1.248 | 1.25 | 1.252 | V |

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| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{CC}$ | Analog Supply Voltage | $V_{CC}$ Must Not Exceed $V^+$ | 2.85 | | 5.5 | V |
| $IO_{VCC}$ | Digital I/O Supply Voltage | | 1.71 | | $V_{CC}$ | V |
| $V^-$ | Negative Supply Voltage | | –15.75 | | 0 | V |
| $V^+$ | Positive Supply Voltage | | 2.85 | | $V^-$ + 33 | V |
| $V_{DD0}$ to $V_{DD4}$ | Output Supply Voltages | | 2.85 | | $V^+$ | V |
| | Supply Current $V_{CC}$ | All Ranges (Code = 0, All Channels) | | 2.6 | 3.8 | mA |
| | Supply Current $IOV_{CC}$ | All Ranges (Code = 0, All Channels) | | 0.01 | 2 | µA |
| | Supply Current $V^+$ | All Ranges (Code = 0, All Channels) | | 385 | 500 | µA |
| | Supply Current $V^-$ | All Ranges (Code = 0, All Channels) | | 2.3 | 3.2 | mA |
| | Supply Current $V_{DD0-4}$ | All Ranges (Code = 0, per Channel) | | 0.7 | 1.2 | mA |
| $I_{SLEEP}$ | Shutdown Current $V_{CC}$ | (Note 4) | | 1 | 10 | µA |
| | Shutdown Current $IO_{VCC}$ | (Note 4) | | 0.01 | 2 | µA |
| | Shutdown Current $V^+$ | (Note 4) | | 20 | 45 | µA |
| | Shutdown Current $V^-$ | (Note 4) | | 30 | 65 | µA |
| | Shutdown Current $V_{DD0-4}$ | (Note 4) per Channel | | 4.2 | 8.1 | µA |

**Note 1:** Linearity is defined from code 384 to code 65,535. Offset current is measured at code 384.

**Note 2:** Wafer probe testing is performed at output currents of up to 100mA. Output currents over 100mA are guaranteed by design and characterization.

**Note 3:** Test conditions: 200mA range; $I_{OUTx}$ = 100mA.

**Note 4:** Digital Inputs at 0V or $IOV_{CC}$.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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