MP6545A

45V, 2.5A, Simple Three-Phase Power Stage with Current Measurement

DESCRIPTION

The MP6545A is a three-phase power stage IC designed to drive brushless DC (BLDC) motors or other loads.

The MP6545A operates across a 4.5V to 45V input voltage (V_{IN}) range. It can deliver an output current (I_{OUT}) up to 2.5A per phase, depending on the ambient temperature (T_A) and PCB layout.

The MP6545A has unique, independent GND pins for each half-bridge. These GND pins make it possible to provide current measurement via an external shunt resistor for different application requirements.

Internal safety and diagnostic features include over-current protection (OCP), input over-voltage protection (OVP), input under-voltage lockout (UVLO), and thermal shutdown.

The MP6545A has separate high-side (HS) and low-side (LS) input pins for each output pin. The MP6545A is available in QFN-28 (4mmx5mm) and TSSOP-28EP packages.

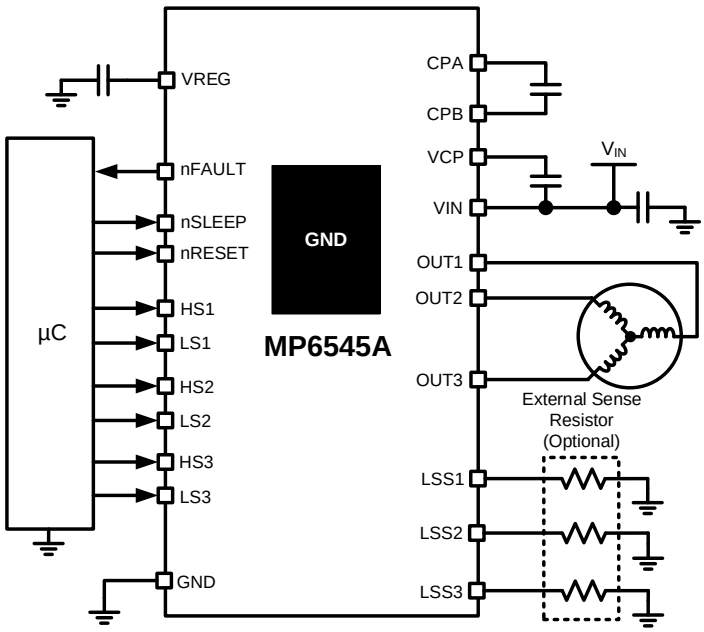
FEATURES

- 4.5V to 45V Operating Input Voltage (V_{IN}) Range
- 2.5A Maximum Output Current (I_{OUT_MAX})
- Three-Channel Half-Bridge (HB) Driver
- Low 150mΩ On Resistance ($R_{DS(ON)}$) per MOSFET
- Protection Functions Include:
  - Over-Current Protection (OCP)
  - Over-Voltage Protection (OVP)
  - Under-Voltage Lockout (UVLO)
  - Over-Temperature (OT) Shutdown
  - Fault Indication Output
- Available in QFN-28 (4mmx5mm) and TSSOP-28EP Packages

APPLICATIONS

- Brushless DC (BLDC) Motors
- Laser Printers and Copiers
- Textile Machines

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6545AGV	QFN-28 (4mmx5mm)	*See Below*	2
MP6545AGF	TSSOP-28EP	*See Below*	2a

* For Tape & Reel, add suffix -Z (e.g. MP6545AGV-Z).

* For Tape & Reel, add suffix -Z (e.g. MP6545AGF-Z).

TOP MARKING (MP6545AGV-Z)

MPSYWW
M6545A
LLLLLL

MPS: MPS prefix
Y: Year code
W: Week code
M6545A: Part number
LLLLLL: Lot number

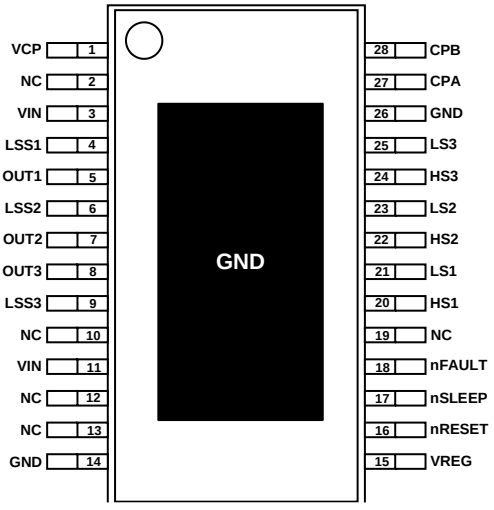
TOP MARKING (MP6545AGF-Z)

MPSYYWW
MP6545A
LLLLLLLLL

MPS: MPS prefix
Y: Year code
W: Week code
M6545A: Part number
LLLLLLLLL: Lot number

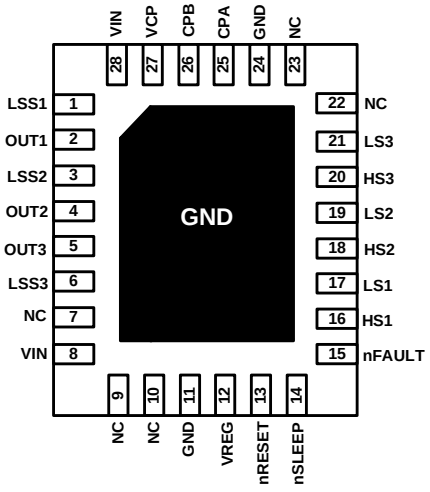
PACKAGE REFERENCE

TOP VIEW



MP6545AGF
TSSOP-28EP

TOP VIEW



MP6545AGV
QFN-28 (4mmx5mm)

PIN FUNCTIONS

Pin # (QFN)	Pin # (TSSOP)	Name	Description
8, 28	3, 11	VIN	**Input supply voltage.** Decouple the VIN pin to ground using a minimum 100nF ceramic capacitor. Additional bulk capacitance may be required.
1	4	LSS1	**Low-side (LS) source connection for phase 1.**
2	5	OUT1	**Phase 1 output terminal.**
3	6	LSS2	**LS source connection for phase 2.**
4	7	OUT2	**Phase 2 output terminal.**
5	8	OUT3	**Phase 3 output terminal.**
6	9	LSS3	**LS source connection for phase 3.**
11, 24	14, 26	GND	**Signal ground.**
12	15	VREG	**Internal regulator.** Connect a 1µF, 16V ceramic capacitor (X7R) to ground.
13	16	nRESET	**Reset input.** Pull the nRESET pin active low to reset the protection circuits and disable the outputs. This pin has an internal pull-down resistor.
14	17	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin logic low to enter low-power sleep mode. This pin has an internal pull-down resistor.
15	18	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. If used, nFAULT requires an external pull-up resistor. nFAULT is in logic low under fault conditions.
16	20	HS1	**High input to turn on the OUT1 high-side MOSFET (HS-FET).** The HS1 pin has an internal pull-down resistor.
17	21	LS1	**High input to turn on the OUT1 low-side MOSFET (LS-FET).** The LS1 pin has an internal pull-down resistor.
18	22	HS2	**High input to turn on the OUT2 HS-FET.** The HS2 pin has an internal pull-down resistor.
19	23	LS2	**High input to turn on the OUT2 LS-FET.** The LS2 pin has an internal pull-down resistor.
20	24	HS3	**High input to turn on the OUT3 HS-FET.** The HS3 pin has an internal pull-down resistor.
21	25	LS3	**High input to turn on the OUT3 LS-FET.** The LS3 pin has an internal pull-down resistor.
25	27	CPA	**Charge pump capacitor.** Connect a 100nF ceramic capacitor that is rated for V_{IN} between the CPA and CPB pins.
26	28	CPB	
27	1	VCP	**Charge pump output.** The VCP pin requires a 1µF, 16V ceramic capacitor connected to VIN.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +48V
OUTx voltage (V_{OUT1}, V_{OUT2}, V_{OUT3}) .....
……-0.7V to +48V
VCP, CPB .....V_{IN} to V_{IN} + 6.5V
LSSx to GND .....-0.3V to +0.3V
All other pins to GND .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN.....……3.125W
TSSOP.....……...3.9W
Storage temperature ..... -55°C to +150°C
Junction temperature .....150°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM).....±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5V to 45V
LSSx to GND .....-0.2V to +0.2V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-28 (4mmx5mm).....40.....9....°C/W
TSSOP-28EP.....32.....6...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, a 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.5		45	V
Quiescent current	I_{INQ}	nSLEEP = 1, with no load		2.8		mA
	$I_{INSLEEP}$	nSLEEP = 0		0.9	10	µA
Internal MOSFETs						
Output on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 1A, T_J = 25°C		135	170	mΩ
	$R_{DS(ON)\_LS}$	I_{OUT} = 1A, T_J = 25°C		150	185	mΩ
Body diode forward voltage	V_F	I_{OUT} = 1A			1.1	V
Control Logic Inputs						
Logic-low input threshold	V_{IL}				0.8	V
Logic-high input threshold	V_{IH}		2			V
Logic input current	I_{IN_H}	V_{IN} = 5V	-100		+100	µA
	I_{IN_L}	V_{IN} = 0V	-20		+20	µA
Internal pull-down resistance	R_{PD}	To GND		100		kΩ
nFAULT Output						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 5V			1	µA
Protection Circuits						
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{UVLO}				4.5	V
V_{IN} UVLO hysteresis	ΔV_{UVLO}			300		mV
V_{IN} over-voltage protection (OVP) threshold	V_{OVP}		45		48	V
Over-current (OC) trip level	I_{OCP1}	Sinking	3	4.5		A
	I_{OCP2}	Sourcing	3	4.5		A
OC deglitch time	t_{OCP}			1		µs
Thermal shutdown	T_{TSD}			165		°C
Thermal shutdown hysteresis	ΔT_{TSD}			15		°C

TYPICAL TIMIMG CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

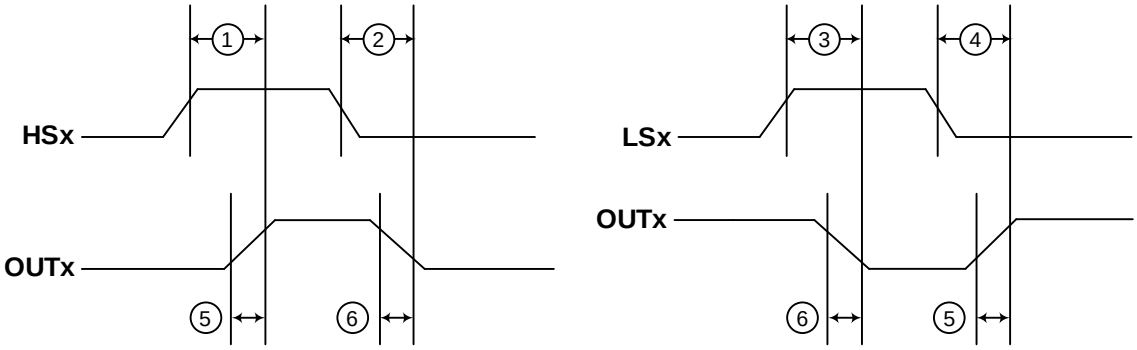


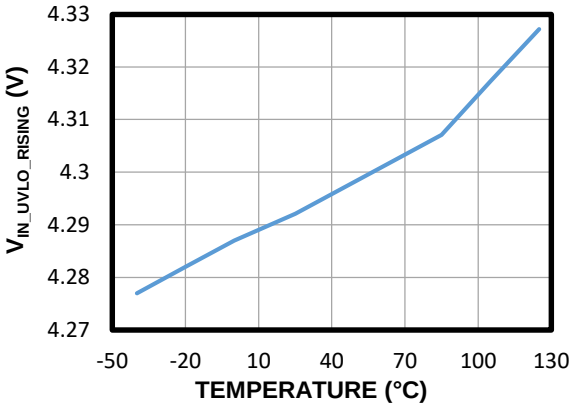
Figure 1: Timing Diagram

Table 1: Timing Characteristics

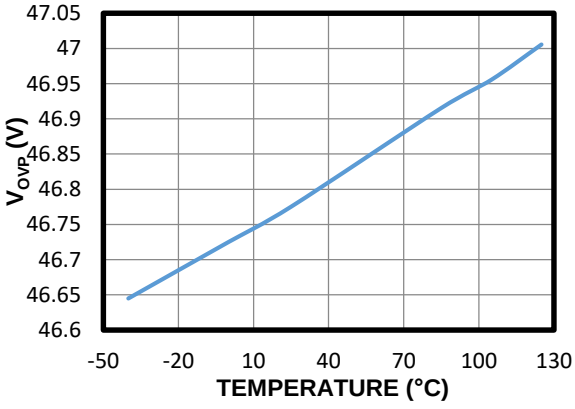
Parameter	Symbol	Condition	Min	Typ	Max	Units
HSx high to OUTx high delay time	t_1	10mA load connected from OUTx to GND	40		360	ns
HSx low to OUTx low delay time	t_2		40		360	ns
LSx high to OUTx low delay time	t_3	10mA load connected from OUTx to VIN	40		360	ns
LSx low to OUTx high delay time	t_4		40		360	ns
Output rise time	t_5		1		55	ns
Output fall time	t_6		1		165	ns
Dead time	-				80	ns

TYPICAL CHARACTERISTICS

V_{IN} UVLO Rising Threshold vs. Temperature

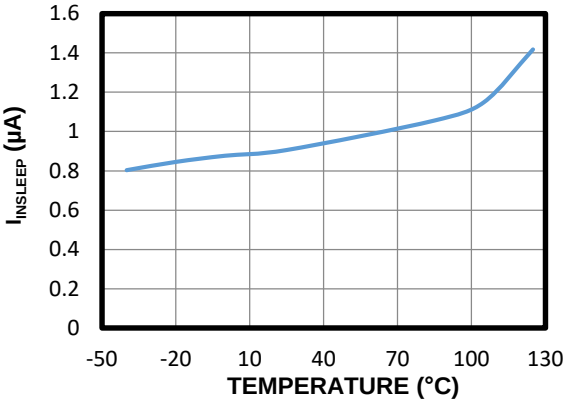


V_{IN} OVP Threshold vs. Temperature



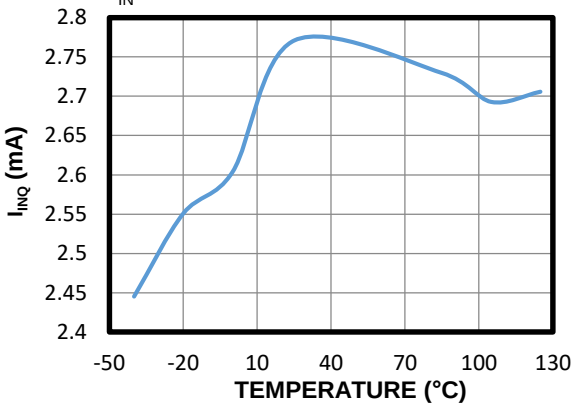
Quiescent Current ($I_{INSLEEP}$) vs. Temperature

V_{IN} = 24V



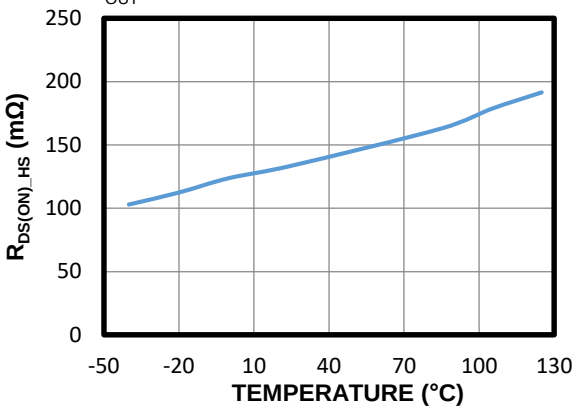
Quiescent Current (I_{INQ}) vs. Temperature

V_{IN} = 24V



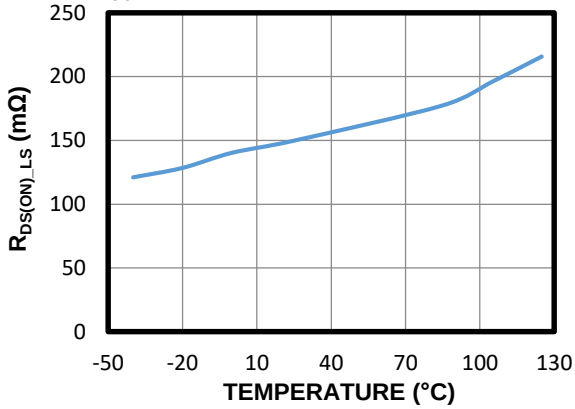
HS-FET On Resistance vs. Temperature

I_{OUT} = 1A



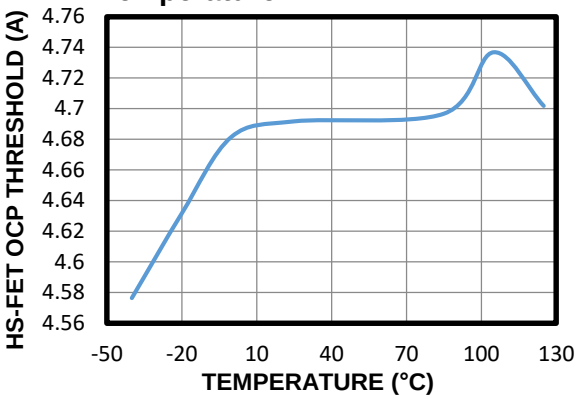
LS-FET On Resistance vs. Temperature

I_{OUT} = 1A

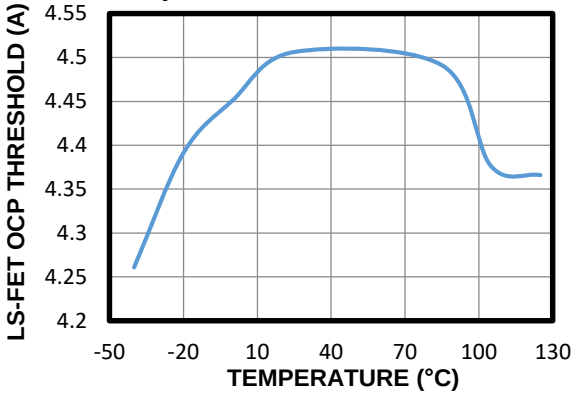


TYPICAL CHARACTERISTICS *(continued)*

HS-FET OCP Threshold vs. Temperature



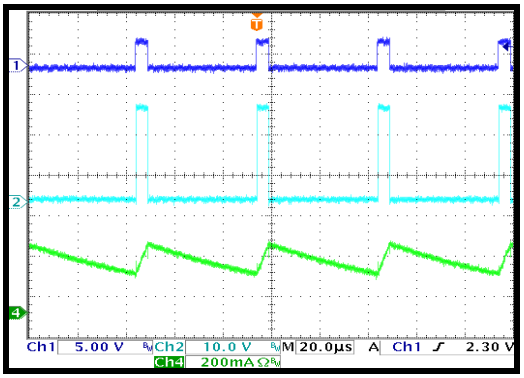
LS-FET OCP Threshold vs. Temperature



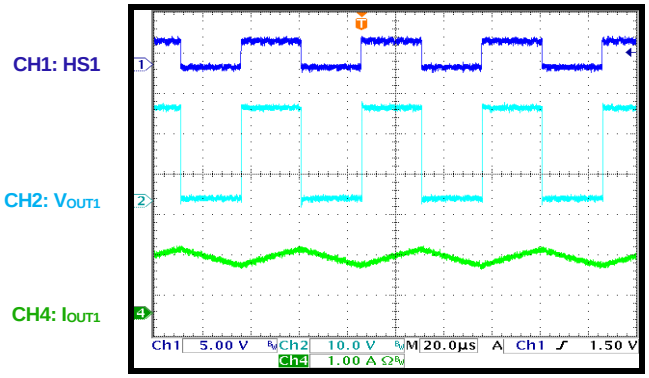
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, phase 1: switching with 20kHz frequency, phase 2: LS-FET on, phase 3: disabled, T_A = 25°C, resistor + inductor load: 4Ω + 0.34mH per phase with star connection.

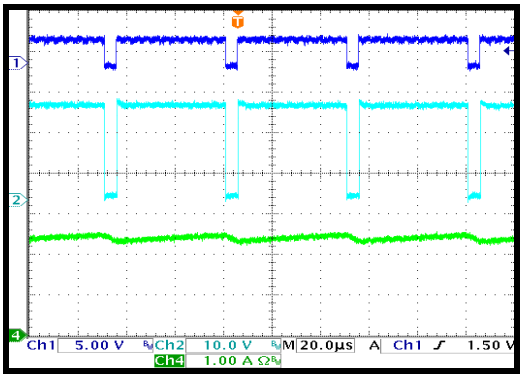
Steady State
Duty = 10%



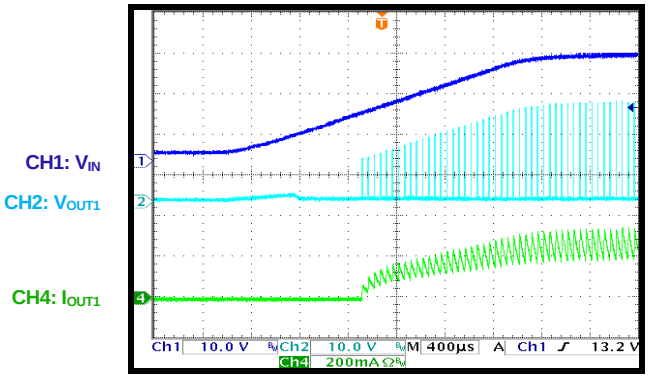
Steady State
Duty = 50%



Steady State
Duty = 90%



Power Ramping Up
Duty = 10%



Power Ramping Up
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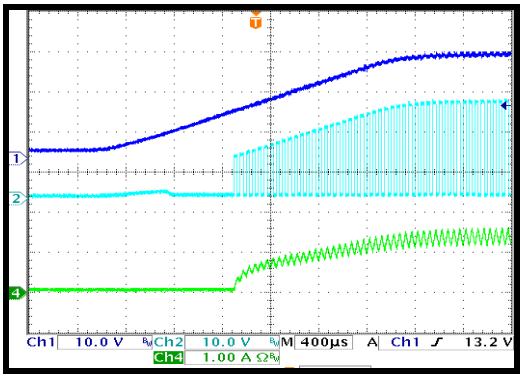
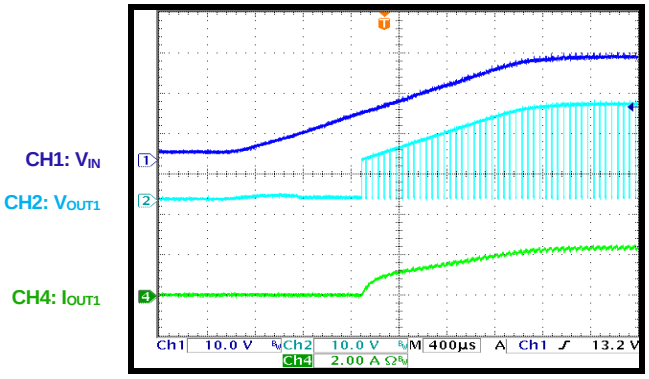


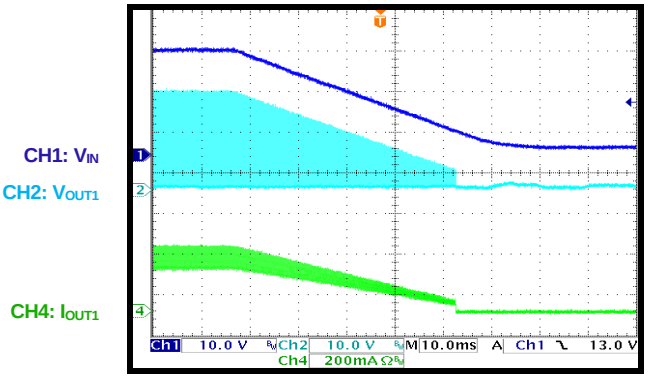
Power Ramping Up
Duty = 90%



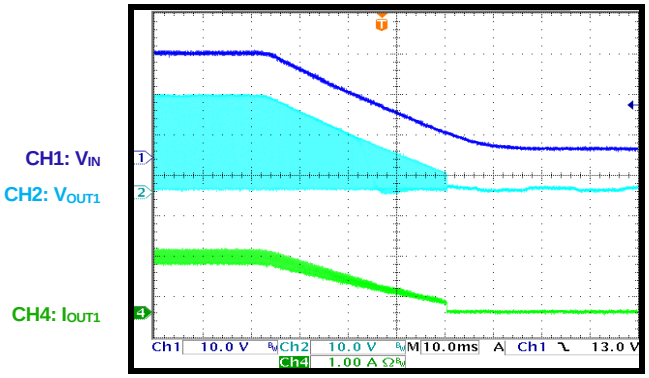
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, phase 1: switching with 20kHz frequency, phase 2: LS-FET on, phase 3: disabled, T_A = 25°C, resistor + inductor load: 4Ω + 0.34mH per phase with star connection.

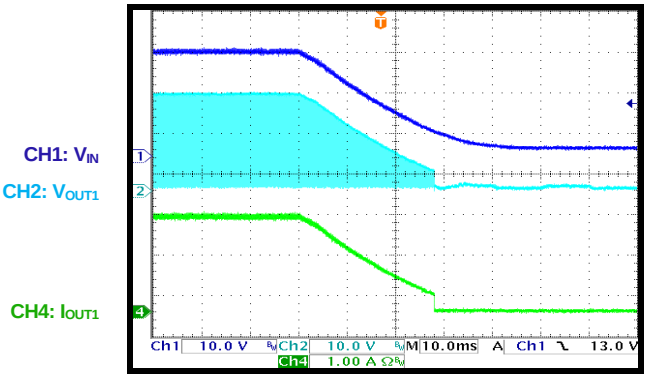
Power Ramping Down
Duty = 10%



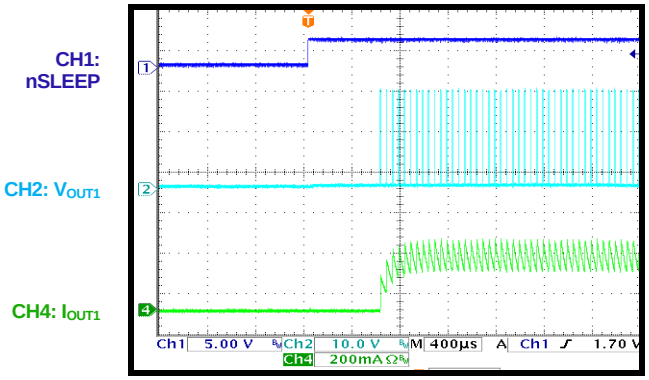
Power Ramping Down
Duty = 50%



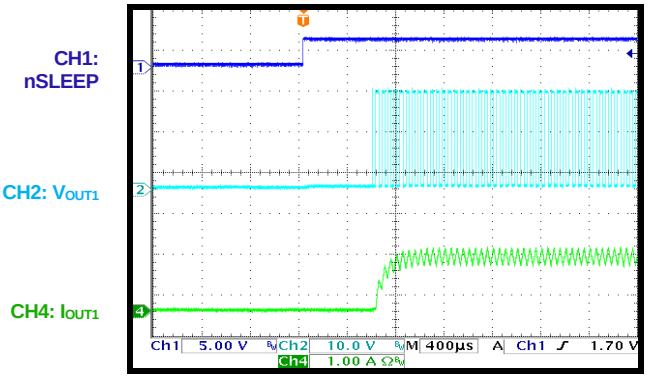
Power Ramping Down
Duty = 90%



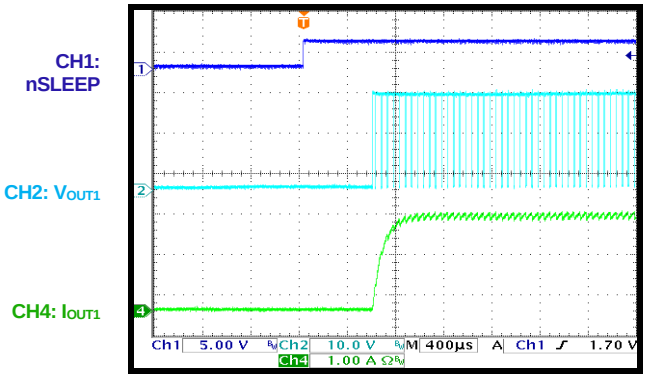
Sleep Recovery
Duty = 10%



Sleep Recovery
Duty = 50%



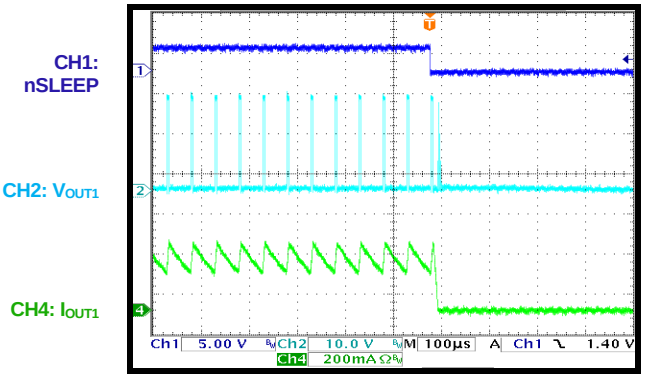
Sleep Recovery
Duty = 90%



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, phase 1: switching with 20kHz frequency, phase 2: LS-FET on, phase 3: disabled, T_A = 25°C, resistor + inductor load: 4Ω + 0.34mH per phase with star connection.

Sleep Entry
Duty = 10%



Sleep Entry
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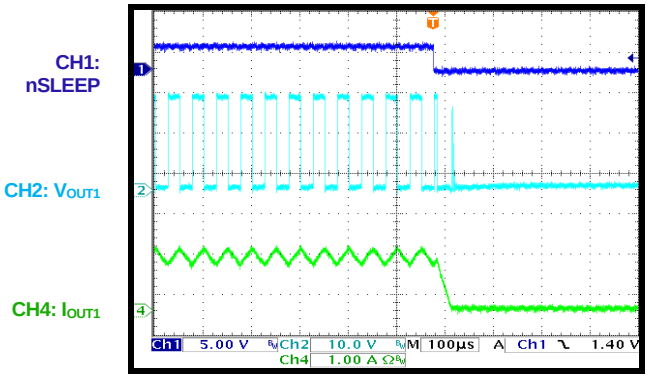
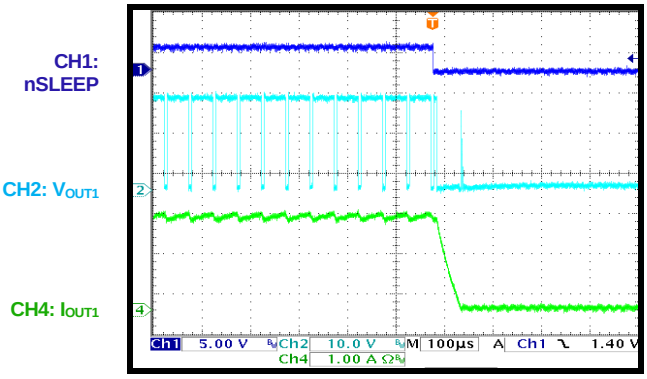
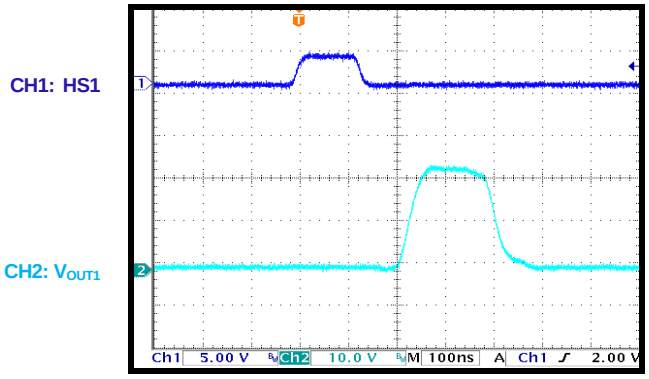


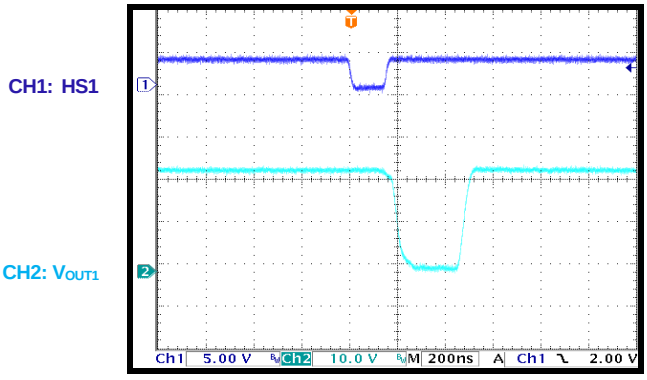
Sleep Entry
Duty = 90%



HS-FET Minimum On Time
No load



LS-FET Minimum On Time
No load



FUNCTIONAL BLOCK DIAGRAM

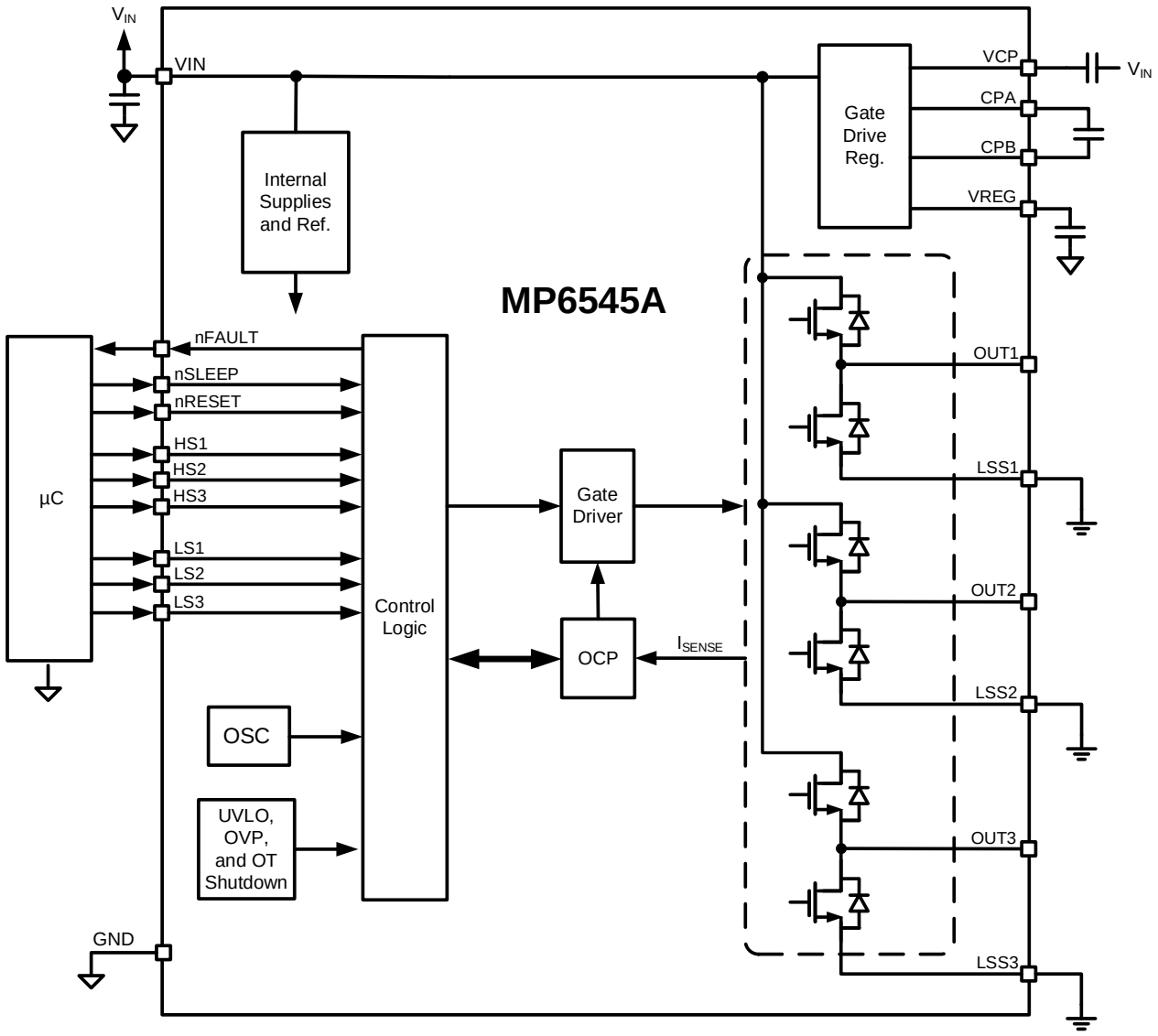


Figure 2: Functional Block Diagram

OPERATION

The MP6545A is a three-phase power stage designed to drive brushless DC (BLDC) motors or other loads. It integrates six N-channel power MOSFETs connected as three half H-bridges, with a 2.5A current capability. The device operates across a wide 4.5V to 45V supply input voltage (V_{IN}) range.

nSLEEP and nRESET

Pull the nSLEEP pin low to force the MP6545A to enter low-power sleep mode. In this mode, the gate driver charge pump stops, and all the internal circuits and outputs are disabled. All inputs are ignored when nSLEEP is active low.

When the MP6545A exits sleep mode, 600µs must pass before driving the motor. This allows the internal circuitry to stabilize. nSLEEP has an internal pull-down resistor.

Pull the nRESET pin low to reset the latched protection features, including over-current protection (OCP) and over-voltage protection (OVP), as well as to disable the outputs to a high-impedance (Hi-Z) state.

Input Interface

The MP6545A contains three half-bridges that operate independently. The device has high-side (HS) and low-side (LS) inputs for each of the output pins. Table 2 shows the HSx and LSx input logic.

Table 2: HSx and LSx Input Logic

HSx	LSx	OUTx
0	0	Hi-Z
0	1	L
1	0	H
1	1	Hi-Z

Note that all logic inputs have weak, internal pull-down resistors.

Automatic Synchronous Rectification

If the output high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) are turned off, then the recirculation current must continue to flow when driving current through an inductive load. This current is typically passed through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6545A implements automatic synchronous rectification.

If both the HS-FET and LS-FET are turned off and the voltage on an OUTx pin (V_{OUTx}) is pulled below ground, then the LS-FET turns on until the current flowing through it approaches 0A, or until the HS-FET is commanded to turn on. Similarly, if V_{OUTx} exceeds V_{IN}, then the HS-FET turns on until the current approaches 0A, or until the LS-FET turns on.

Internal Supply Voltages (V_{REG} and V_{CP})

The internal regulators generate a 5V supply voltage (V_{REG}) for the LS gate drive, and a supply exceeding V_{IN} by 5V (V_{CP}) for the HS gate drive. These supplies require external capacitors.

The VREG pin requires a 1µF ceramic capacitor to ground. Meanwhile, the VCP pin requires a 1µF ceramic capacitor to VIN. Both capacitors should be X7R ceramic capacitors, and rated for at least 16V.

Connect the charge pump flying capacitor between the CPA and CPB pins using a 100nF ceramic capacitor (X7R) that is rated for at least the maximum V_{IN}.

nFAULT

The MP6545A provides an nFAULT pin to report to the system if a fault condition such as OCP, OVP, or over-temperature protection (OTP) occurs. nFAULT is an open-drain output, and is pulled low during fault conditions. If used, nFAULT should be pulled high via an external pull-up resistor.

Over-Current Protection (OCP)

OCP circuitry limits the current through the HS-FET and LS-FET by disabling the gate driver. If the over-current (OC) limit threshold is reached and lasts for longer than the OC deglitch time (t_{OCP}), then all the MOSFETs in the H-bridge are disabled and nFAULT is pulled low. The driver remains disabled until the device is reset by pulling nRESET low, or cycling the power on the MP6545A.

OC conditions on the HS and LS devices (i.e. an OC condition to ground, supply, or across a motor winding) all result in an OC shutdown.

Over-Voltage Protection (OVP)

If V_{IN} exceeds the OVP threshold (V_{OVP}), then the outputs are disabled and nFAULT is pulled low. The driver remains disabled until the device is reset by pulling nRESET low, or cycling the power on the MP6545A.

Input Under-Voltage Lockout (UVLO) Protection

If V_{IN} falls below the under-voltage lockout (UVLO) threshold (V_{UVLO}), then all circuitry in the device is disabled and the internal logic resets. Once V_{IN} exceeds V_{IN_UVLO}, the device starts up again and resumes normal operation.

Thermal Shutdown

If the die temperature exceeds safe limits, then all the MOSFETs in the H-bridge are disabled and nFAULT is pulled low. Once the die temperature returns to a safe level, the MP6545A automatically starts up again and resumes normal operation.

APPLICATION INFORMATION

Selecting the External Components

Bypass the two VIN pins to GND using a minimum 100nF ceramic capacitor with X7R dielectrics, placed as close to the IC as possible. Place an additional 1µF to 10µF ceramic capacitor close to the 100nF capacitor. Depending on the supply impedance and distance to other large capacitors, an electrolytic bulk capacitor may also be required to stabilize VIN.

Connect a 100nF ceramic capacitor rated for V_{IN} between the CPA and CPB pins. Connect a 1µF, 16V ceramic capacitor between the VIN and VCP pins.

Connect a 1µF, 16V ceramic capacitor with X7R dielectrics from the VREG pin to GND.

PCB Layout Guidelines

Efficient PCB layout is critical to achieve stable operation. For the best results, refer to Figure 3 and Figure 4, and follow the guidelines below:

1. Place the supply bypass and charge pump capacitors as close to the IC as possible, ideally adjacent to the pins on the same PCB layer.
2. Each VIN pin requires a bypass capacitor.
3. Place as much copper on the long pads as possible.
4. Place large copper areas on the pads and the device's outer copper layer.
5. The thermal pad should be soldered directly to the copper on the PCB.
6. Add thermal vias to transfer heat to the other PCB layers.

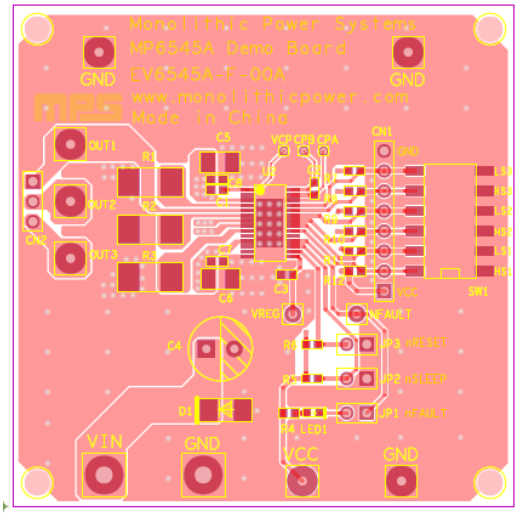


Figure 3: Recommended PCB Layout (MP6545AGF)

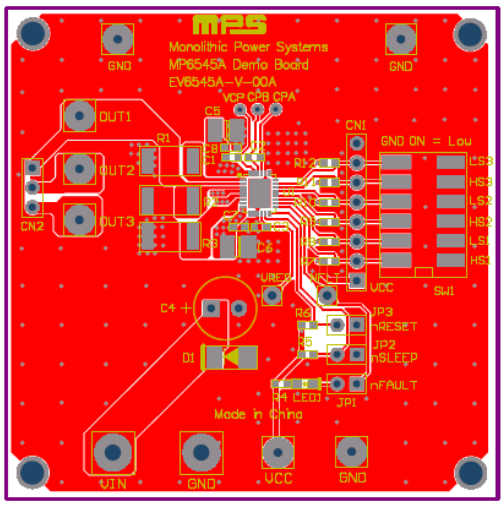


Figure 4: Recommended PCB Layout (MP6545AGV)

TYPICAL APPLICATION CIRCUIT

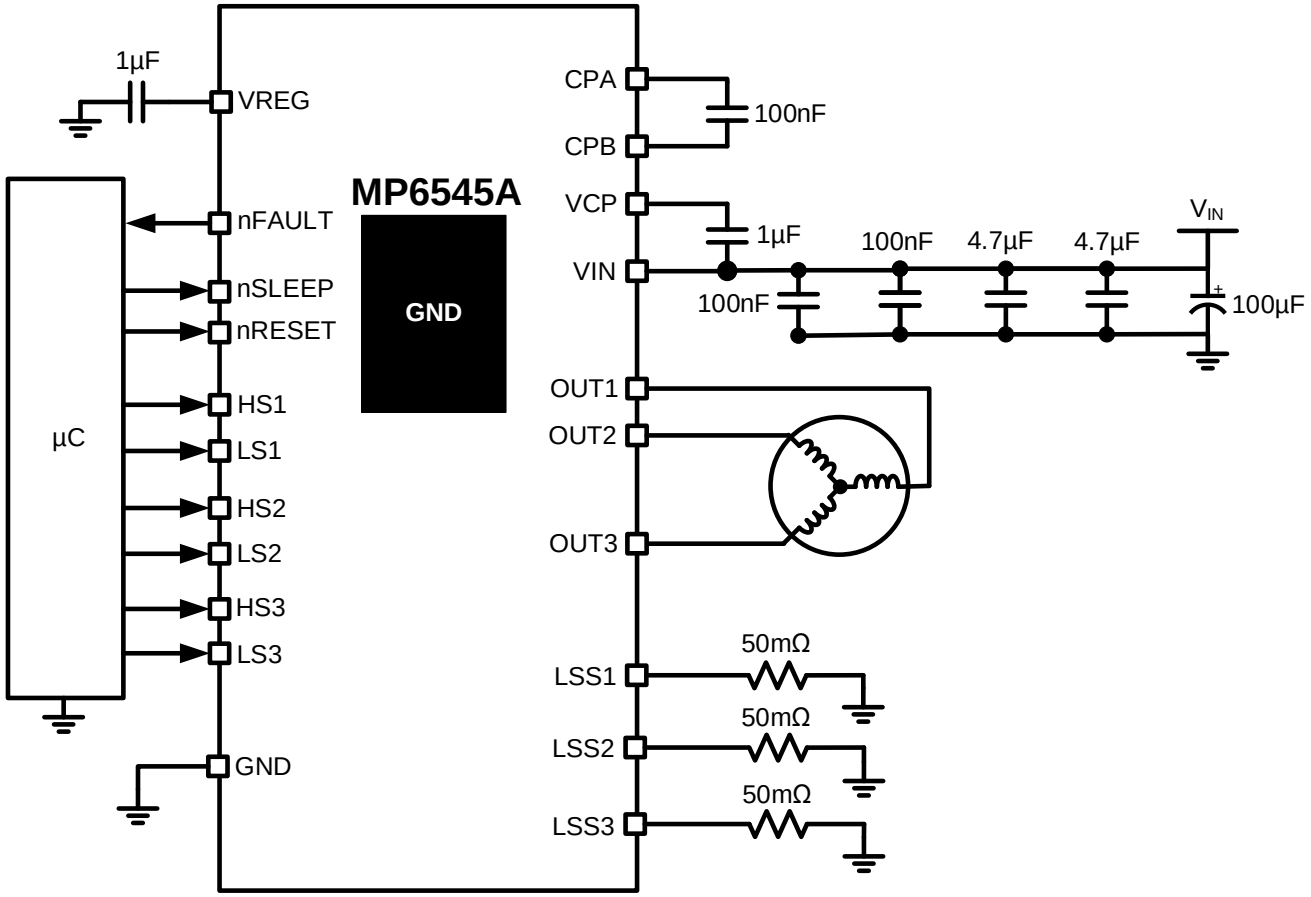
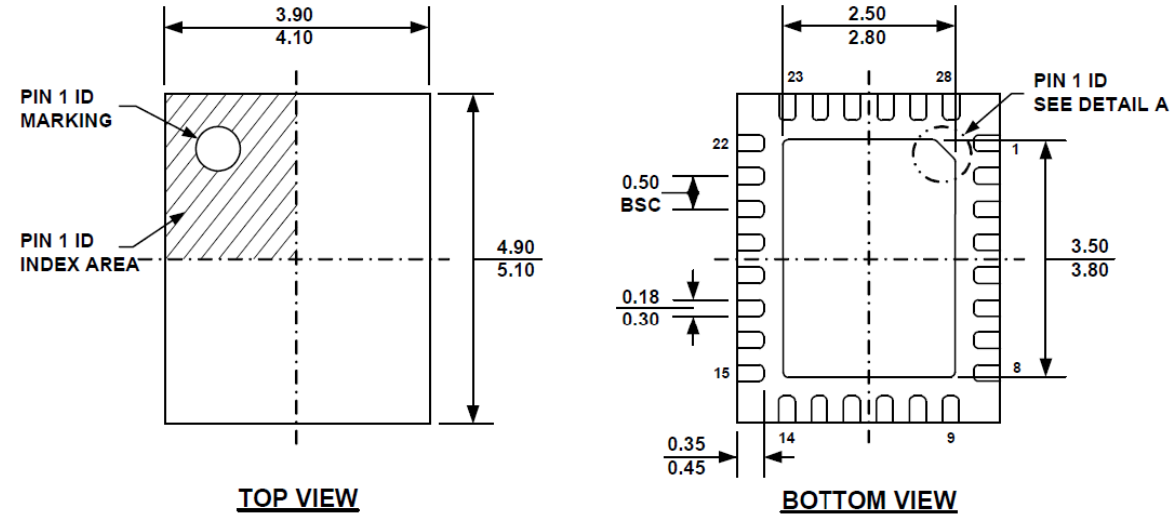


Figure 5: Typical Application Circuit

PACKAGE INFORMATION

QFN-28 (4mmx5mm)

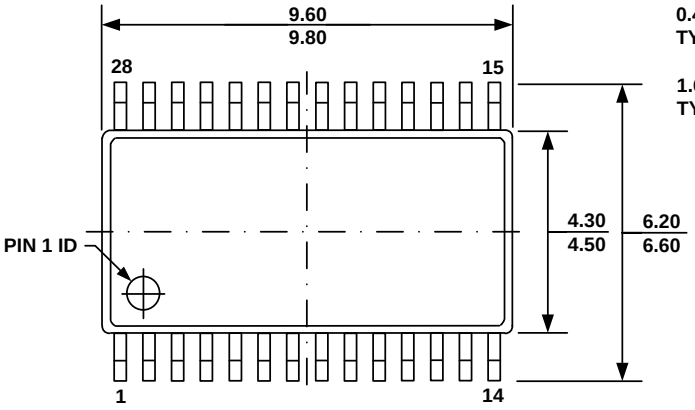


NOTE:

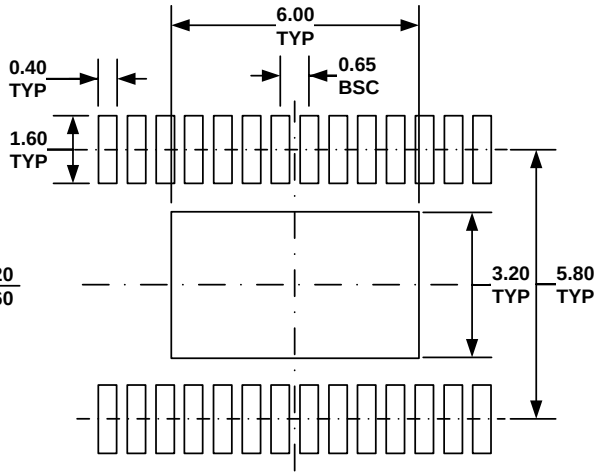
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VHGD-3.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

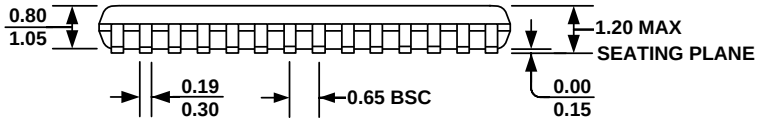
TSSOP-28EP



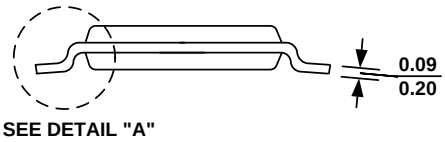
TOP VIEW



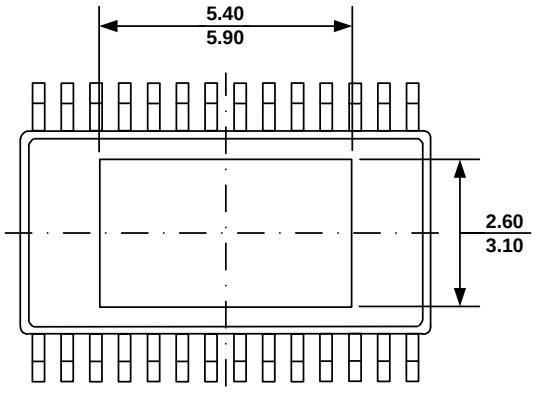
RECOMMENDED LAND PATTERN



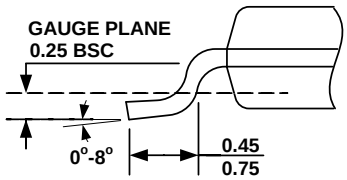
FRONT VIEW



SIDE VIEW



BOTTOM VIEW

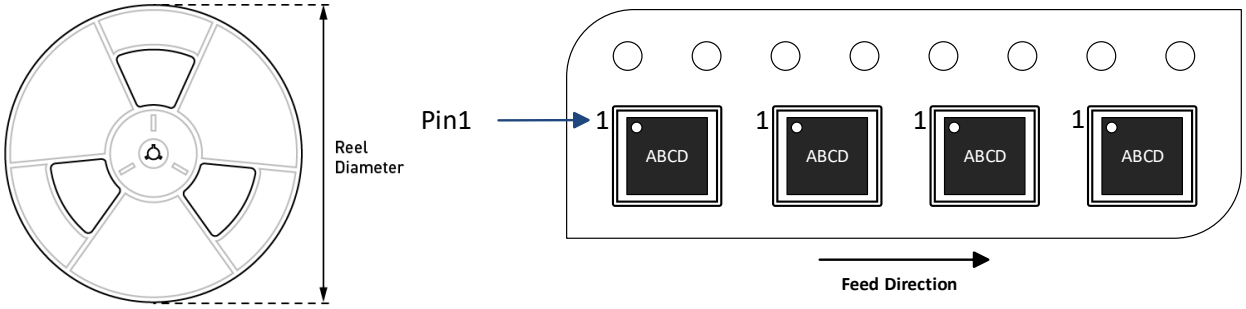


DETAIL “A”

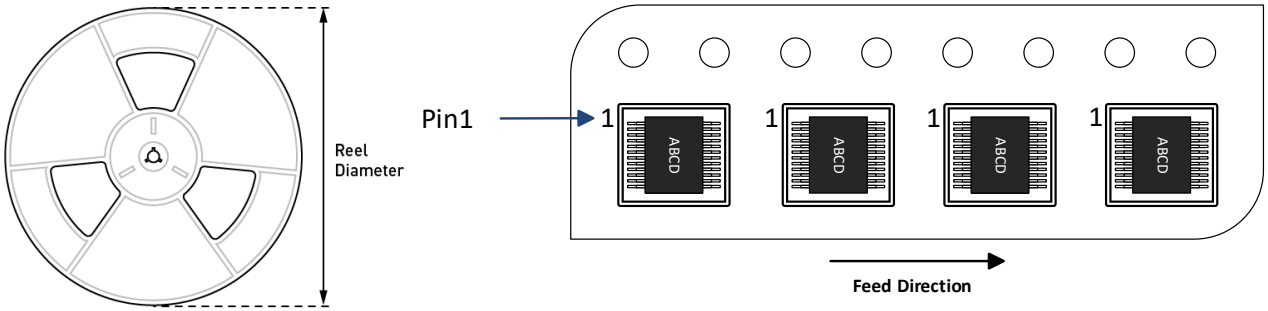
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6545AGV-Z	QFN-28 (4mmx5mm)	5000	N/A	13in	12mm	8mm



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6545AGF-Z	TSSOP-28EP	2500	N/A	13in	16mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/14/2022	Initial Release	-
1.1	5/12/2023	Updated the MSL rating for the MP6545AGV to “2” in the Ordering Information section	2