MP6605D

4-Channel, Parallel-Interface Low-Side MOSFET Driver IC

DESCRIPTION

The MP6605D is a 4-channel low-side MOSFET (LS-FET) driver IC that integrates four LS-FETs and high-side (HS) clamp diodes to drive inductive loads. It is well-suited for unipolar stepper motor and solenoid driver applications.

The device can achieve up to 1.5A of output current (I_{OUT}) across a wide 4.5V to 60V input voltage (V_{IN}) range. The maximum voltage of the motor driver output pins is 60V.

Full protection features include over-current protection (OCP), under-voltage lockout (UVLO) protection, and thermal shutdown.

The MP6605D is available in a QFN-24 (4mmx4mm) package.

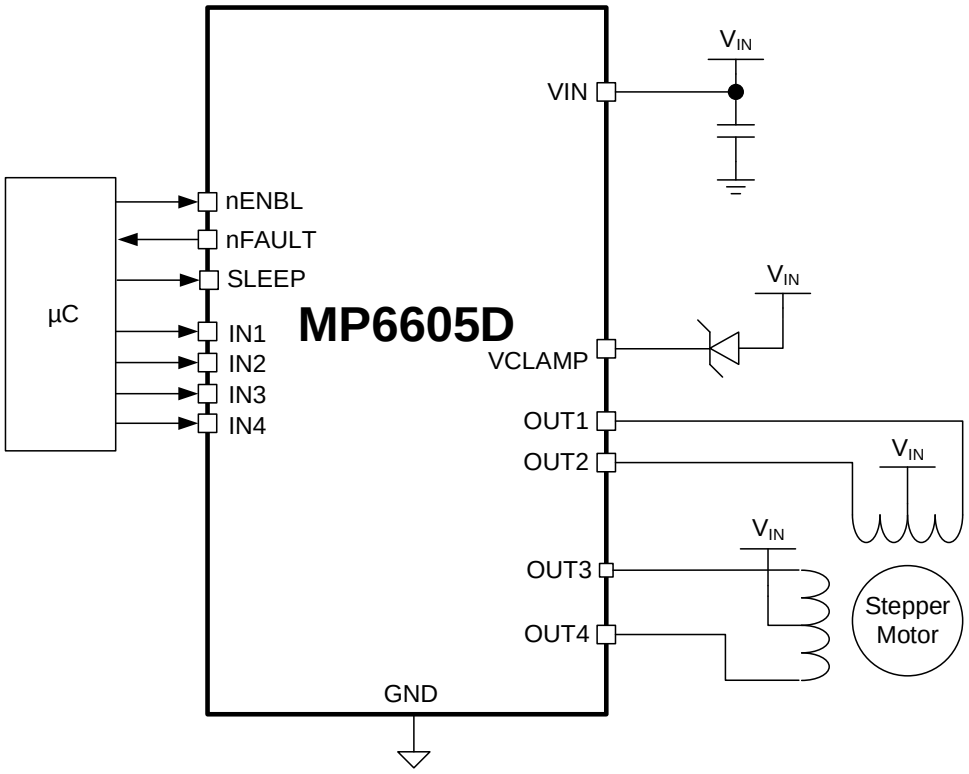
FEATURES

- Wide 4.5V to 60V Input Voltage (V_{IN}) Range
- 60V Maximum Winding Clamp Voltage (V_{CLAMP})
- Four Low-Side MOSFETs (LS-FETs) and Four High-Side (HS) Clamp Diodes
- 350mΩ MOSFET On Resistance
- 1.5A Maximum Output Current (I_{OUT}) while One LS-FET Is On or 700mA Maximum I_{OUT} while Four LS-FETs Are On
- Over-Current Protection (OCP)
- Under-Voltage Lockout (UVLO) Protection
- Thermal Shutdown
- Fault Indication Output
- Control Power Supply Not Required
- Simple Logic Interface
- 3.3V and 5V Compatible Logic Supply
- Available in a QFN-24 (4mmx4mm) Package

APPLICATIONS

- Unipolar Stepper Motors
- Solenoid Drivers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6605DGR*	QFN-24 (4mmx4mm)	*See Below*	1

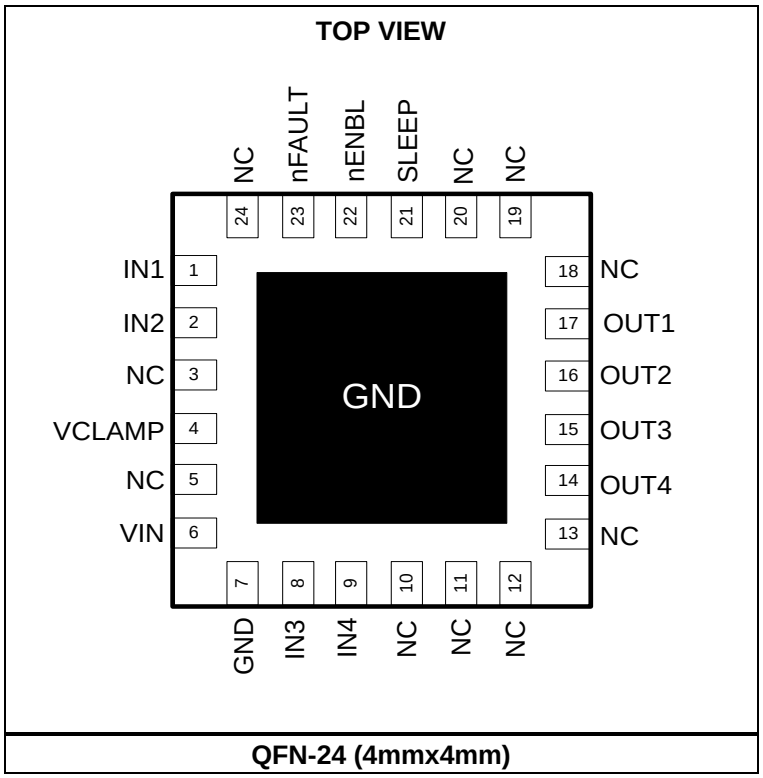
* For Tape & Reel, add suffix -Z (e.g. MP6605DGR-Z)

TOP MARKING

MPSYWW
M6605D
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M6605D: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
6	VIN	**Input supply voltage.** Decouple the VIN pin using a 100nF ceramic decoupling capacitor connected to ground. Additional bulk capacitance may be required.
7, EP	GND	**Power ground.**
4	VCLAMP	**High-side MOSFET clamp.** Connect the VCLAMP and VIN pins via a TVS or Zener diode to clamp the leakage inductance spike. See the Leakage Inductance Clamp (VCLAMP) section on page 9.
1	IN1	**Control input 1.** Pull the IN1 pin high to drive the corresponding output (OUT1) low. If IN1 is low, then OUT1 is in a high-impedance (Hi-Z) state. IN1 has an internal pull-down resistor.
2	IN2	**Control input 2.** Pull the IN2 pin high to drive the corresponding output (OUT2) low. If IN2 is low, then OUT2 is in a high-impedance (Hi-Z) state. IN2 has an internal pull-down resistor.
8	IN3	**Control input 3.** Pull the IN3 pin high to drive the corresponding output (OUT3) low. If IN3 is low, then OUT3 is in a high-impedance (Hi-Z) state. IN3 has an internal pull-down resistor.
9	IN4	**Control input 4.** Pull the IN4 pin high to drive the corresponding output (OUT4) low. If IN4 is low, then OUT4 is in a high-impedance (Hi-Z) state. IN4 has an internal pull-down resistor.
22	nENBL	**Enable input.** Pull the nENBL pin high to disable the outputs. Pull nENBL low to enable the outputs. nENBL has an internal pull-down resistor.
21	SLEEP	**Sleep mode input.** Pull the SLEEP pin high to enter low-power sleep mode. Pull SLEEP low or connect SLEEP to ground for normal operation. SLEEP has an internal pull-down resistor.
23	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. nFAULT requires an external pull-up resistor if used. If a fault occurs, nFAULT is pulled low.
17	OUT1	**Output terminal 1.**
16	OUT2	**Output terminal 2.**
15	OUT3	**Output terminal 3.**
14	OUT4	**Output terminal 4.**

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +65V
OUTx voltage (V_{OUTx}) .....-0.7V to +65V
VCLAMP voltage (V_{CLAMP}).....-0.7V to +65V
All other pins to GND .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
..... 2.9W
Storage temperature..... -55°C to +150°C
Junction temperature ..... +150°C
Lead temperature (solder) ..... +260°C

ESD Ratings

Human body model (HBM) …….. ±2kV
Charged device model (CDM) …… ±2kV

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....4.5V to 60V
Output voltage (V_{OUTx})..... 0 to 60V
Maximum LS-FET current (I_{LSx}) 1.5A
Maximum HS-FET diode current (I_{HSx}) at <20% duty cycle…….…….…… 1.5A
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-24 (4mmx4mm)……42.....9....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

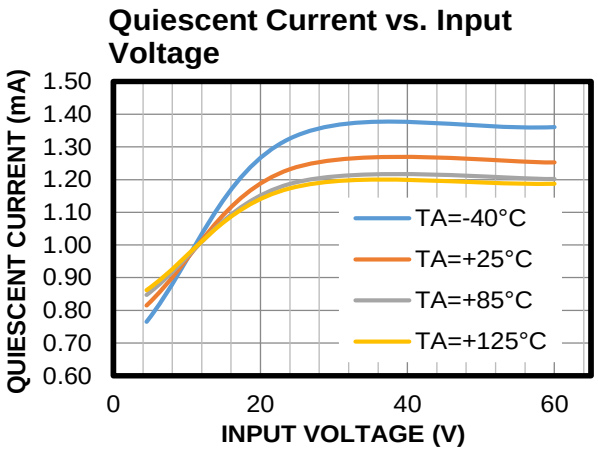
V_{IN} = 12V, V_{CLAMP} = 36V, T_A = 25°C, unless otherwise noted.

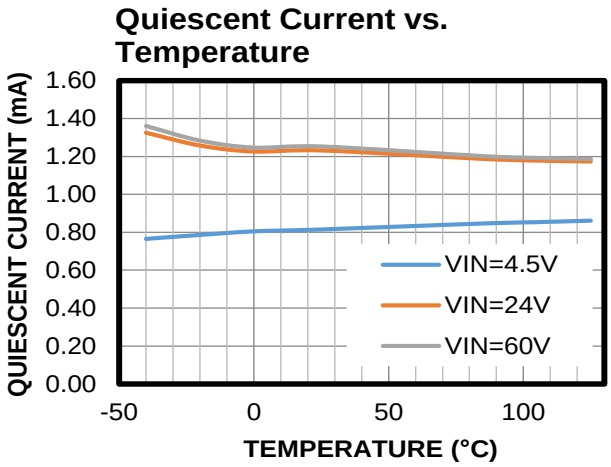
Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.5	12 or 24	60	V
Clamp voltage	V_{CLAMP}		V_{IN}		60	V
Quiescent current	I_Q	V_{IN} = 24V, V_{nENBL} = 0V, V_{SLEEP} = 0V, no load		1.2	5	mA
SLEEP current	I_{SLEEP}	V_{IN} = 24V, V_{SLEEP} = 1		2	5	µA
Internal MOSFETs						
On resistance	$R_{DS(ON)}$	V_{IN} = 24V, I_{OUT} = 700mA, T_J = 25°C		350	500	mΩ
		V_{IN} = 24V, I_{OUT} = 700mA, T_J = 85°C			800	mΩ
High-side (HS) diode forward voltage	V_{FWD_HS}	I_{OUT} = 700mA			1.1	V
Low-side MOSFET (LS-FET) body diode forward voltage	V_{FWD_LS}	I_{OUT} = 700mA			1.1	V
Control Logic						
Input logic low threshold	V_{IN_LOW}				0.7	V
Input logic high threshold	V_{IN_HIGH}		2.3			V
Input logic hysteresis	$V_{IN\_HIGH\_HYS}$			560		mV
Input logic high current	I_{IN_HIGH}	V_{IN_HIGH} = 5V			20	µA
Input logic low current	I_{IN_LOW}	V_{IN_LOW} = 0.8V			5	µA
nFAULT Output (Open-Drain Outputs)						
Output low voltage	V_{OUT_LOW}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{LKG_HIGH}	V_{OUT} = 3.3V			1	µA
Protections						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$			3.4	4.5	V
Over-current protection (OCP) threshold	I_{OCP}		1.5	4		A
OCP deglitch time	t_{OCP}			3.5		µs
OCP retry time	t_{OCR}			2.5		ms
Thermal shutdown (5)	T_{SD}			155		°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}			25		°C
Output enable (EN) time (5)	t_{EN}			3.3		µs

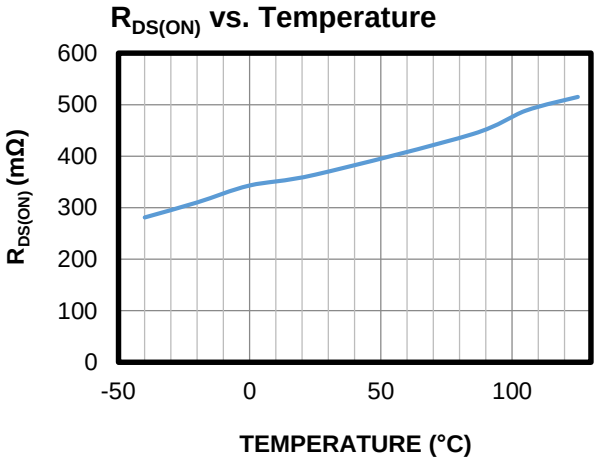
Note:

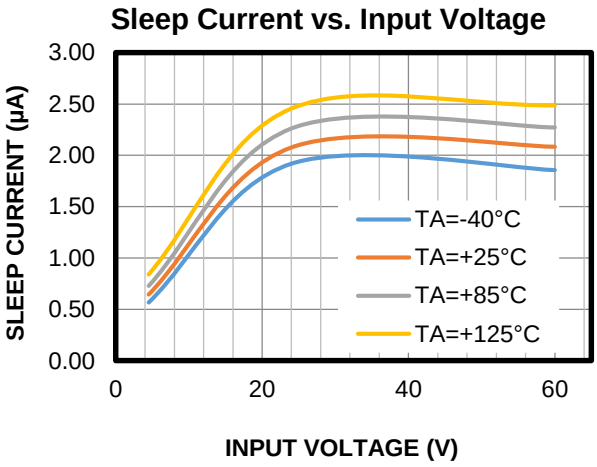
5) Guaranteed by design.

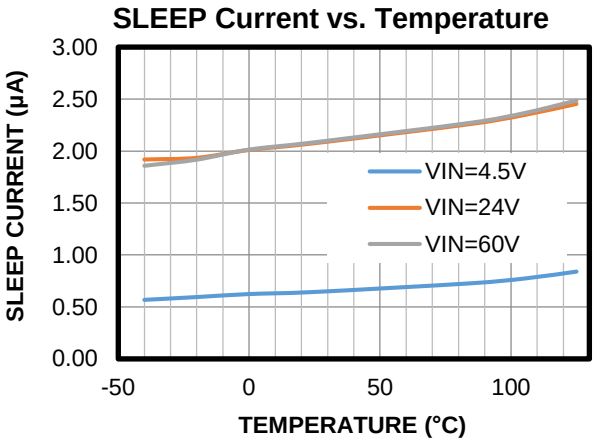
TYPICAL CHARACTERISTICS









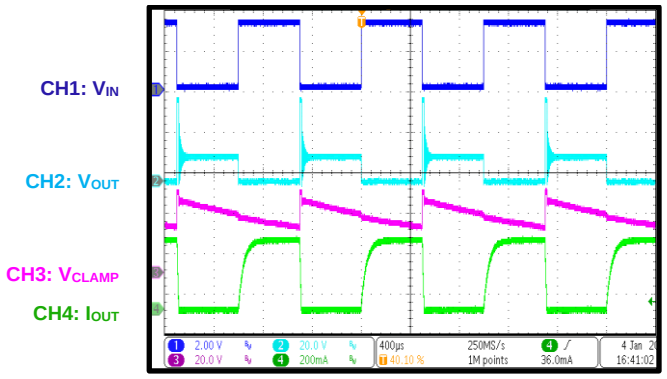


TYPICAL PERFORMANCE CHARACTERISTICS

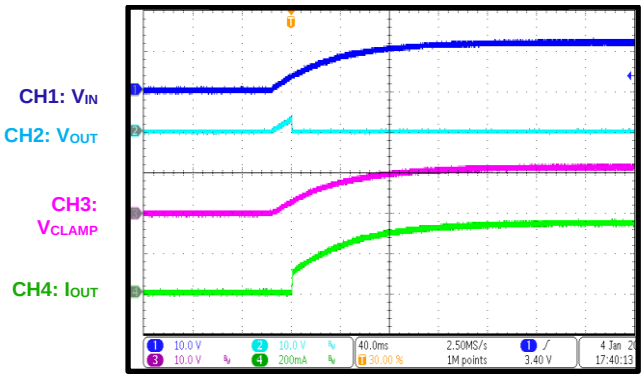
V_{IN} = 12V, VCLAMP connected to VIN with 24V TVS diode, I_{OUT} = 700mA, T_A = 25°C, output load = resistance (33Ω) + inductance (1.5mH), unless otherwise noted.

Normal Operation

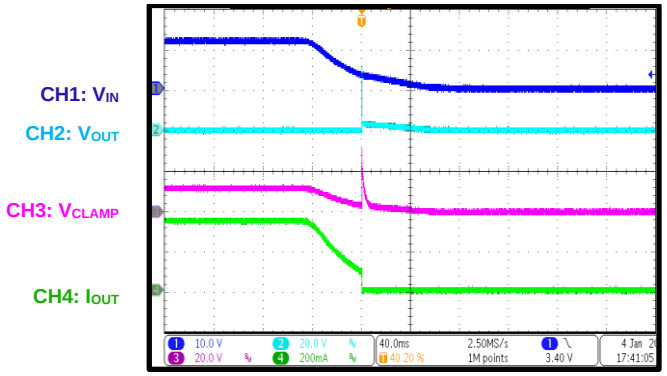
f_{SW} = 1kHz



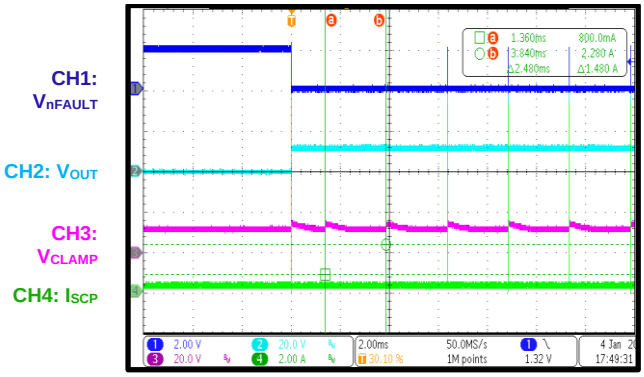
Start-Up through VIN



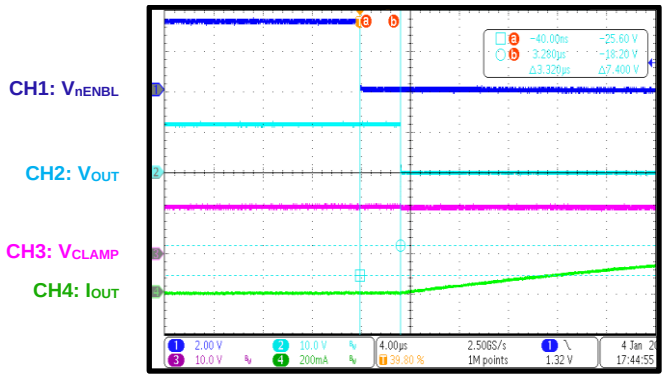
Shutdown through VIN



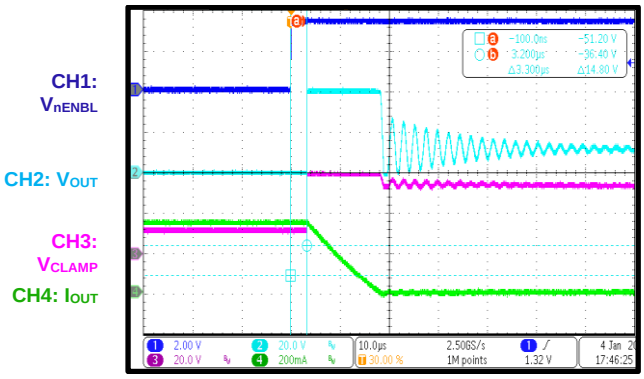
Short-Circuit Protection



IC Enable



IC Disable



FUNCTIONAL BLOCK DIAGRAM

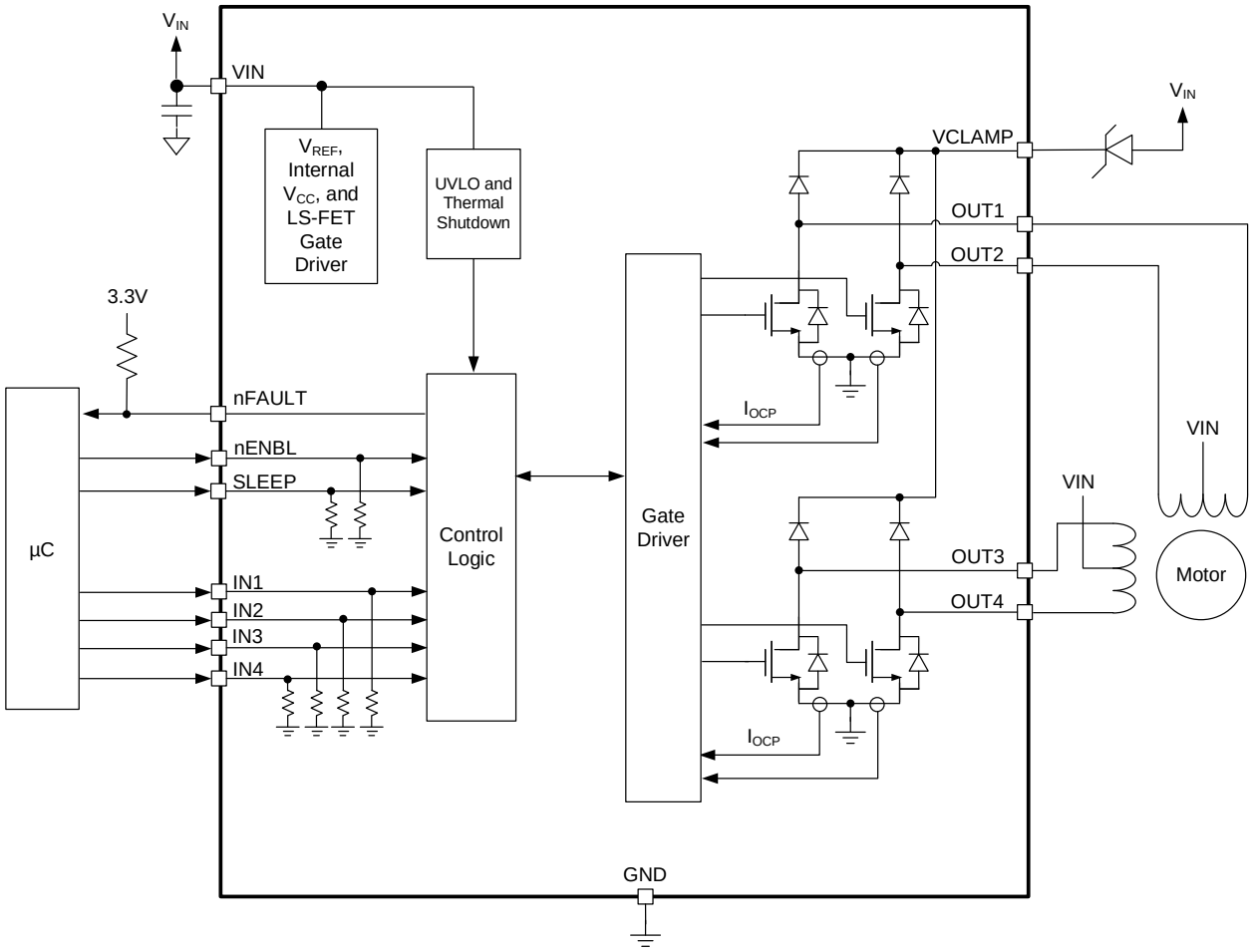


Figure 1: Functional Block Diagram

OPERATION

The MP6605D is a 4-channel low-side MOSFET driver that integrates four N-channel power MOSFETs (LS-FETs) and four clamp diodes with 1.5A of current capability per channel. It operates across a wide 4.5V to 60V input voltage (V_{IN}) range.

The MP6605D is designed to drive inductive loads, such as unipolar stepper motors and solenoids.

Unipolar Stepper Motor Operation

Unipolar stepper motors have two windings that are driven by 90° out-of-phase currents. Each winding has a center tap, which is connected to the power source. Current flows through the winding in a push-pull fashion, alternately pulling one side of the winding to ground, and then the other. This reverses the current, as well as the magnetic field.

If a MOSFET is turned off via the winding's inductance, then the current continues to flow through the opposite side of the winding. This current flows from ground via the opposite MOSFET's body diode to the power supply.

Leakage Inductance Clamp (VCLAMP)

A unipolar stepper motor has a leakage inductance due the two halves of the winding not being coupled perfectly. If a MOSFET turns off, then the voltage exceeds 2 x V_{IN} for a short period of time. This leakage inductance spike should be clamped to prevent damage to the IC from an over-voltage (OV) condition on the MOSFETs.

If a MOSFET turns off while driving a solenoid connected to VIN, the current should continue to flow until the magnetic field decays. This current flows to the VCLAMP pin.

These currents flow through the internal diodes of each output to a common VCLAMP pin. This pin is typically connected to a transient voltage suppressor to limit the voltage on the output pins to 60V max, regardless of V_{IN}.

Connect the VCLAMP and VIN pins if VCLAMP is not used (if the outputs should not exceed V_{IN}).

SLEEP and nENBL Operation

Pull SLEEP high to have the device enter low-power sleep mode. In sleep mode, the gate driver charge pump turns off, and all of the internal circuits and outputs are disabled. All of the inputs are ignored while SLEEP is pulled high.

There is a delay time (1ms) between when the part exits sleep mode and when a serial interface command can be issued to allow the internal circuitry to stabilize. SLEEP has an internal pull-down resistor.

The nENBL pin controls the output drivers. Pull nENBL low to enable the outputs. Pull nENBL high to diable the outputs. nENBL has an internal pull-down resistor.

Fault Reporting

The MP6605D's nFAULT pin reports whether an over-current (OC), over-temperature (OT) , or OV fault occurs. nFAULT is an open-drain output that is pulled low if a fault occurs. Once the fault condition is removed, nFAULT is pulled high via an external pull-up resistor.

Over-Current Protection (OCP)

Over-current protection (OCP) circuitry disabled the gate driver to limit the current flowing through the MOSFETs. If the current exceeds OCP threshold for longer than the OCP deglitch time (t_{OCP}), then the MOSFET with the OC condition is disabled, and nFAULT is pulled low. All other outputs remain active. The driver turns on again after about 1.2ms.

V_{IN} Under-Voltage Lockout (UVLO) Protection

If V_{IN} drops below the under-voltage lockout (UVLO) threshold, then all of the IC's circuitry is disabled, and the internal logic is reset. Operation resumes once V_{IN} exceeds the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, the outputs are disabled, and nFAULT is driven low. Once the die temperature has fallen to a safe level, operation resumes automatically.

APPLICATION INFORMATION

External Component Selection

The MP6605D requires a 100nF ceramic bypass capacitor with X7R dielectrics connected at the VIN pin. It also requires a ≥4.7µF connected near VIN. An additional electrolytic capacitor is recommended if the IC is located away from other power supply capacitances.

The VCLAMP pin dissipates the energy in an inductive load while there is no current flowing through the device. Depending on the application, VCLAMP can be connected to VIN directly or via a TVS diode.

Connecting the VCLAMP and VIN pins is equivalent to connecting a diode between each output and VIN. Using a TVS diode allows the voltage on the output pins to exceed V_{IN} until the TVS diode breaks down. This increased voltage allows the current flowing through the load to decay faster. This is typically required for unipolar stepper motor high-speed operation.

The TVS diode's breakdown voltage should be chosen such that the VCLAMP voltage (V_{CLAMP}) remains below its maximum ratings.

Choose a 24V TVS diode for input voltages ≤24V to ensure that V_{CLAMP} remains within its operating limits.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the bypass capacitors near the IC.
2. Place the VCLAMP TVS diode near the IC if used.
3. Place multiple thermal vias under the exposed pad to improve thermal dissipation. This allows heat to move between the IC and a plane located on a middle-layer or on the back side of the PCB.

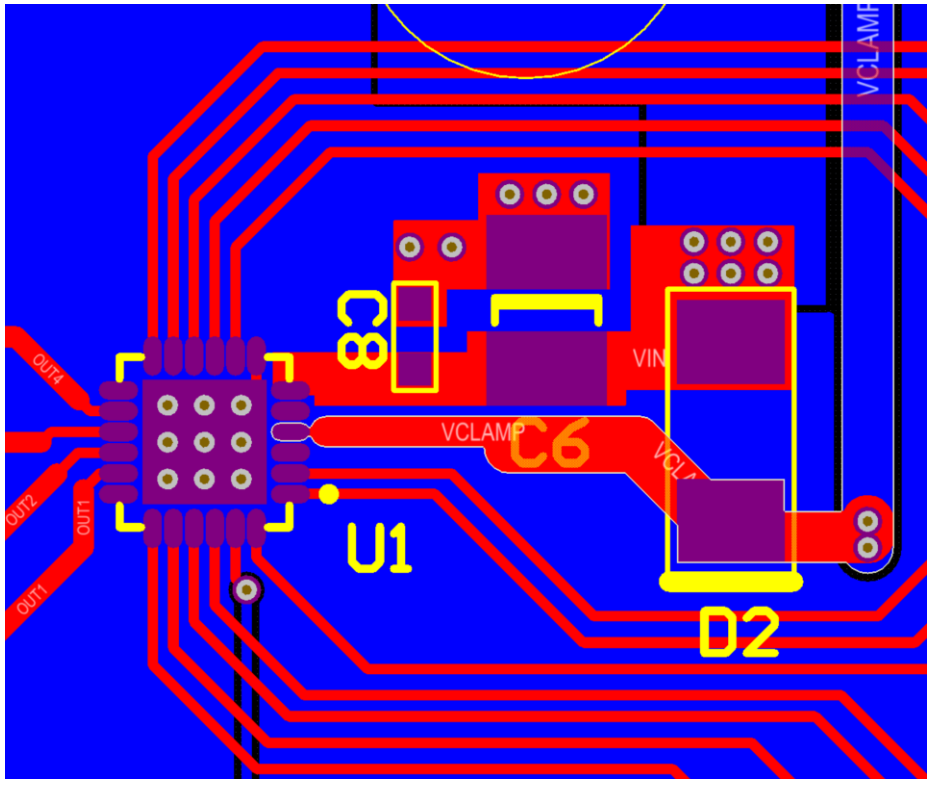


Figure 2: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

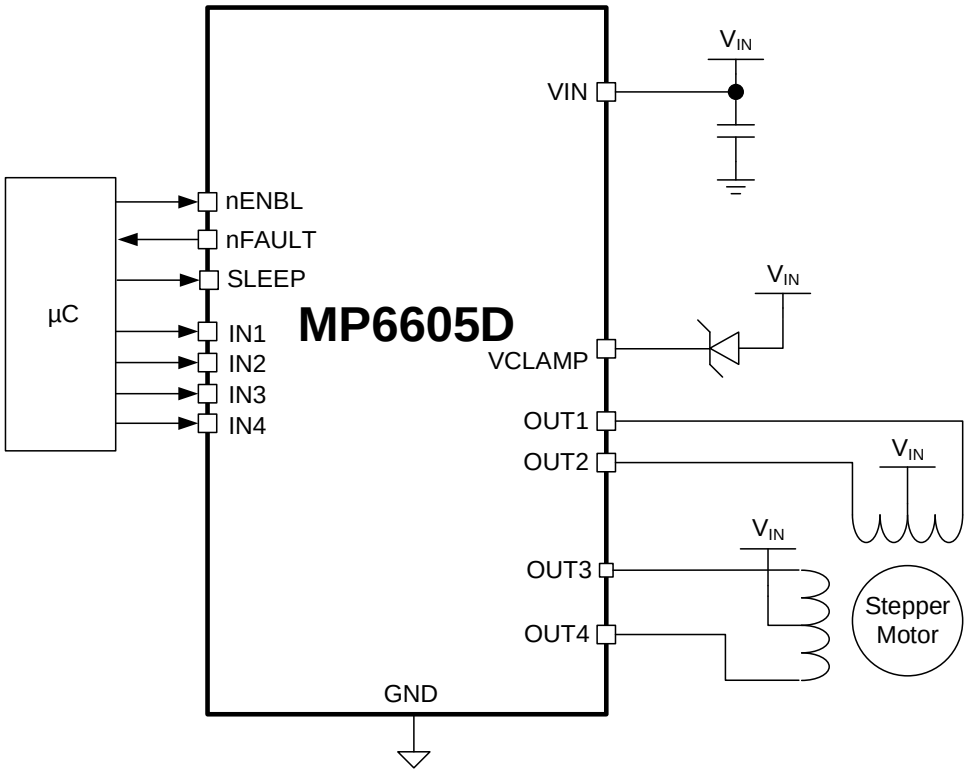
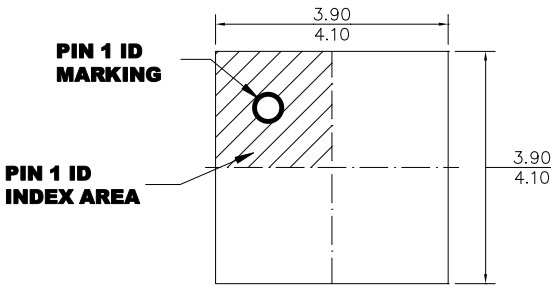


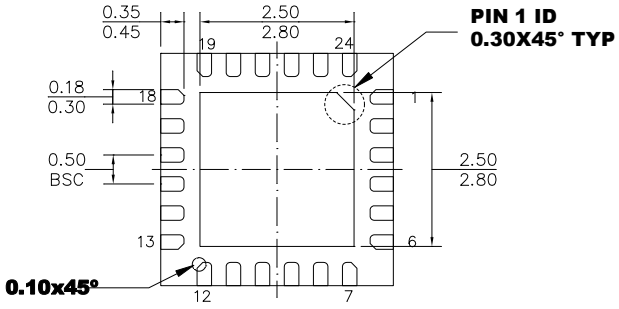
Figure 3: Typical Application Circuit

PACKAGE INFORMATION

QFN-24 (4mmx4mm)

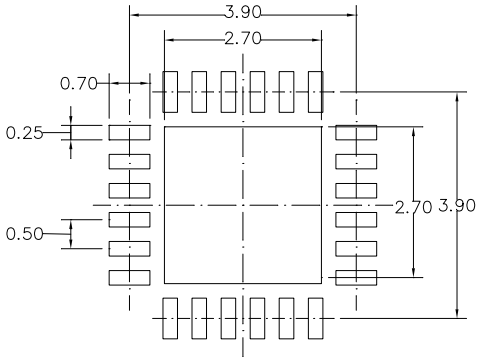


TOP VIEW



BOTTOM VIEW

SIDE VIEW

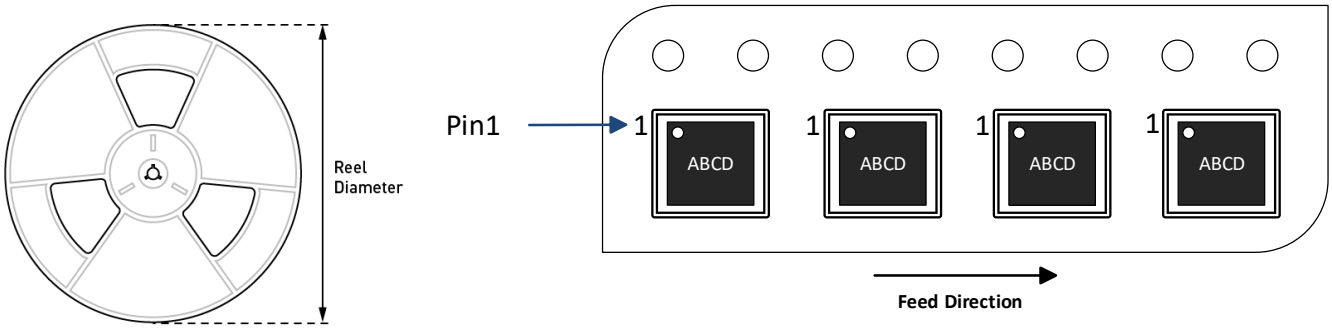


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITIES SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6605DGR-Z	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/26/2022	Initial Release	-