EV6605E-R-00A

4-Channel Low-Side Driver with Serial Interface Evaluation Board

DESCRIPTION

The EV6605E-R-00A evaluation board is designed to demonstrate the capabilities of the MP6605E, a 4-channel low-side (LS) driver with a serial interface. It integrates low-side MOSFETs (LS-FETs) and high-side (HS) clamp diodes to drive inductive loads.

The MP6605E operates from a supply voltage up to 60V, and can deliver output current (I_{OUT}) up to 1.5A. The MP6605E supports a 3.3V and 5V logic supply. Internal safety features include over-current protection (OCP), under-voltage lockout (UVLO), and over-temperature (OT) shutdown.

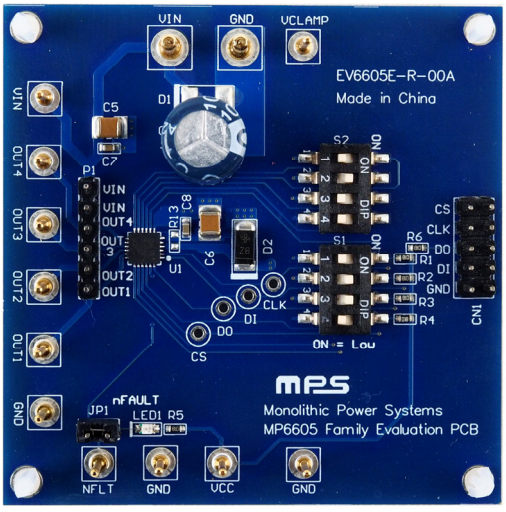
The MP6605E is typically used for unipolar stepper motors and solenoid drivers. The MP6605E is available in a QFN-24 (4mmx4mm) package.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Supply voltage range (V_{IN})	24V TVS diode connected between VIN and VCLAMP	4.5V to 30V
	VCLAMP connected to VIN	4.5V to 60V
High-side (HS) clamp voltage (V_{CLAMP})		≤60V
Maximum low-side (LS) output current (I_{OUT_LS})	For low-side MOSFETs (LS-FETs)	1.5A
Maximum HS output current (I_{OUT_HS})	For HS diodes	1.5A at duty cycle < 20%

EV6605E-R-00A EVALUATION BOARD



LxWxH (6.35cmx6.35cmx2.5cm)

Board Number	MPS IC Number
EV6605E-R-00A	MP6605EGR

QUICK START GUIDE

1. Preset the logic power supply voltage (typically 3.3V or 5V).
2. To preset the input power supply voltage, follow the steps below:
   a. Connect the 24V TVS diode between the VIN and VCLAMP pins (where V_{IN} is between 4.5V and 30V).
   b. Connect VCLAMP to VIN (where V_{IN} is between 4.5V and 60V).
3. Connect the SPI communication interface to CN1.
4. Connect the loads to the OUTx terminals.
5. Connect the logic power supply terminals to:
   a. Positive (+): VCC
   b. Negative (-): GND
6. Connect the input power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
7. Set the physical device address via S2.
8. LED1 indicates fault events including over-current protection (OCP), under-voltage lockout (UVLO), and over-temperature (OT) shutdown.

   Figure 1 shows the measurement equipment set-up.

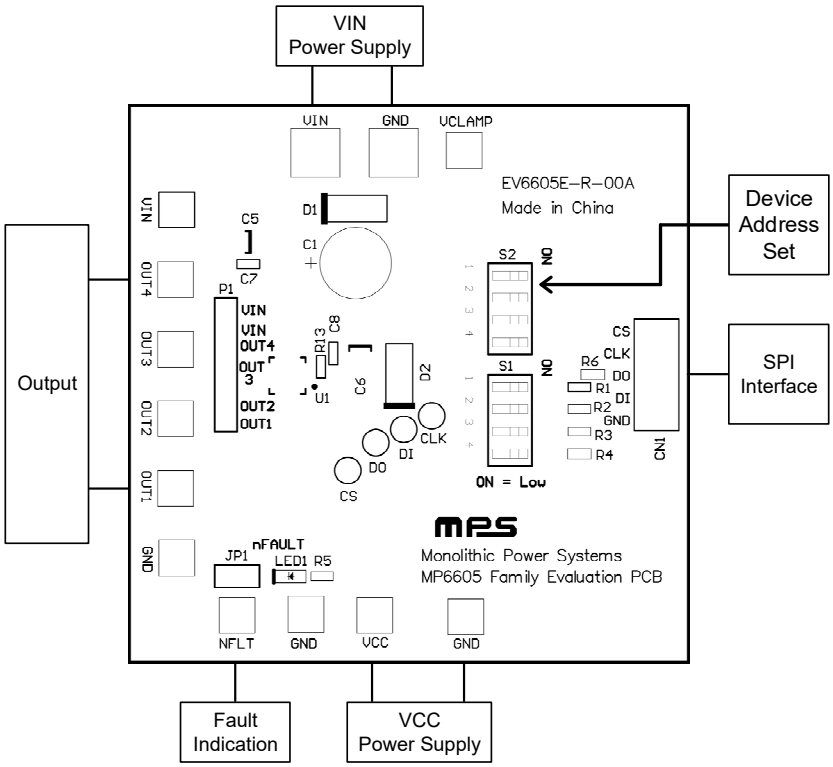


Figure 1: Measurement Equipment Test Set-Up

GUI OPERATION

To configure the device using the graphic user interface (GUI), refer to Figure 2 and follow the steps below:

1. Select the SPI clock frequency (the default is 100kHz).
2. Input the hexadecimal data to Send Buf (e.g. FE 0F 7E).
3. Set the delay time (denoted as “Delay Time” in Figure 2) under the Send Buf section. The delay time is set between two bytes. Typically, its default value is used.
4. Click “Send” to send the typed data once, or click “Loop Send” to send the data repeatedly with a fixed frequency.
5. Read the serial data output in Receive Buf. Note that this data cannot be displayed in loop send mode.

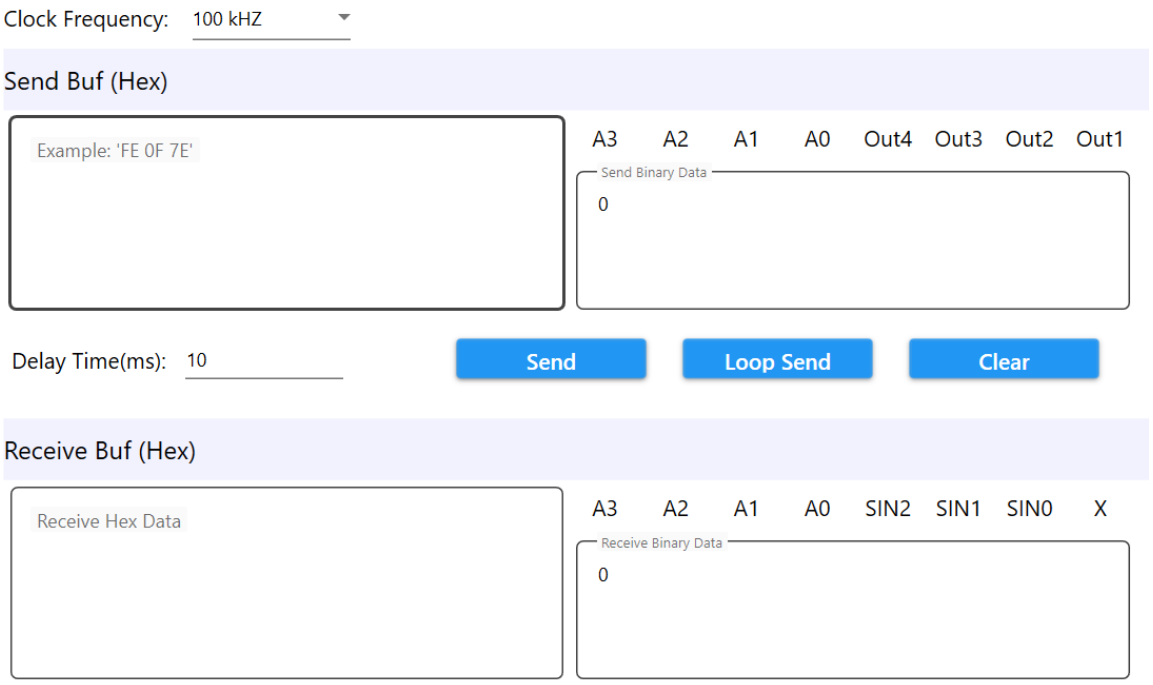


Figure 2: GUI Operation Configuration

EVALUATION BOARD SCHEMATIC

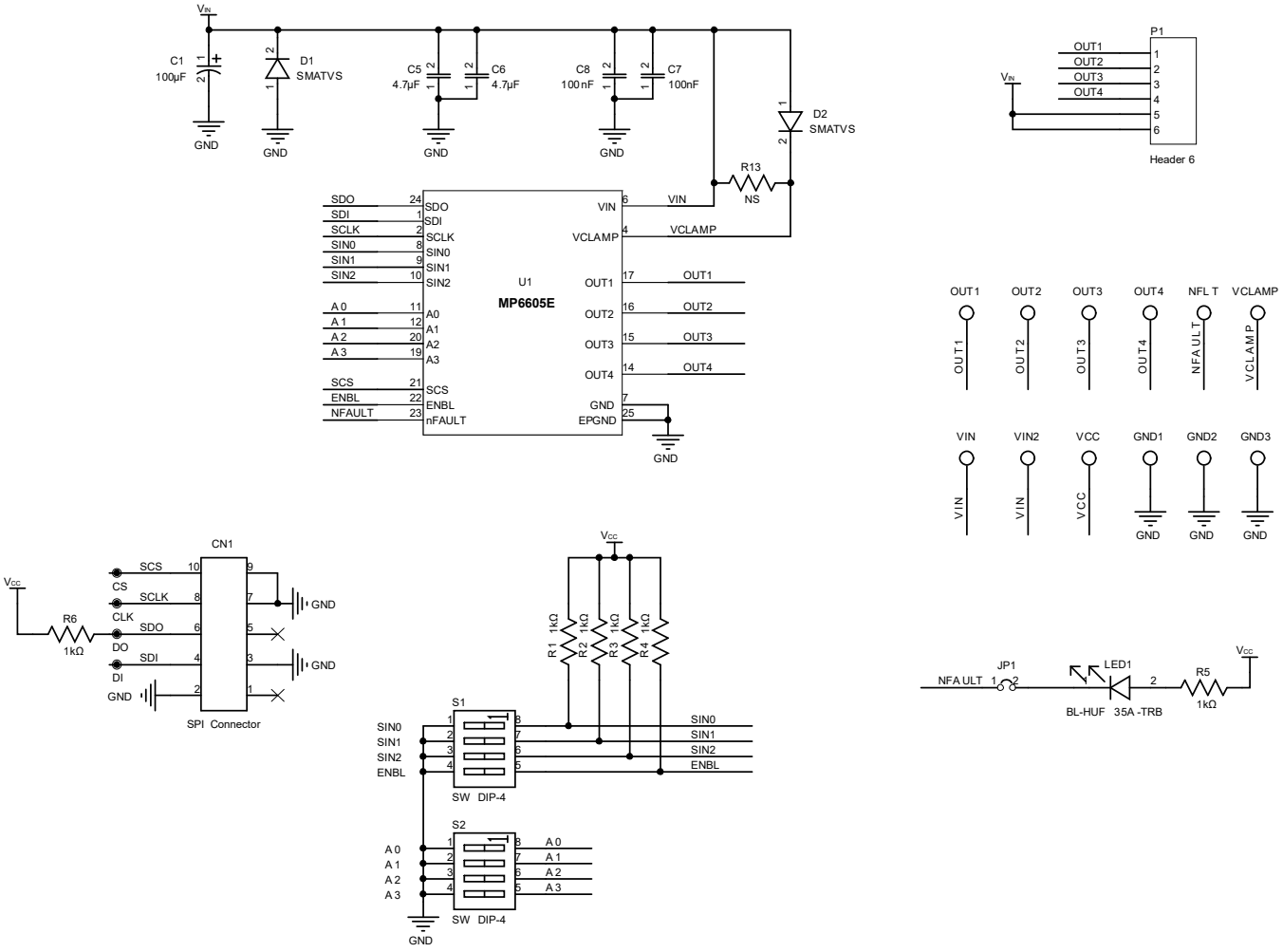


Figure 3: Evaluation Board Schematic

EV6605E-R-00A BILL OF MATERIALS

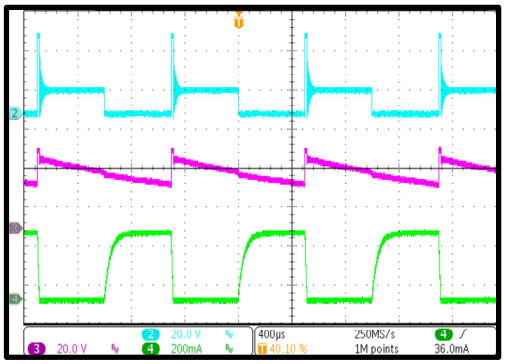
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	100µF	Electrolytic capacitor, 100V	DIP	Jianghai	CD263-100V100
2	C5, C6	4.7µF	Ceramic capacitor, 100V, X8L	1210	Murata	GCM32DL8EL475KE07L
2	C7, C8	100nF	Ceramic capacitor, 100V, X7R	0603	Murata	GRM188R72A104KA35D
6	R1, R2, R3, R4, R5, R6	1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071KL
1	R13	NS				
1	D2	24V	TVS diode	DO-214C-2	Vishay	SMAJ24A
2	S1, S2	4-bit	Dial switch	SMD	Wurth	418121270804
1	LED1	20mA	Red LED	0805	Baihong	BL-HUE35A-AV-TRB
1	JP1	2.54mm	Single-line needle with jumper	SIP	Custom	
1	P1	2.54mm	Single-line needle	SIP	Custom	
1	CN1	2.54mm	Dual-line needle	DIP	Custom	
2	VIN, GND1	2mm	Needle	SIP	Custom	
11	VCLAMP, VIN, OUT1, OUT2, OUT3, OUT4, NFLT, GND, VCC	1mm	Needle	SIP	Custom	
1	U1	MP6605E	4-channel low-side driver with serial interface	QFN-24 (4mmx 4mm)	MPS	MP6605EGR

EVB TEST RESULTS

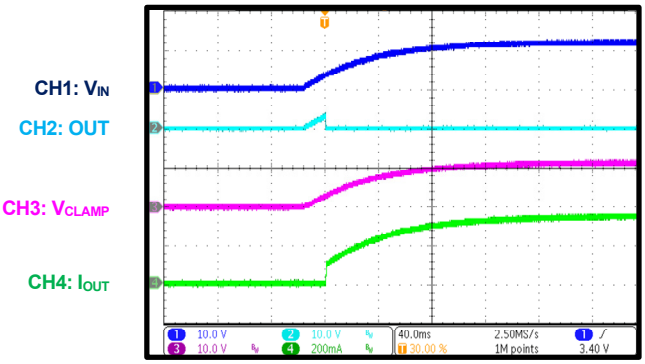
V_{IN} = 12V, V_{CLAMP} = 24V TVS to VIN, T_A = 25°C, resistor + inductor load: R = 33Ω, L = 1.5mH per channel, unless otherwise noted.

Normal Operation

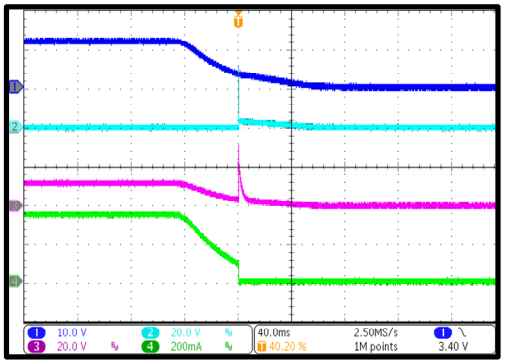
f_{SW} = 1kHz



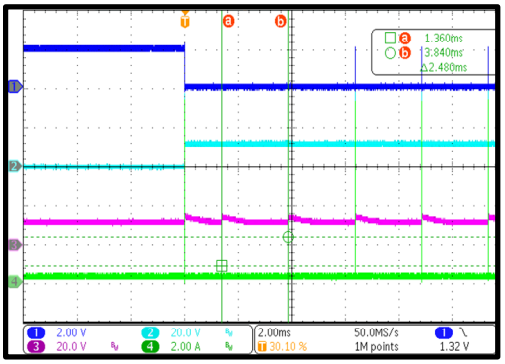
Start-Up through VIN



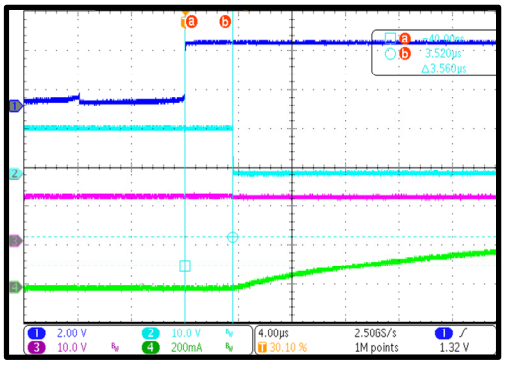
Shutdown through VIN



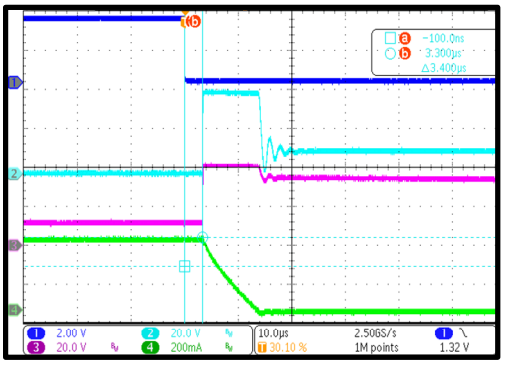
SCP



Chip Enabled



Chip Disabled



PCB LAYOUT

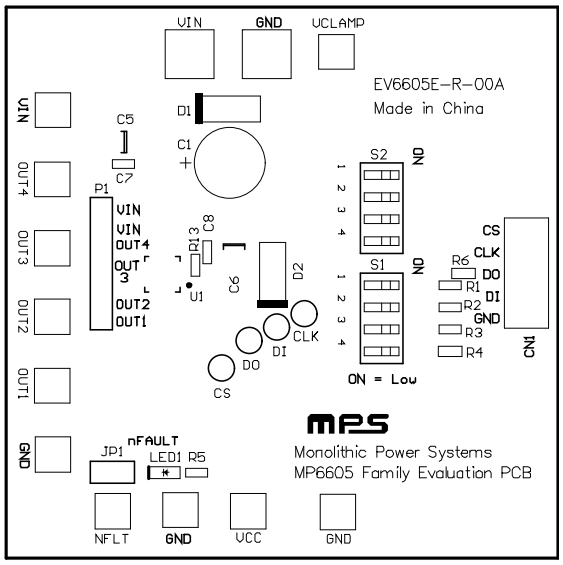


Figure 4: Top Silk

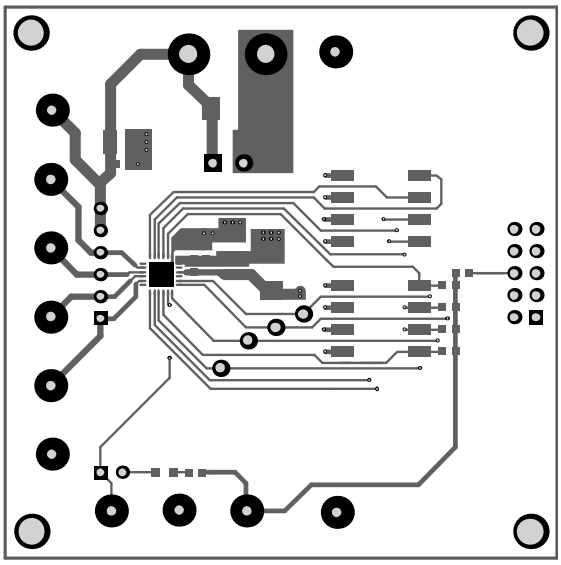


Figure 5: Top Layer

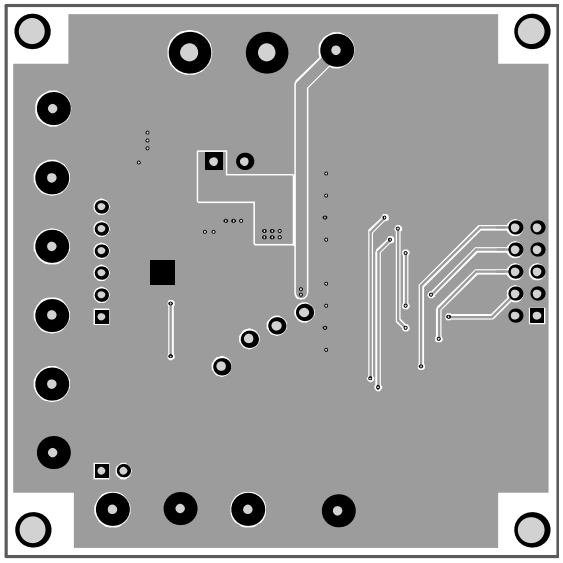


Figure 6: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/11/2022	Initial Release	-