2N3713 thru 2N3716 NPN

361-392

SILICON NPN POWER TRANSISTORS

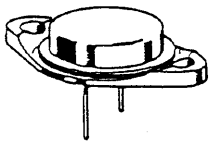
. . . designed for medium-speed switching and amplifier applications. These devices feature:

- Total Switching Time at 3 A typically 1.15 μs
- Gain Ranges Specified at 1 A and 3 A
- Low $V_{CE(sat)}$: typically 0.5V at I_C = 5A and I_B = 0.5A
- Excellent Safe Operating Areas
- Complement to 2N3789-92

10 AMPERE

POWER TRANSISTORS
SILICON NPN

60-80 VOLTS
150 WATTS



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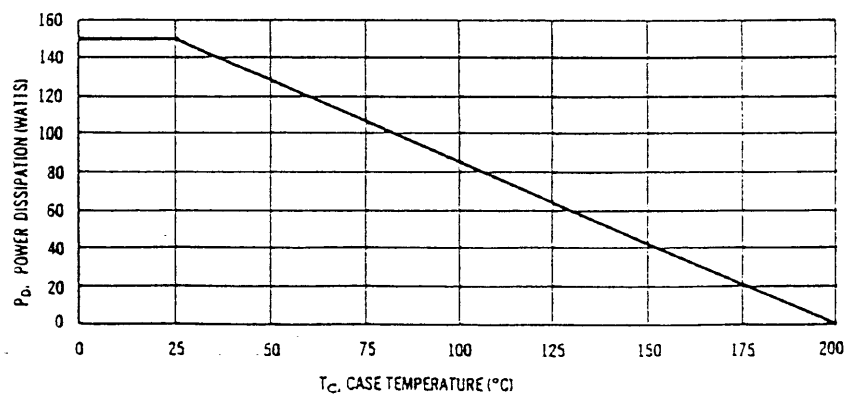
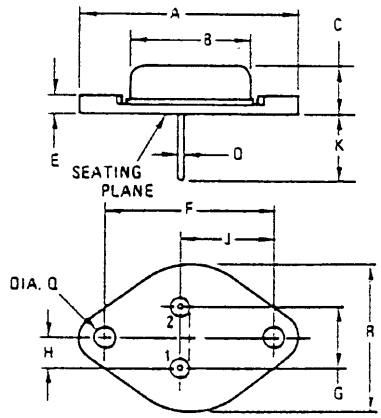
MAXIMUM RATINGS

Rating	Symbol	2N3713 2N3715	2N3714 2N3716	Unit
Collector-Base Voltage	V_{CB}	80	100	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current	I_C	10	10	Amps
Base Current	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resistance	θ_{JC}	1.17	1.17	°C/W
Operating Junction and Storage Temperature Range	T_J and T_{stg}	-65 to +200		°C

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Limits are indicated by Figures 12, 13. Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

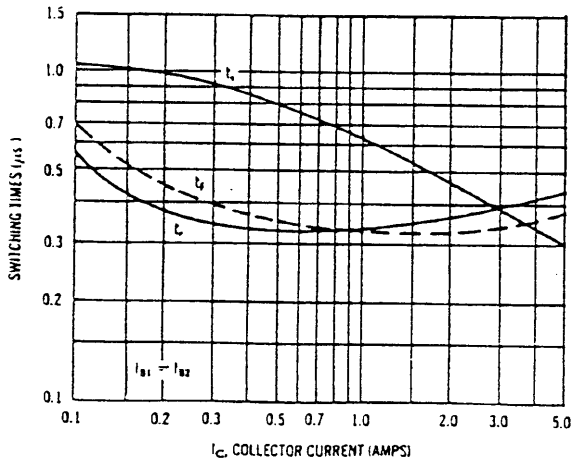
Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Emitter-Base Cutoff Current (V_{EB} 7 Vdc)	All Types	I_{EBO}	—	5	mAdc
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc)	2N3713, 2N3715		—	1	
(V_{CE} = 100 Vdc, V_{BE} = -1.5 Vdc)	2N3714, 2N3716		—	1	
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3713, 2N3715		—	10	
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3714, 2N3716		—	10	
Collector-Emitter Sustaining Voltage*		$V_{CEO(sus)}$*			Vdc
(I_C = 200 mAdc, I_B = 0)	2N3713, 2N3715		60	—	
	2N3714, 2N3716		80	—	
DC Current Gain*		h_{FE}*			—
(I_C = 1 Adc, V_{CE} = 2 Vdc)	2N3713, 2N3714		25	90	
	2N3715, 2N3716		50	150	
(I_C = 3 Adc, V_{CE} = 2 Vdc)	2N3713, 2N3714		15	—	
	2N3715, 2N3716		30	—	
Collector-Emitter Saturation Voltage*		$V_{CE(sat)}$*			Vdc
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3713, 2N3714		—	1.0	
	2N3715, 2N3716		—	0.8	
Base-Emitter Saturation Voltage*		$V_{BE(sat)}$*			Vdc
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3713, 2N3714		—	2.0	
	2N3715, 2N3716		—	1.5	
Base-Emitter Voltage*		V_{BE}*			Vdc
(I_C = 3 Adc, V_{CE} = 2 Vdc)	All Types		—	1.5	
Small Signal Current Gain		h_{fe}			—
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 MHz)	All Types		4	—	
Switching Times (Figure 2)			Typ		μs
(I_C = 5A, I_{B1} = I_{B2} = 0.5 Adc)					
Rise Time		t_r	0.45		
Storage Time		t_s	0.3		
Fall Time		t_f	0.4		

*Use sweep test to prevent overheating

FIGURE 2 – TYPICAL SWITCHING TIMES



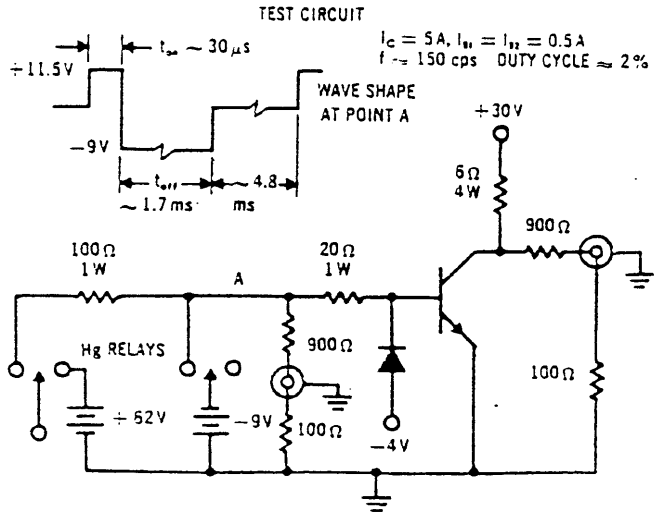


FIGURE 3 – COLLECTOR CURRENT versus BASE CURRENT

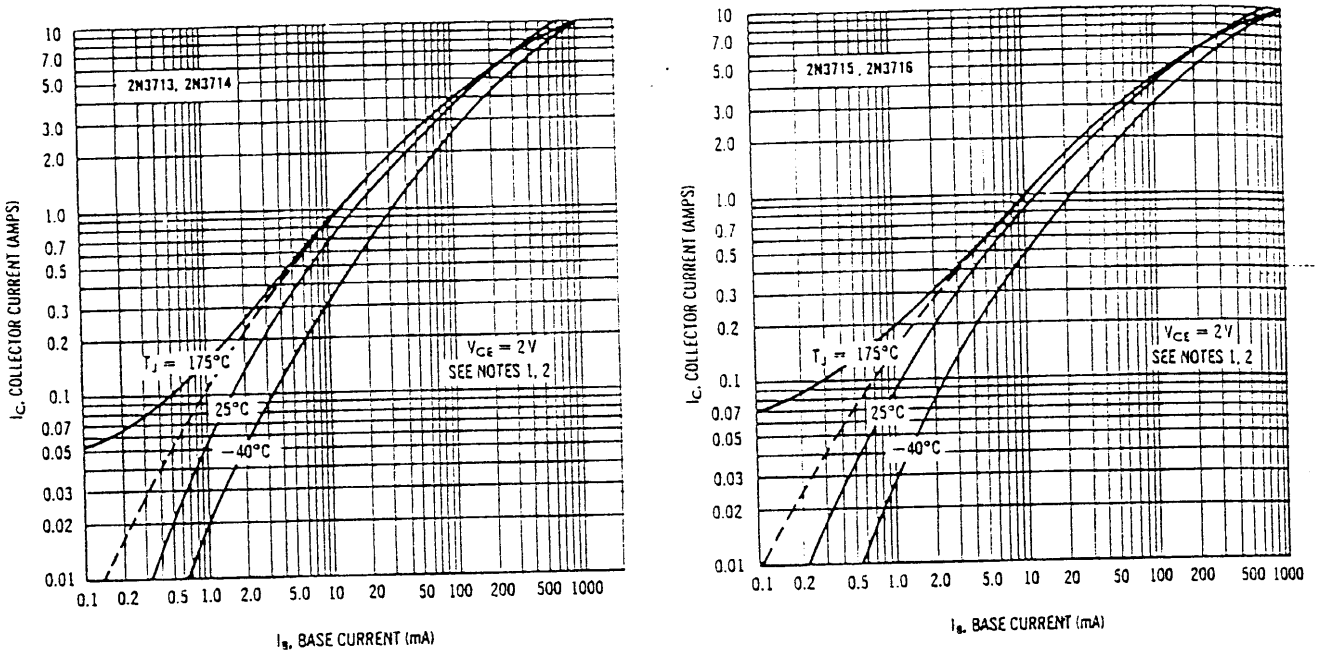


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FIGURE 4 – BASE CURRENT-VOLTAGE VARIATIONS

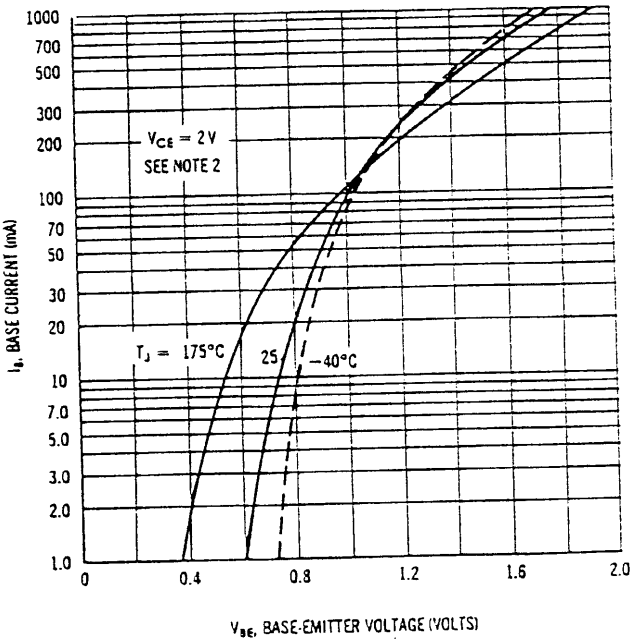
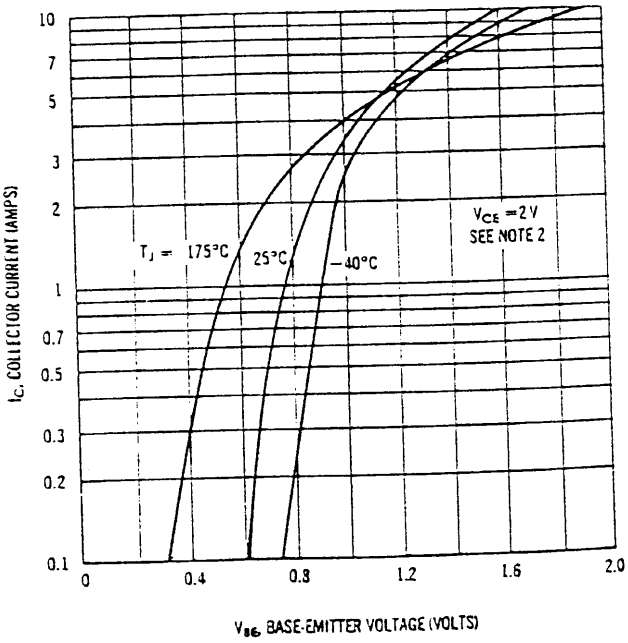


FIGURE 5 – COLLECTOR CURRENT-VOLTAGE VARIATIONS



NOTE 1. Dotted line indicates metered base current plus the I_{CBO} of the transistor at 175°C.

NOTE 2. Pulse test: pulse width ≈ 200 μsec, duty cycle ≈ 1.5%

FIGURE 6 – COLLECTOR-EMITTER SATURATION VOLTAGE VARIATIONS

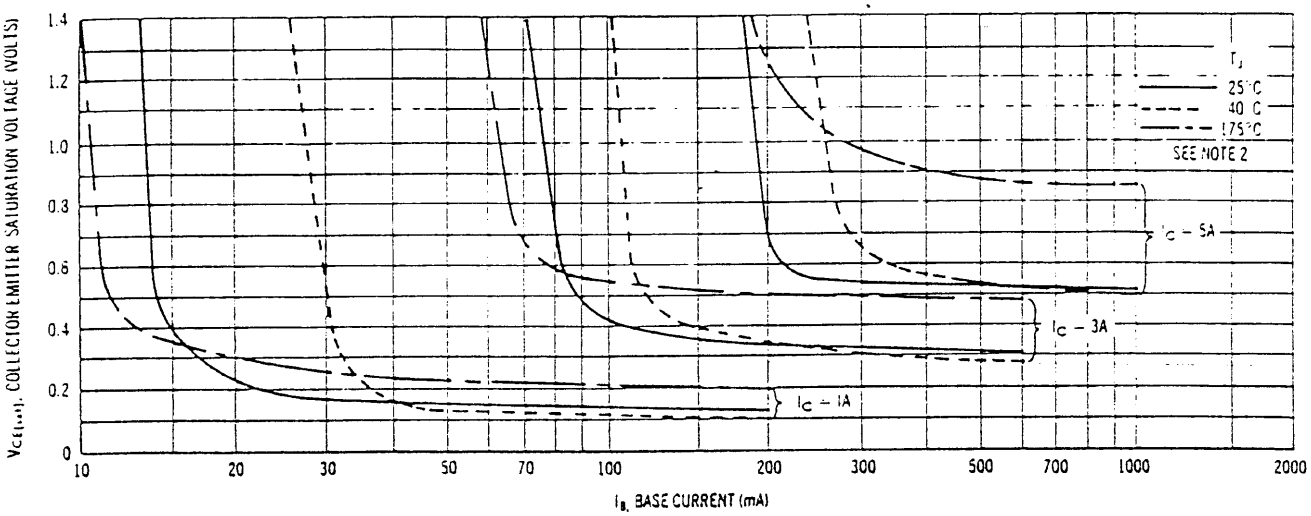


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE VARIATIONS

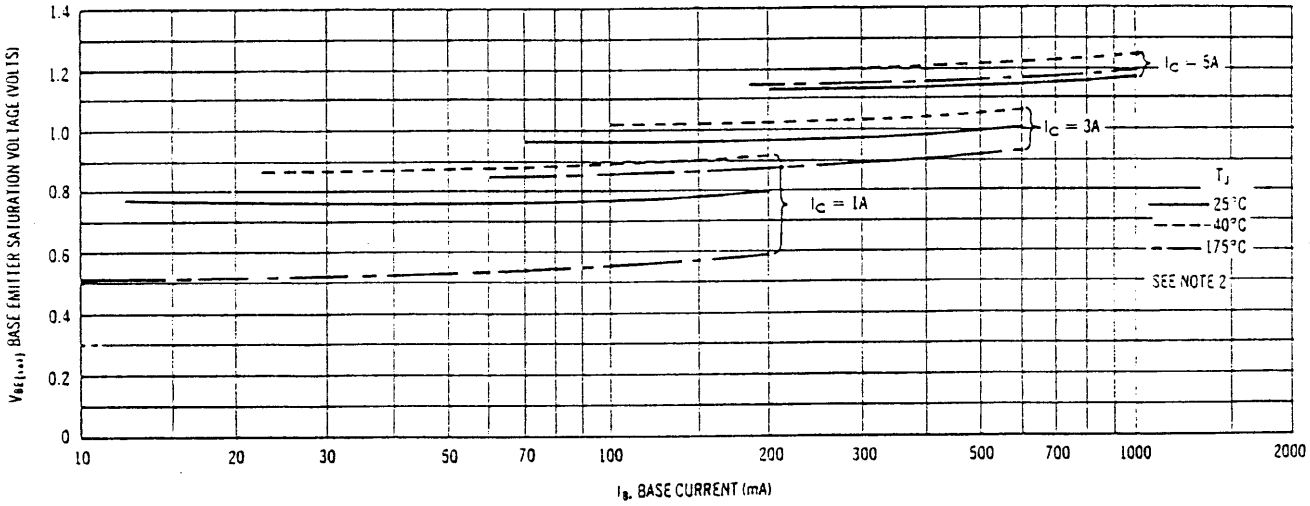


FIGURE 8 – COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

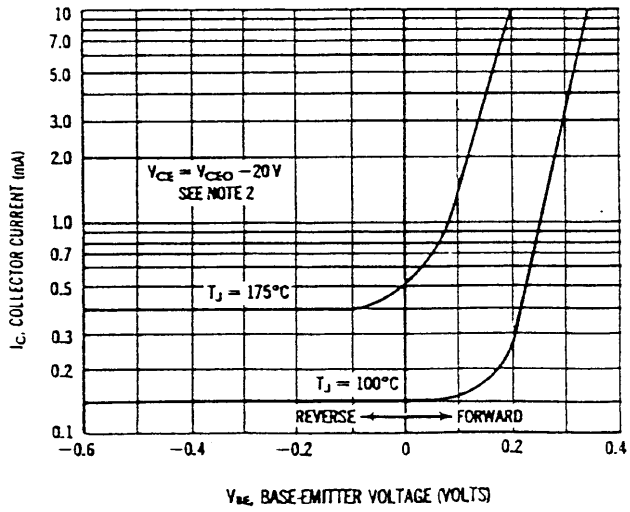


FIGURE 9 – COLLECTOR CURRENT versus BASE-EMITTER RESISTANCE

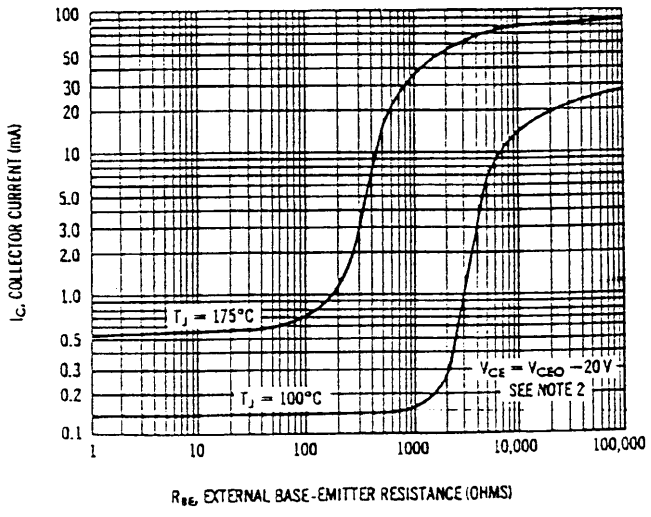
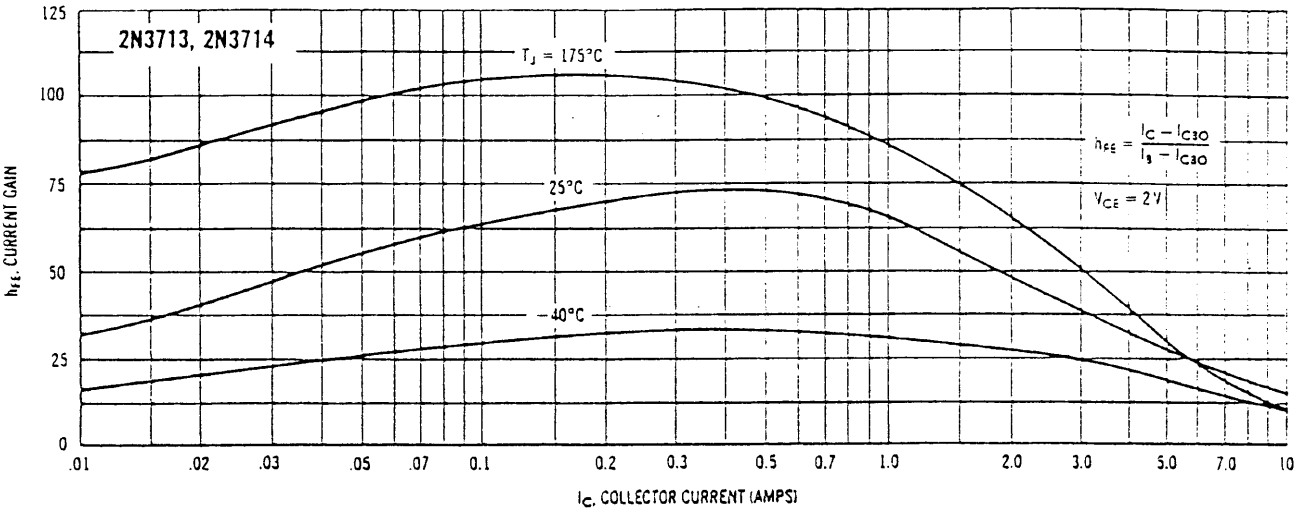


FIGURE 10 – CURRENT GAIN VARIATIONS



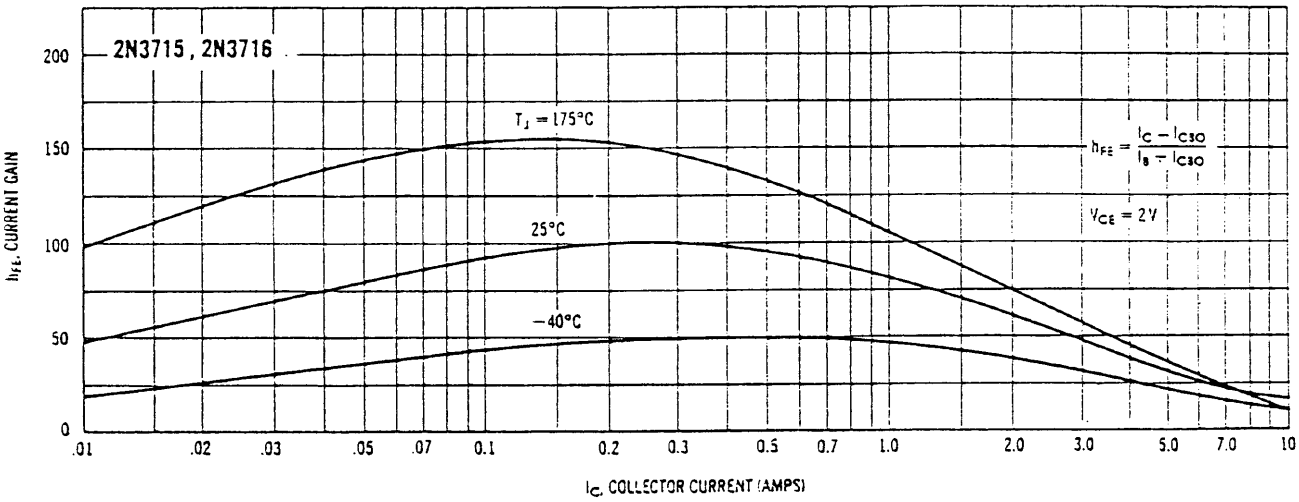
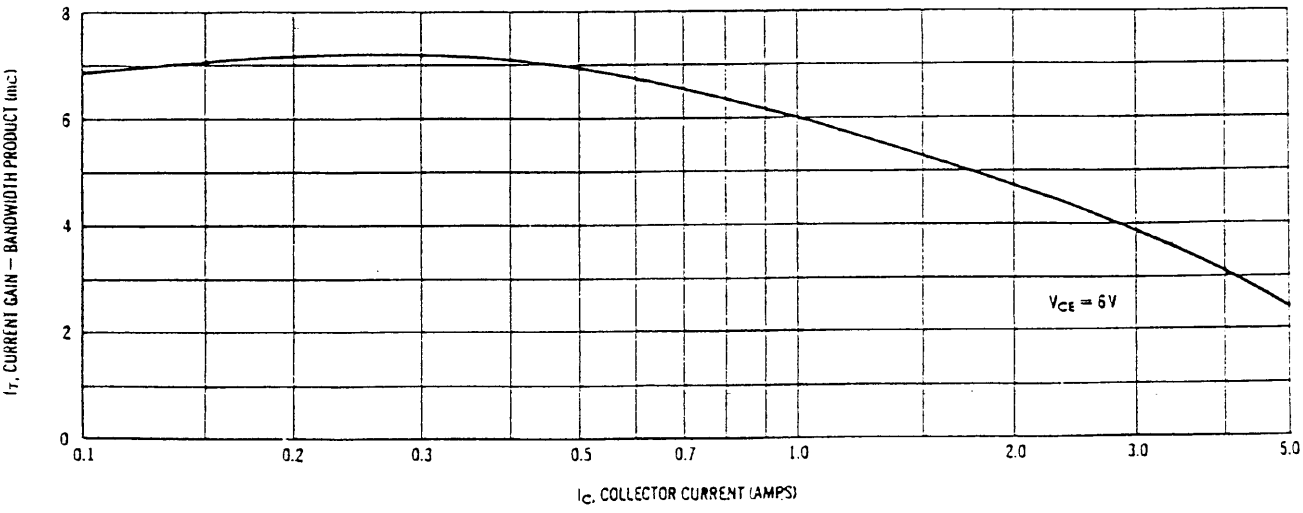


FIGURE 11 – CURRENT GAIN – BANDWIDTH PRODUCT versus COLLECTOR CURRENT



SAFE OPERATING AREAS

FIGURE 12 – 2N3713, 2N3715

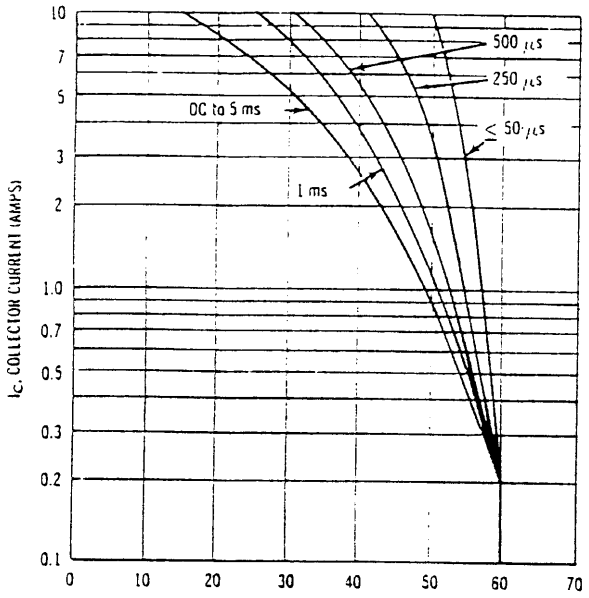
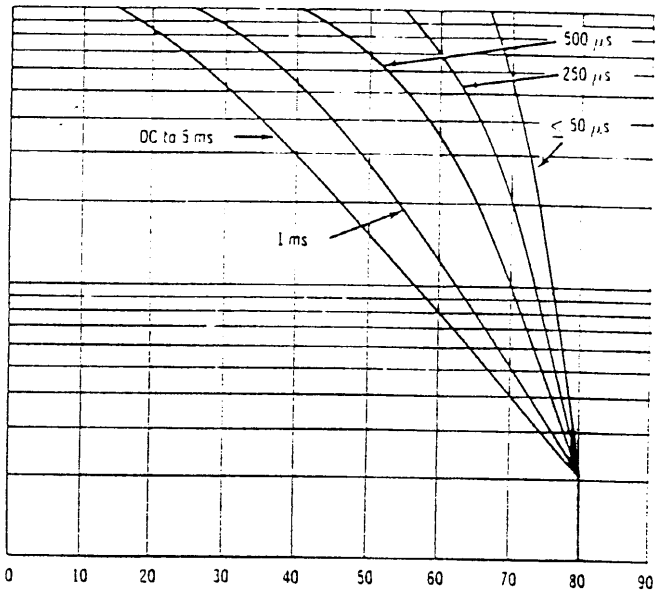


FIGURE 13 – 2N3714, 2N3716



V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate I_C — V_{CE} limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.