



Customer Information Notification

202306035I : i.MX RT1170 Reference Manual Update to Rev 2

Note: This notice is NXP Company Proprietary.

Issue Date: Jul 22, 2023 **Effective date:** Jul 23, 2023

Dear Emma Tempest,

Here is your personalized notification about a NXP general announcement.

For detailed information we invite you to [view this notification online](#)

Management summary

The reference manual has been updated to correct errors and / or provide additional technical clarification on some device features.

Change Category

<input type="checkbox"/> Wafer Fab Process	<input type="checkbox"/> Assembly Process	<input type="checkbox"/> Product Marking	<input type="checkbox"/> Test Process	<input type="checkbox"/> Design
<input type="checkbox"/> Wafer Fab Materials	<input type="checkbox"/> Assembly Materials	<input type="checkbox"/> Mechanical Specification	<input type="checkbox"/> Test Equipment	<input type="checkbox"/> Errata
<input type="checkbox"/> Wafer Fab Location	<input type="checkbox"/> Assembly Location	<input type="checkbox"/> Packing/Shipping/Labeling	<input type="checkbox"/> Test Location	<input type="checkbox"/> Electrical spec./Test coverage
<input type="checkbox"/> Firmware <input checked="" type="checkbox"/> Other: Reference Manual				

PCN Overview

Description

NXP Semiconductors announces a reference manual update to revision 2 for i.MX RT1170.

The revision history included in the updated document provides a detailed description of the changes.

Below are changes to be highlighted:

1. Error correction - Add 1Gbps ENET QoS w/TSN block in Block diagram
2. Error correction - For System memory map (CM7) , Merged 2036_0000 to 203F_FFFF and also added a note for this below.
3. Error correction - CM4 interrupts Updated IRQ 62 as reserved
4. Error correction - CM7 interrupts Updated IRQ 62 and 109 as reserved
5. Error correction - All DSE and SRE bits should be reserved in IOMUXC SNVS register description section.
6. New information – Fuse: Added the 0x950[0] fuse in Table "FlexSPI (Serial NOR) boot fusemap".
7. Error correction – SEMC: For SDRAM interface, maximum size should be 1024Mb
8. New information – SEMC: For NAND interface, maximum space is 512GB
9. New information – FlexRAM, added Error Injection registers are added at 8C, 90, 94, 98.
10. New information – XECC: the code to enable XECC should be placed in internal RAM to avoid

bus hung.

11. Error correction – MIPI CSI-2: Removed two feature in feature list.

The i.MX RT1170 reference manual revision 2 is attached to this notice, and can be found at:
<https://www.nxp.com/products/processors-and-microcontrollers/arm-microcontrollers/i-mx-rt-crossover-mcus/i-mx-rt1170-crossover-mcu-dual-core-arm-cortex-m7-and-cortex-m4-operating-up-to-1-ghz:i.MX-RT1170>

Corresponding ZVEI Delta Qualification Matrix ID: SEM-DS-02

Reason

The reference manual has been updated to correct errors and / or provide additional technical clarification on some device features.

Identification of Affected Products

Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No Impact on form, fit, function, reliability or quality

Additional information

Additional documents: [view online](#)

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly:

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NXP Quality Management Team.

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