

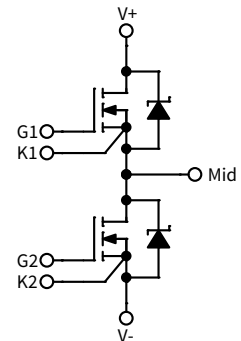
CAS310M17BM3

1700 V, 310 A, Silicon Carbide, Half-Bridge Module

V_{DS}	1700 V
I_{DS}	310 A

Technical Features

- Industry Standard 62mm Footprint
- Ultra Low Loss , High-Frequency Operation
- Zero Reverse Recovery from Diodes
- Zero Turn-off Tail Current from MOSFET
- Normally-off, Fail-safe Device Operation
- Copper Baseplate and Aluminum Nitride Insulator



Applications

- Induction Heating
- Motor Drives
- Renewables
- Railway Auxiliary & Traction
- EV Fast Charging
- UPS and SMPS

System Benefits

- 62mm Form Factor Enables System Retrofit
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC

Maximum Parameters (Verified by Design)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Voltage	V_{DS}			1700	V		
Gate-Source Voltage, Maximum Value	$V_{GS\ max}$	-8		+19		Transient, <100 ns	Fig. 33
Gate-Source Voltage, Recommended	$V_{GS\ op}$	-4		+15		Static	
DC Continuous Drain Current	I_D		399		A	$V_{GS} = 15\ V, T_c = 25\ ^\circ C, T_{VJ} \leq 175\ ^\circ C$	Fig. 21
			307			$V_{GS} = 15\ V, T_c = 90\ ^\circ C, T_{VJ} \leq 175\ ^\circ C$	
DC Source-Drain Current (Diode)	I_{SD}		482			$V_{GS} = -4\ V, T_c = 25\ ^\circ C, T_{VJ} \leq 175\ ^\circ C$	
			345			$V_{GS} = -4\ V, T_c = 90\ ^\circ C, T_{VJ} \leq 175\ ^\circ C$	
Pulsed Drain Current	$I_{D\ (pulsed)}$			620		$t_{p\ max}$ limited by $T_{VJ\ max}$ $V_{GS} = 15\ V, T_c = 25\ ^\circ C$	
Virtual Junction Temperature	$T_{VJ\ op}$	-40		150	$^\circ C$	Operation	
				175		Intermittent with Reduced Life	

MOSFET Characteristics (Per Position) ($T_{VJ} = 25\text{ °C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1700				$V_{GS} = 0\text{ V}, T_{VJ} = -40\text{ °C}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.8	V	$V_{DS} = V_{GS}, I_D = 102\text{ mA}$	
			2.0			$V_{DS} = V_{GS}, I_D = 102\text{ mA}, T_{VJ} = 175\text{ °C}$	
Zero Gate Voltage Drain Current	I_{DSS}		26.4	2560	μA	$V_{GS} = 0\text{ V}, V_{DS} = 1700\text{ V}$	
Gate-Source Leakage Current	I_{GSS}		4	1000	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		4.29	5.80	m Ω	$V_{GS} = 15\text{ V}, I_D = 310\text{ A}$	Fig. 2
			8.42			$V_{GS} = 15\text{ V}, I_D = 310\text{ A}, T_{VJ} = 150\text{ °C}$	Fig. 3
Transconductance	g_{fs}		290		S	$V_{DS} = 20\text{ V}, I_D = 310\text{ A}$	Fig. 4
			284			$V_{DS} = 20\text{ V}, I_D = 310\text{ A}, T_{VJ} = 150\text{ °C}$	
Turn-On Switching Energy, $T_{VJ} = 25\text{ °C}$ $T_{VJ} = 125\text{ °C}$ $T_{VJ} = 150\text{ °C}$	E_{On}		4.4		mJ	$V_{DD} = 900\text{ V},$ $I_D = 310\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V},$ $R_{G(OFF)} = 1.0\ \Omega, R_{G(ON)} = 1.0\ \Omega,$ $L = 13.6\ \mu\text{H}$	Fig. 11 Fig. 13
			4.1				
			4.0				
Turn-Off Switching Energy, $T_{VJ} = 25\text{ °C}$ $T_{VJ} = 125\text{ °C}$ $T_{VJ} = 150\text{ °C}$	E_{Off}		7.2				
			7.4				
			7.4				
Internal Gate Resistance	$R_{G(int)}$		1.85		Ω	$f = 100\text{ kHz}, V_{AC} = 25\text{ mV}$	
Input Capacitance	C_{iss}		31.5		nF	$V_{GS} = 0\text{ V}, V_{DS} = 1000\text{ V},$ $V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$	Fig. 9
Output Capacitance	C_{oss}		1.8				
Reverse Transfer Capacitance	C_{rss}		45				
Gate to Source Charge	Q_{GS}		320		nC	$V_{DS} = 1200\text{ V}, V_{GS} = -4\text{ V}/15\text{ V},$ $I_D = 310\text{ A},$ Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		280				
Total Gate Charge	Q_G		996				
FET Thermal Resistance, Junction to Case	$R_{th\text{ JC}}$		0.092		$^{\circ}\text{C}/\text{W}$		Fig. 17

Diode Characteristics (Per Position) ($T_{VJ} = 25\text{ °C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_F		1.78		V	$V_{GS} = -4\text{ V}, I_F = 310\text{ A}, T_{VJ} = 25\text{ °C}$	Fig. 7
			2.50			$V_{GS} = -4\text{ V}, I_F = 310\text{ A}, T_{VJ} = 150\text{ °C}$	
Reverse Recovery Time	t_{rr}		27		ns	$V_{GS} = -4\text{ V}, I_{SD} = 310\text{ A}, V_R = 900\text{ V}$ $di/dt = 26.5\text{ A/ns}, T_{VJ} = 150\text{ °C}$	Fig. 32
Reverse Recovery Charge	Q_{rr}		4.5		μC		
Peak Reverse Recovery Current	I_{rrm}		281		A		
Reverse Recovery Energy, $T_{VJ} = 25\text{ °C}$ $T_{VJ} = 125\text{ °C}$ $T_{VJ} = 150\text{ °C}$	E_{rr}		3.5		mJ	$V_{DS} = 900\text{ V}, I_D = 310\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V}, R_{G(ext)} = 1.0\ \Omega,$ $L = 13.6\ \mu\text{H}$	Fig. 14 Note 1
			3.8				
			3.9				
Diode Thermal Resistance, JCT. to Case	$R_{th\text{ JC}}$		0.086		$^{\circ}\text{C}/\text{W}$		Fig. 18

Note:

¹ SiC Schottky diodes do not have reverse recovery energy but still contribute capacitive energy.



Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Package Resistance, M1 (High-Side)	R_{3-1}		1.31		m Ω	$T_c = 25^\circ\text{C}$, $I_{SD} = 310\text{ A}$, Note 2	
			1.84			$T_c = 125^\circ\text{C}$, $I_{SD} = 310\text{ A}$, Note 2	
Package Resistance, M2 (Low-Side)	R_{1-2}		1.26	$T_c = 25^\circ\text{C}$, $I_{SD} = 310\text{ A}$, Note 2			
			1.77	$T_c = 125^\circ\text{C}$, $I_{SD} = 310\text{ A}$, Note 2			
Stray Inductance	L_{Stray}		11.1		nH	Between DC- and DC+, $f = 10\text{ MHz}$	
Case Temperature	T_c	-40		125	$^\circ\text{C}$		
Mounting Torque	M_s		4	5	5.5	N-m	Baseplate, M6-1.0 bolts
			4	5	5.5		Power Terminals, M6-1.0 bolts
Weight	W		300		g		
Case Isolation Voltage	V_{isol}	5			kV	AC, 50 Hz, 1 minute	
Clearance Distance			9		mm	Terminal to Terminal	
			30			Terminal to Baseplate	
Creepage Distance			30			Terminal to Terminal	
			40			Terminal to Baseplate	

Note:

²Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance



Typical Performance

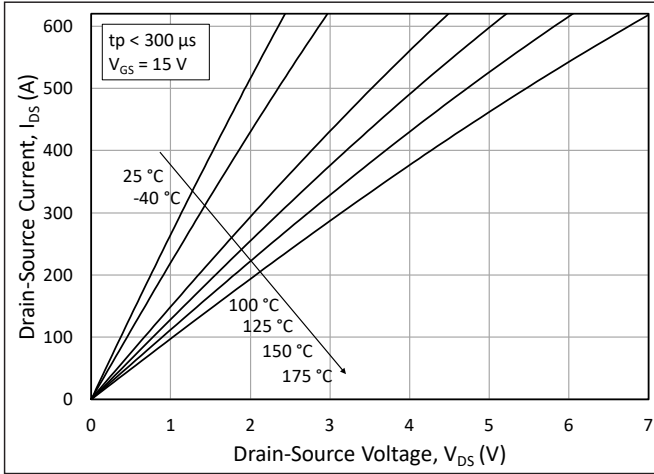


Figure 1. Output Characteristics for Various Junction Temperatures

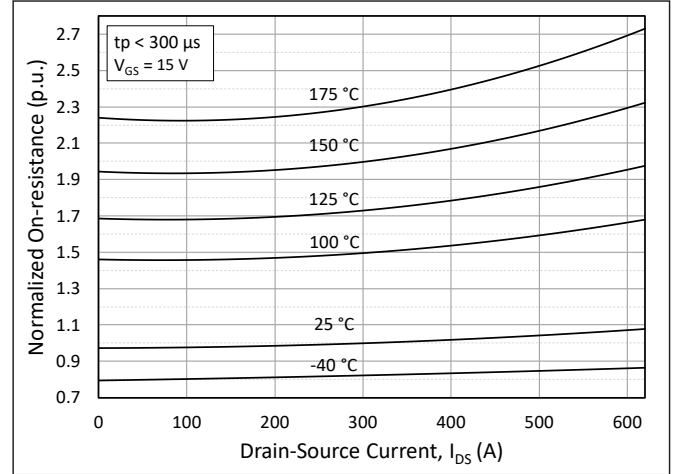


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

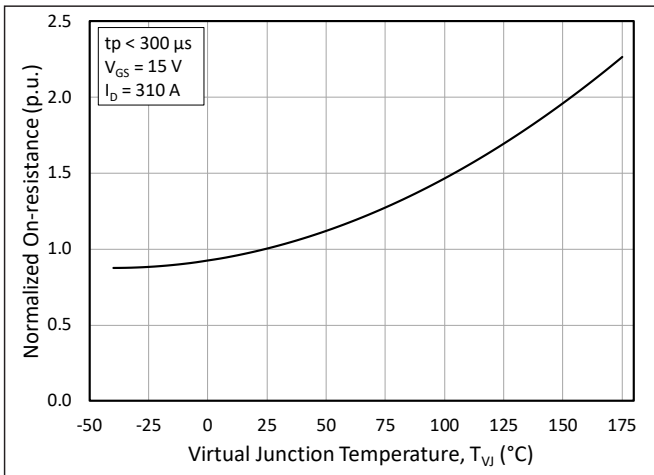


Figure 3. Normalized On-State Resistance vs. Junction Temperature

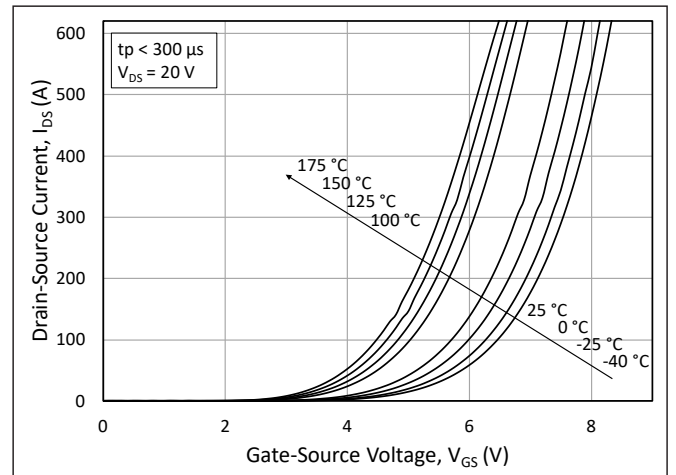


Figure 4. Transfer Characteristic for Various Junction Temperatures

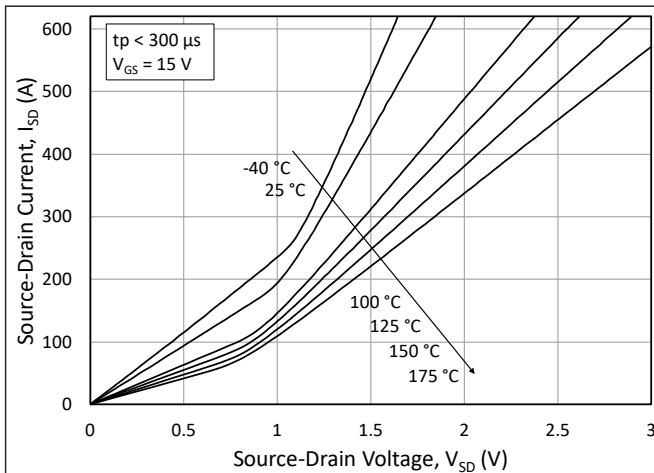


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15\text{ V}$

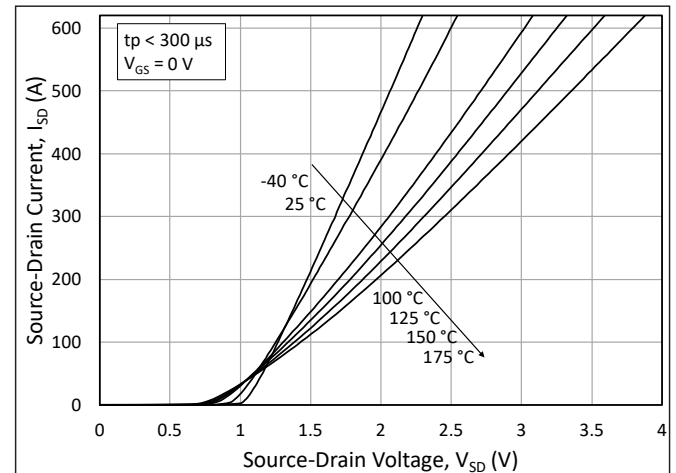


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0\text{ V}$ (Diode)



Typical Performance

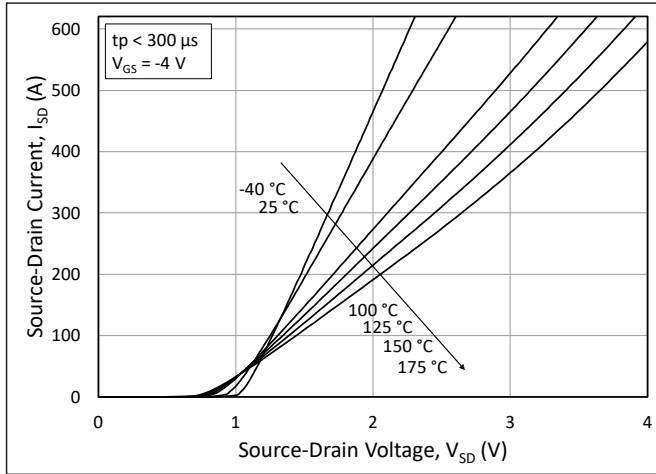


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4$ V (Diode)

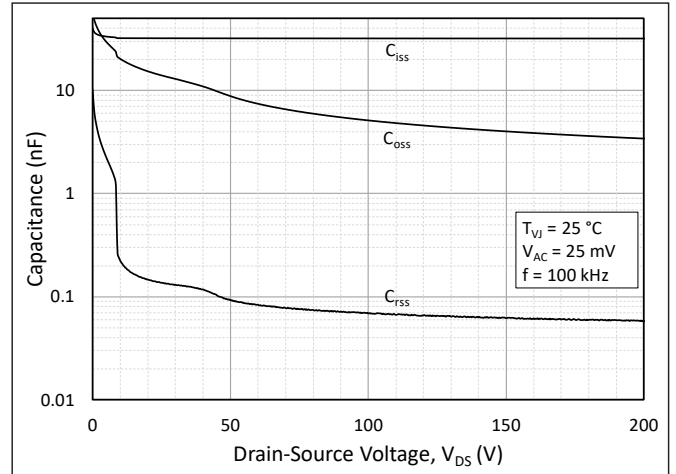


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

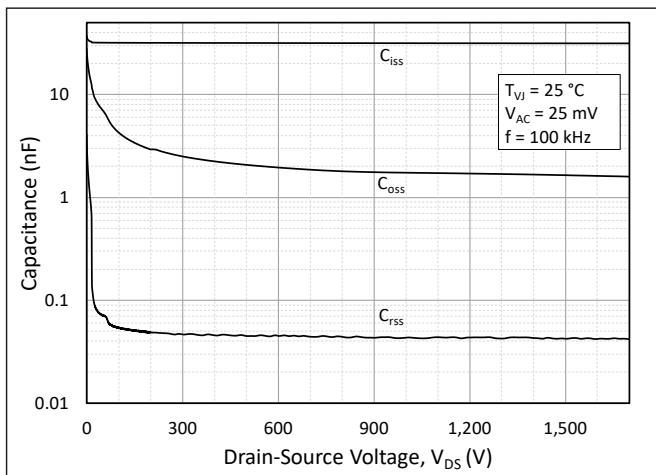


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1700V)

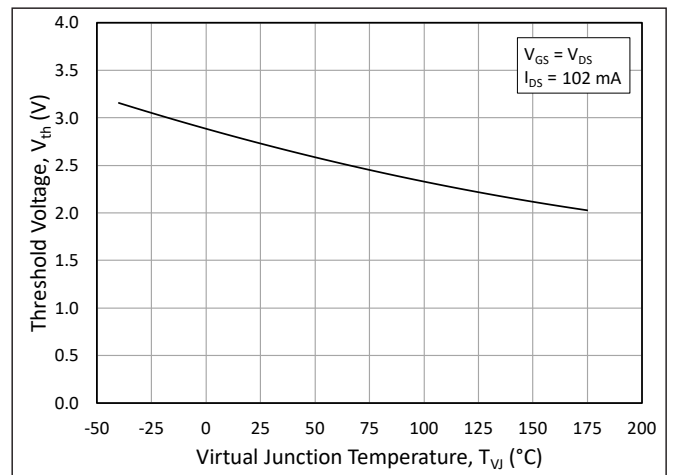


Figure 10. Threshold Voltage vs. Junction Temperature

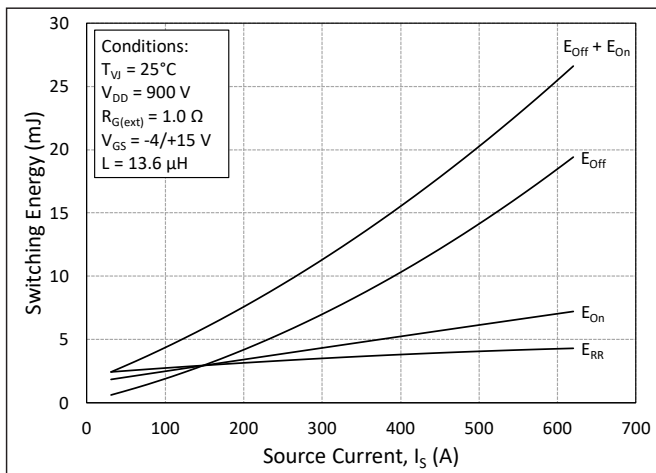


Figure 11. Switching Energy vs. Drain Current ($V_{DD} = 900$ V)

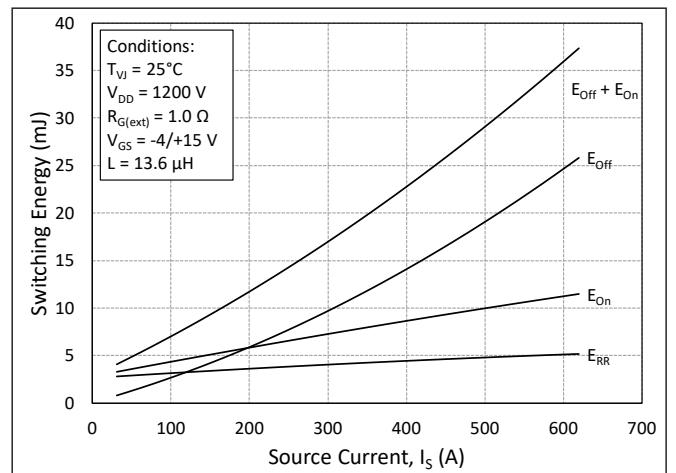


Figure 12. Switching Energy vs. Drain Current ($V_{DD} = 1200$ V)

Typical Performance

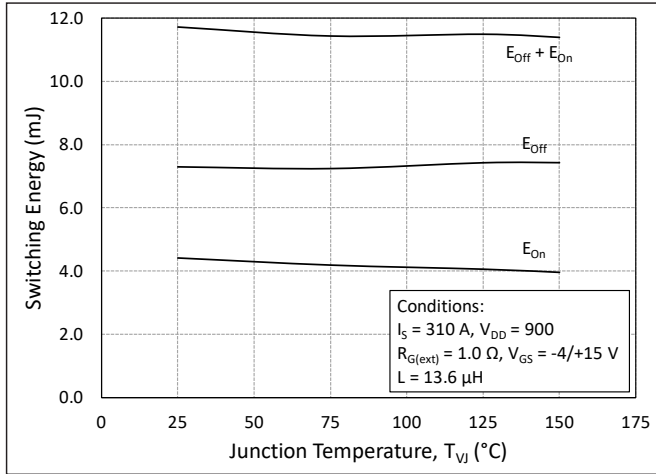


Figure 13. MOSFET Switching Energy vs. Junction Temperature

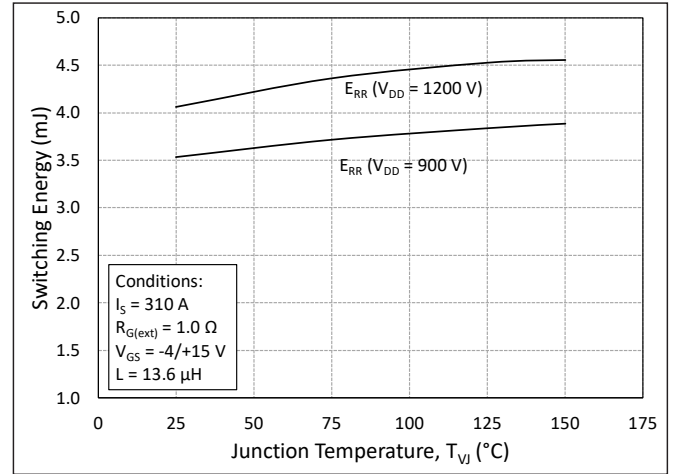


Figure 14. Reverse Recovery Energy vs. Junction Temperature

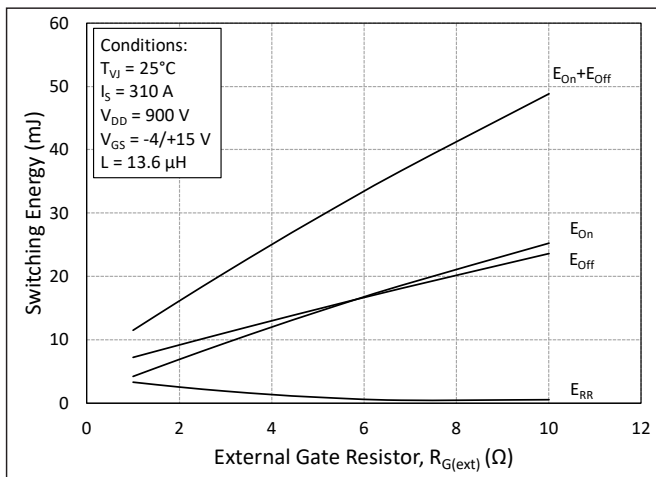


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

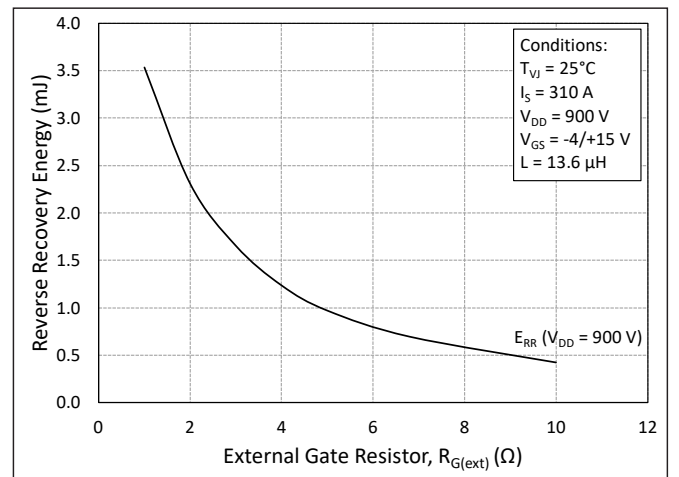


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

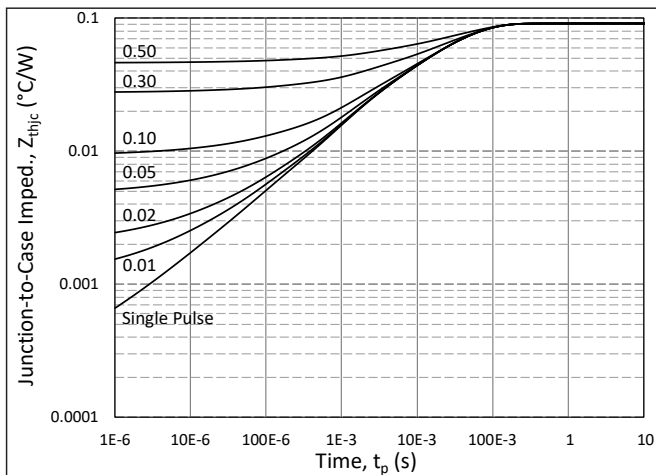


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, Z_{thjc} (°C/W)

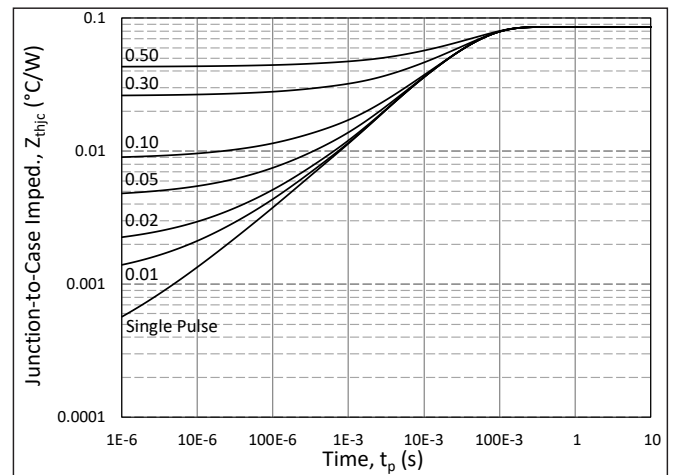


Figure 18. Diode Junction to Case Transient Thermal Impedance, Z_{thjc} (°C/W)



Typical Performance

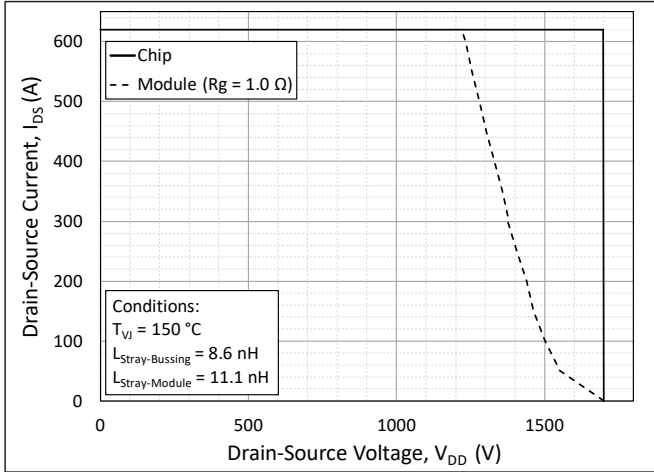


Figure 19. Switching Safe Operating Area

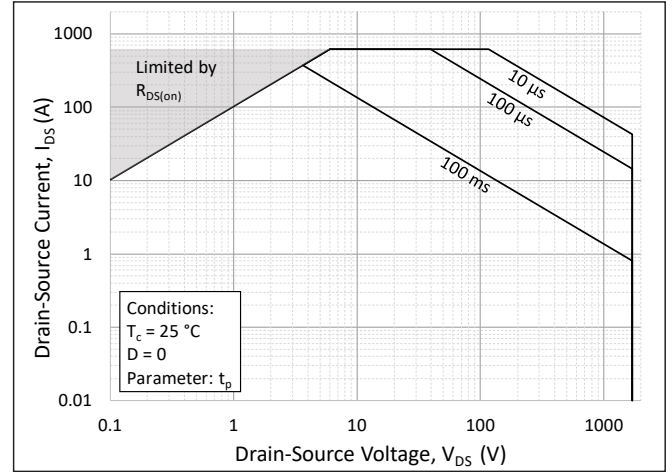


Figure 20. Forward Bias Safe Operating Area (FBSOA)

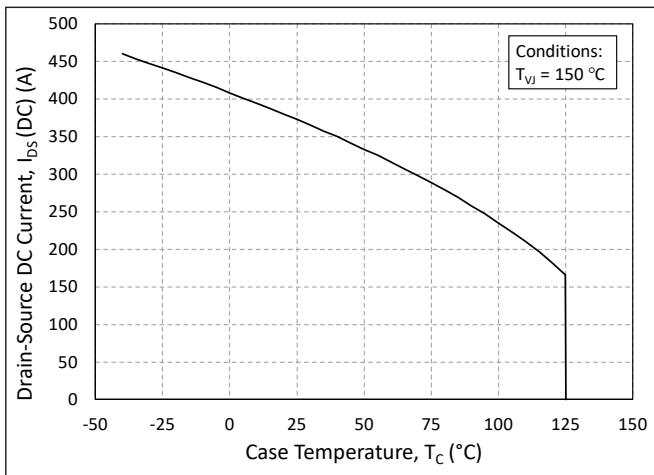


Figure 21. Continuous Drain Current Derating vs. Case Temperature

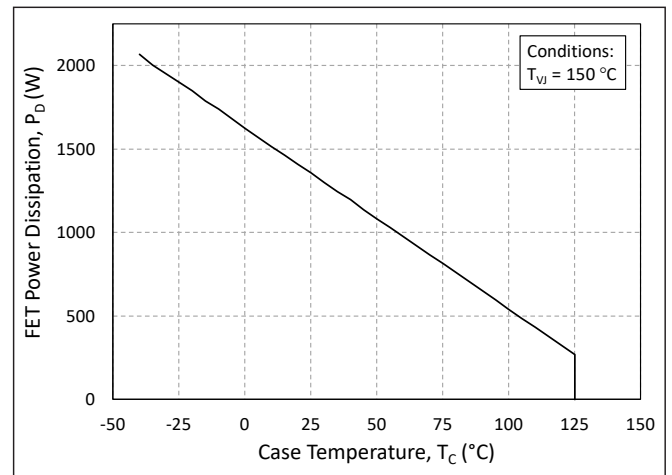


Figure 22. Maximum Power Dissipation Derating vs. Case Temperature

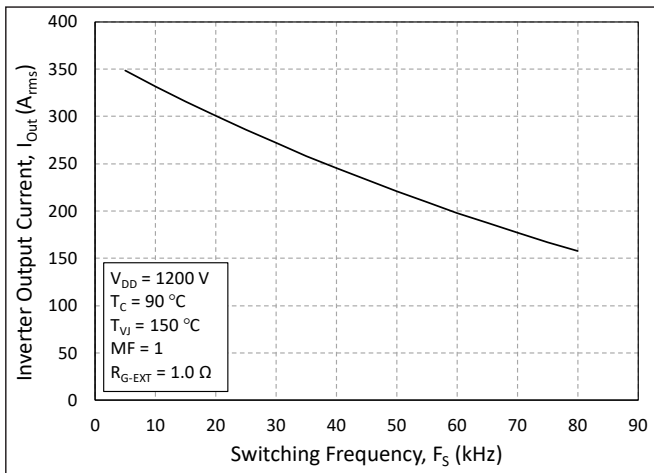


Figure 23. Typical Output Current Capability vs. Switching Frequency (Inverter Application)



Timing Characteristics

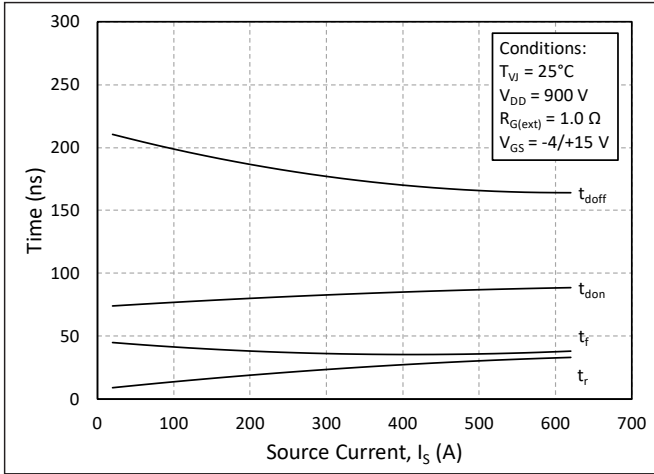


Figure 24. Timing vs. Source Current

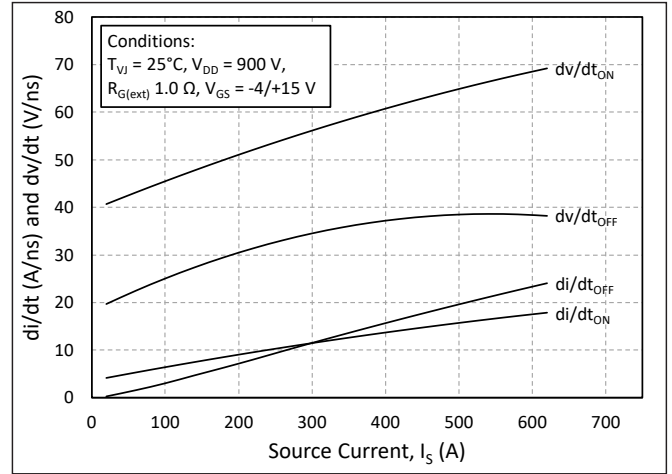


Figure 25. dv/dt and di/dt vs. Source Current

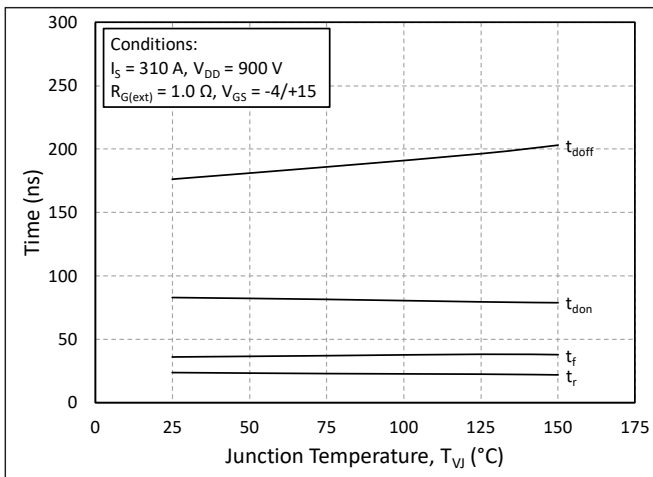


Figure 26. Timing vs. Junction Temperature

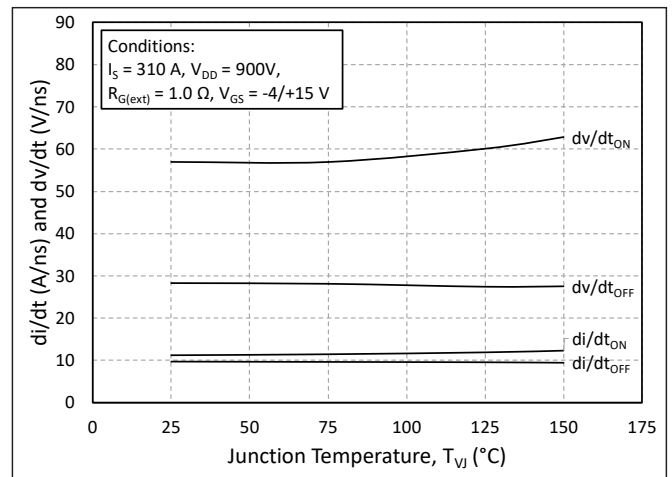


Figure 27. dv/dt and di/dt vs. Junction Temperature

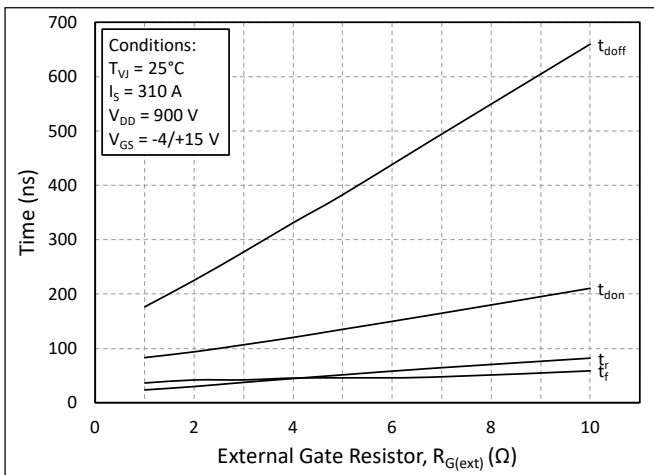


Figure 28. Timing vs. External Gate Resistance

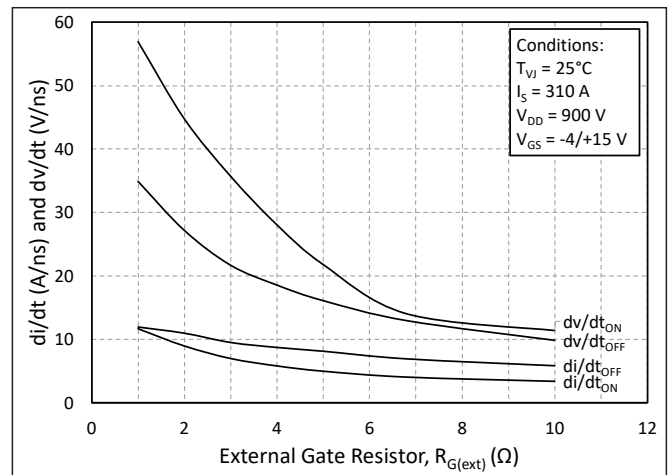


Figure 29. dv/dt and di/dt vs. External Gate Resistance



Definitions

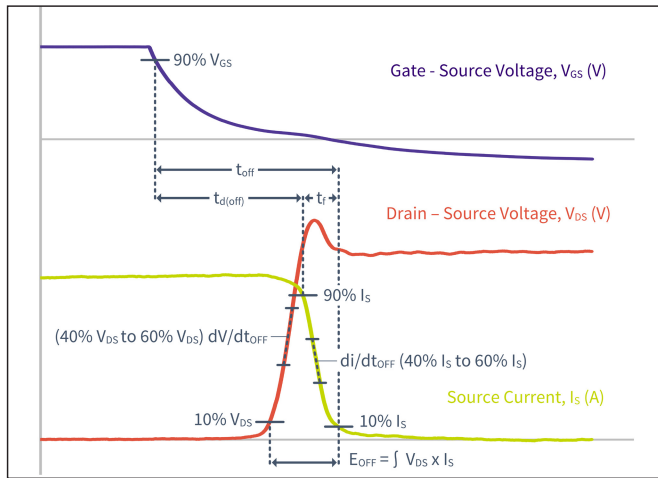


Figure 30. Turn-off Transient Definitions

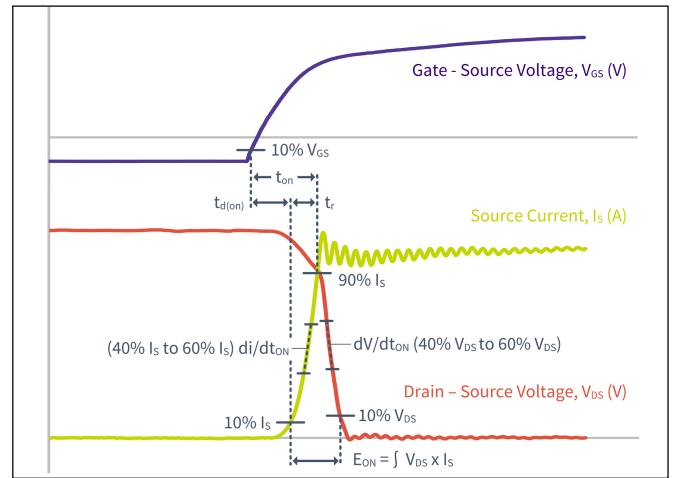


Figure 31. Turn-on Transient Definitions

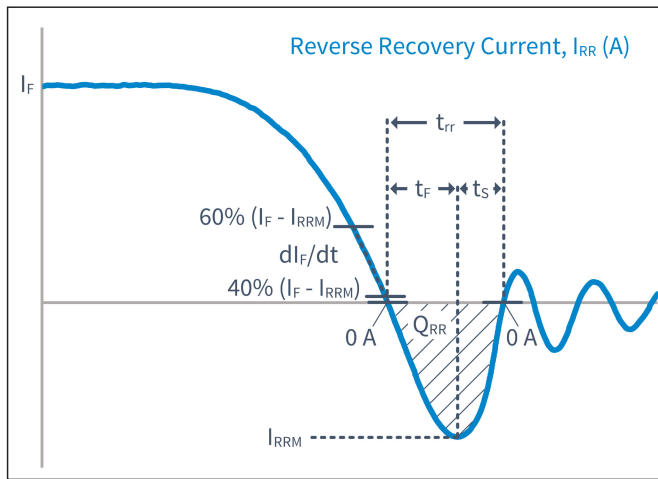


Figure 32. Reverse Recovery Definitions

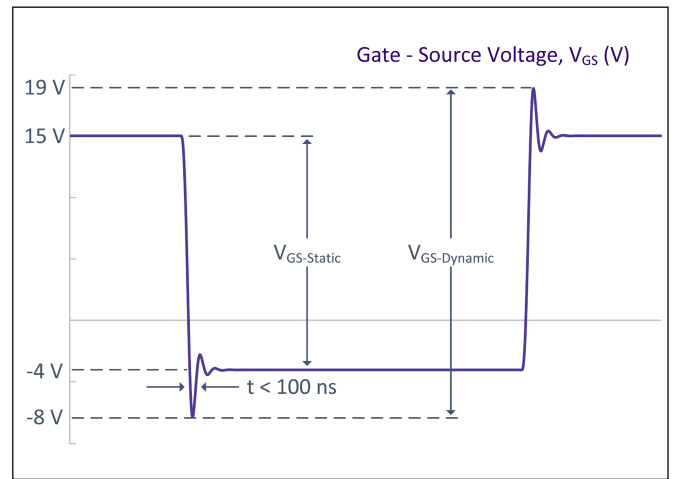
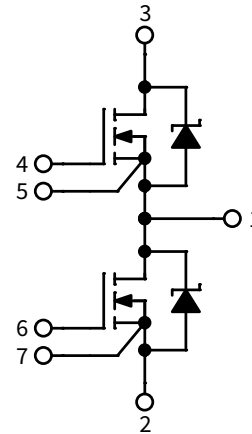
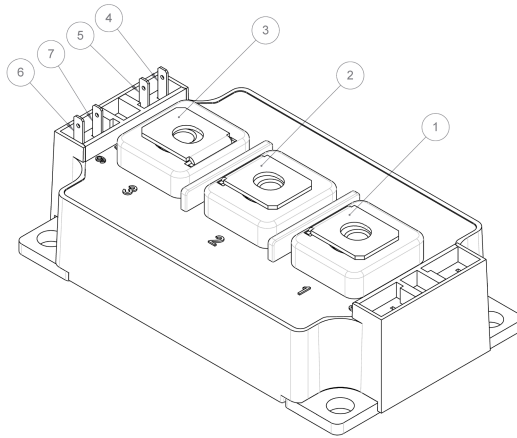


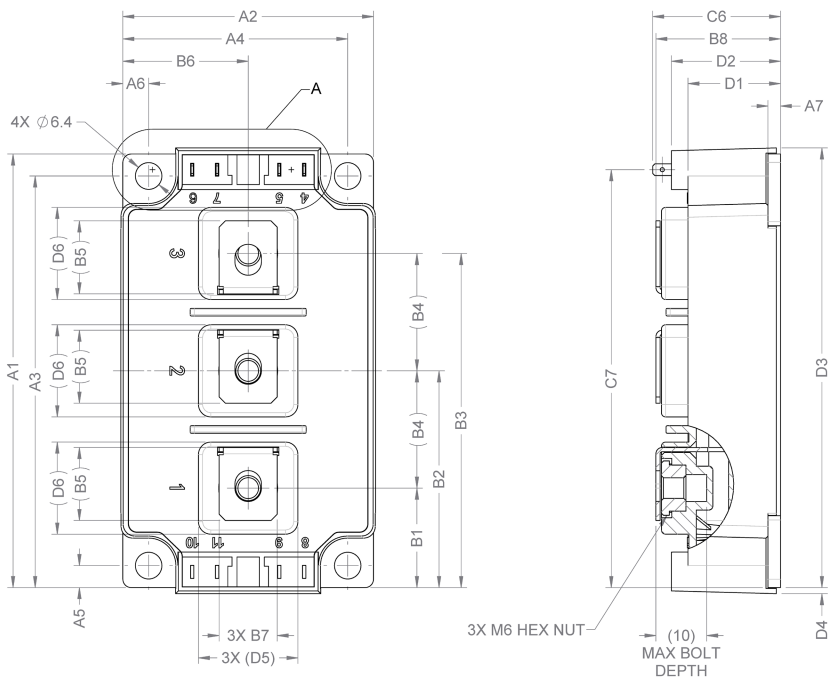
Figure 33. V_{GS} Transient Definitions



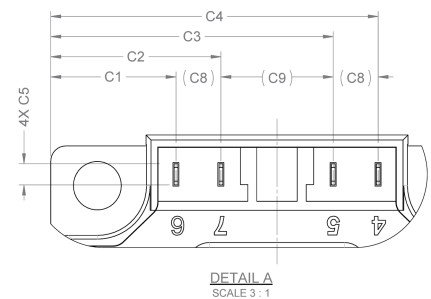
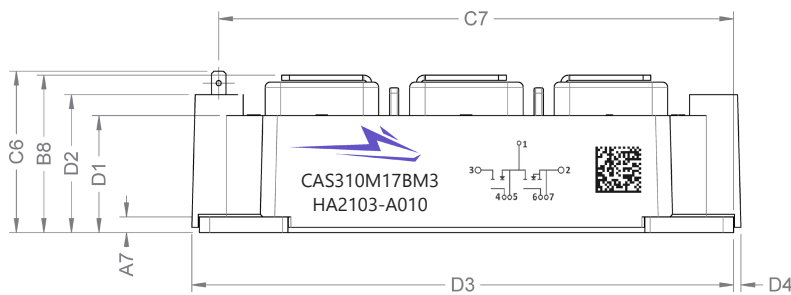
Schematic and Pin Out



Package Dimension (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	103.5	±0.30
A2	60.44	±0.30
A3	98.25	±0.30
A4	54.22	±0.30
A5	5.25	±0.30
A6	6.22	±0.30
A7	3	±0.30
B1	23.75	±0.40
B2	51.75	±0.40
B3	79.75	±0.40
B4	(28)	REF.
B5	(17.43)	REF.
B6	30.23	±0.40
B7	(14)	REF.
B8	30.03	±0.40
C1	16.73	±0.40
C2	22.73	±0.40
C3	37.73	±0.40
C4	43.73	±0.40
C5	2.8	±0.40
C6	30.8	±0.50
C7	99.75	±0.40
C8	(6)	REF.
C9	(15)	REF.
D1	22.3	±0.30
D2	26.3	±0.30
D3	104.95	±0.30
D4	1.45	±0.40
D5	(24)	REF.
D6	(22)	REF.





Supporting Links & Tools

Evaluation Tools & Support

- [SpeedFit 2.0 Design Simulator™](#)
- [Technical Support Forum](#)

Dual-Channel Gate Driver Board

- [CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers](#)

Application Notes

- [CPWR-AN35: 62mm Module Thermal Interface Material Application Note](#)
- [CPWR-AN34: 62mm Module Mounting Guide Application Note](#)
- [CPWRAN12: Understanding the Effects of Parasitic Inductance Part 1.](#)
- [CPWRAN13: Understanding the Effects of Parasitic Inductance Part 2.](#)



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