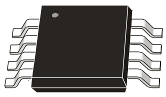
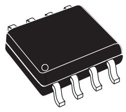
Very high accuracy (20 μV), zero-drift, rail-to-rail output, 3 MHz, 36 V op amp



MiniSO8



SO8

Maturity status link
TSB182

Related products	
TSB612	For lower current consumption
TSB622	For lower speed
TSB572	For rail-to-rail inputs
TSB712	For higher speed, precision, and rail-to-rail inputs

Features

- Very low offset voltage: 20 μV max. @ 25 °C
- Rail-to-rail output
- Wide supply voltage: 4 to 36 V
- Gain bandwidth product: 3 MHz
- Slew rate: 2 V/μs
- Low noise: 24 nV/√Hz
- EMI hardened
- High ESD tolerance: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- AEC-Q100 qualified

Applications

- Industrial
- Power supplies
- Automotive

Description

The TSB182 is a very high precision dual operational amplifier with a maximum guaranty of 20 μV on input offset voltage. It can operate over an extended supply voltage operating range and features rail-to-rail output. It offers an excellent speed/ power consumption ratio with 3 MHz gain bandwidth product while consuming 650 μA typically per operational amplifier on a large supply voltage range.

The TSB182 operates over a wide temperature range from -40 °C to 125 °C making this device ideal for industrial and automotive applications with the associated qualification.

Thanks to its small package size, the TSB182 can be used in applications where space on the board is limited. It can thus reduce the overall cost of the PCB.

1 Pin description

Figure 1. Pin connections (top view)

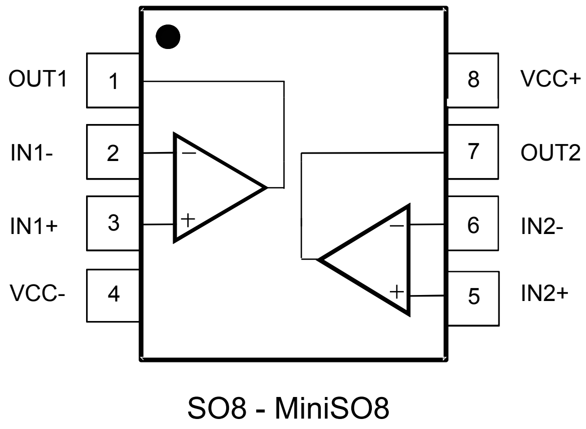


Table 1. Pin description

Pin	Pin name	Description
1	OUT1	Output
2	IN1 -	Negative input voltage
3	IN1 +	Positive input voltage
4	VCC -	Negative supply voltage
5	IN2 +	Positive input voltage
6	IN2 -	Negative input voltage
7	OUT2	Output
8	VCC +	Positive supply voltage

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
Vcc	Supply voltage [1]	40	V
Vid	Differential input voltage [2]	± 0.7	V
Vin	Input voltage	(Vcc-) -0.3 to (Vcc+) +0.3	V
Iin	Input current [3]	10	mA
Tstg	Storage temperature	-65 to 150	°C
Tj	Junction temperature	150	°C
Rth-ja	Thermal resistance junction-to-ambient [4] [5] SO8 MiniSO8	 125 190	°C/W
ESD	Human Body Model (HBM) [6]	4000	V
	Machine Model (MM) [7]	200	
	Charged Device Model (CDM) [8]	1500	

1. *All voltage values, except differential voltage, are with respect to network ground terminal.*
2. *The differential voltage is the difference between inverting and non-inverting terminal voltage.*
3. *Input current must be limited by a resistor in series with the inputs.*
4. *Rth are typical values.*
5. *Short-circuits can cause excessive heating and destructive dissipation.*
6. *According to JEDEC standard JESD22-A114F.*
7. *According to JEDEC standard JESD22-A115A.*
8. *According to ANSI/ESD STM 5.3.1.*

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
Vcc	Supply voltage	4 to 36	V
Vicm	Common mode voltage on input pins	(Vcc-) to (Vcc+) -2	V
T	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 4. Electrical characteristics V_{CC} = 5 V, V_{icm} = V_{CC}/2, R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		DC performance				
V_{IO}	Input offset voltage	V_{icm} = V_{CC}/2				µV
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
		V_{icm} = 0 V				
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		30	100	nV/°C
I_{IB}	Input bias current	T = 25 °C			400	pA
		Tmin < T < Tmax			400	
I_{IO}	Input offset current	T = 25 °C			600	
		Tmin < T < Tmax			600	
CMR	Common mode rejection ratio	V_{icm} = 0 to V_{CC} -2 V, V_{out} = V_{CC}/2	105	130		dB
		Tmin < T < Tmax	97			
Avd	Large signal voltage gain	V_{OUT} = 0.5 to (V_{CC} -0.5 V)	105	130		dB
		Tmin < T < Tmax	96			
V_{OL}	Output swing from negative rail	T = 25 °C		30	50	mV
		Tmin < T < Tmax			80	
V_{OH}	Output swing from positive rail	T = 25 °C		20	40	
		Tmin < T < Tmax			60	
I_{OUT}	Isink	V_{OUT} = V_{OL}				mA
		T = 25 °C	20	27		
		Tmin < T < Tmax	10			
	Isource	V_{OUT} = V_{OH}				
		T = 25 °C	20	29		
		Tmin < T < Tmax	10			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		650	850	µA
		Tmin < T < Tmax			900	
		AC performance				
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.8	3		MHz
		Tmin < T < Tmax	1.6			
SR	Slew rate	T = 25 °C	0.85	2		V/µs
		Tmin < T < Tmax	0.75			
Φm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		58		°
Gm	Gain margin			15		dB
En	Equivalent input noise voltage	f = 1 kHz		27		nV/√Hz
		0.1 to 10 Hz		700		nVpp

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
THD+N	Total harmonic distortion + noise	f = 1 kHz, G = 1, V_{OUT} = 1 Vpp		0.005		%
Cs	Channel separation	f = 1 kHz		130		dB
trec	Overload recovery time	G = -10		2		µs
Ts	Settling time	0.1% to final value, G = 1, 1 V step		18		µs
Cload	Capacitive load drive	No sustained oscillation		1		nF

Table 5. Electrical characteristics V_{CC} = 12 V, V_{icm} = V_{CC}/2, R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	V_{icm} = V_{CC}/2				µV
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
		V_{icm} = 0 V				
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		25	100	nV/°C
I_{IB}	Input bias current	T = 25 °C			400	pA
		Tmin < T < Tmax			400	
I_{IO}	Input offset current	T = 25 °C			600	
		Tmin < T < Tmax			600	
CMR	Common mode rejection ratio	V_{icm} = 0 to V_{CC} - 2 V, V_{OUT} = V_{CC}/2	116	140		dB
		Tmin < T < Tmax	107			
Avd	Large signal voltage gain	V_{OUT} = 0.5 to (V_{CC} - 0.5 V)	113	135		dB
		Tmin < T < Tmax	106			
V_{OL}	Output swing from negative rail	T = 25 °C		60	90	mV
		Tmin < T < Tmax			120	
V_{OH}	Output swing from positive rail	T = 25 °C		40	70	
		Tmin < T < Tmax			90	
I_{OUT}	Isink	V_{OUT} = V_{OL}				mA
		T = 25 °C	20	26		
		Tmin < T < Tmax	10			
	Isource	V_{OUT} = V_{OH}				
		T = 25 °C	20	29		
		Tmin < T < Tmax	10			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		650	850	µA
		Tmin < T < Tmax			900	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.8	3		MHz
		Tmin < T < Tmax	1.6			
SR	Slew rate	T = 25 °C	0.8	1.8		V/µs
		Tmin < T < Tmax	0.75			
Φm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		55		°
Gm	Gain margin			12		dB
En	Equivalent input noise voltage	f = 1 kHz		25		nV/√Hz
		0.1 to 10 Hz		650		nVpp
THD+N	Total harmonic distortion + noise	f = 1 kHz, Gain = 1, V_{OUT} = 1 Vpp		0.004		%
Cs	Channel separation	f = 1 kHz		130		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time	G = -10		1		µs
T_s	Settling time	0.1% to final value, G = 1, 10 V step		7		µs
C_{load}	Capacitive load drive	No sustained oscillation		1		nF

Table 6. Electrical characteristics V_{CC} = 36 V, V_{icm} = V_{CC}/2, R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	V_{icm} = V_{CC}/2				µV
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
		Vicm = 0 V				
		T = 25 °C	-20		+20	
		Tmin < T < Tmax	-30		+30	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		20	100	nV/°C
I_{IB}	Input bias current	T = 25 °C			500	pA
		Tmin < T < Tmax			500	
I_{IO}	Input offset current	T = 25 °C			800	
		Tmin < T < Tmax			800	
CMR	Common mode rejection ratio	V_{icm} = 0 to V_{CC} -2 V, V_{OUT} = V_{CC}/2	127	150		dB
		Tmin < T < Tmax	120			
SVR	Supply voltage rejection ratio	V_{CC} = 4 to 36 V	127	138		dB
		Tmin < T < Tmax	120			
Avd	Large signal voltage gain	V_{OUT} = 0.5 to (V_{CC} -0.5 V)	124	145		dB
		Tmin < T < Tmax	115			
V_{OL}	Output swing from negative rail	T = 25 °C		140	200	mV
		Tmin < T < Tmax			270	
V_{OH}	Output swing from positive rail	T = 25 °C		130	200	
		Tmin < T < Tmax			300	
I_{OUT}	Isink	V_{OUT} = V_{OL}				mA
		T = 25 °C	20	24		
		Tmin < T < Tmax	12			
	Isource	V_{OUT} = V_{OH}				
		T = 25 °C	20	27		
		Tmin < T < Tmax	12			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		670	850	µA
		Tmin < T < Tmax			900	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.8	3		MHz
		Tmin < T < Tmax	1.8			
SR	Slew rate	T = 25 °C	0.8	1.7		V/µs
		Tmin < T < Tmax	0.6			
Φm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		54		°
Gm	Gain margin			11		dB
En	Equivalent input noise voltage	f = 1 kHz		24		nV/√Hz
		0.1 to 10 Hz		620		nVpp

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
THD+N	Total harmonic distortion + noise	f = 1 kHz, G = 1, V_{OUT} = 2 Vpp		0.002		%
C_s	Channel separation	f = 1 kHz		130		dB
t_{rec}	Overload recovery time	G = -10		1		µs
T_s	Settling time	0.1% to final value, G = 1, 10 V step		7		µs
C_{load}	Capacitive load drive	No sustained oscillation		1		nF

4 Typical performance characteristics

Figure 2. Input offset voltage distribution at V_{CC} = 5 V

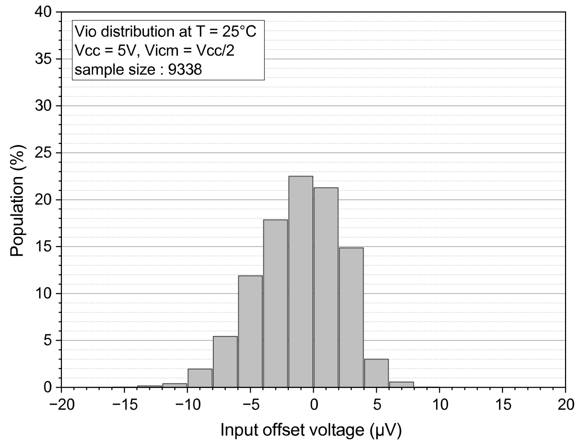


Figure 3. Input offset voltage distribution at V_{CC} = 12 V

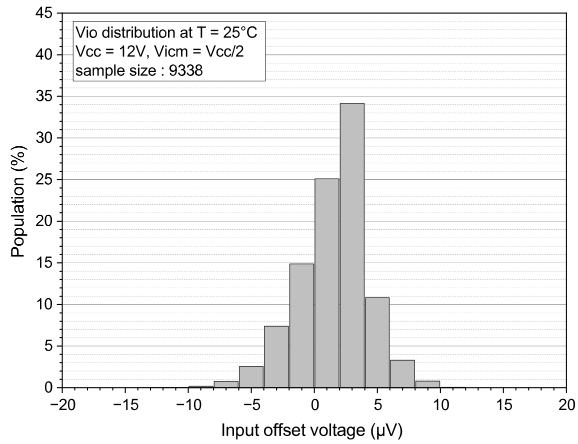


Figure 4. Input offset voltage distribution at V_{CC} = 36 V and V_{icm} = 0 V

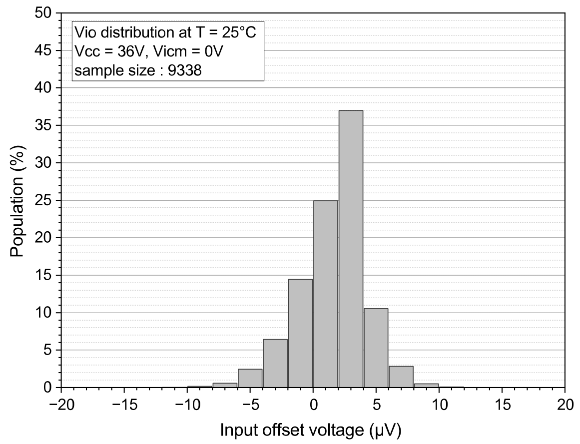


Figure 5. Input offset voltage distribution at V_{CC} = 36 V and V_{icm} = $V_{CC}/2$

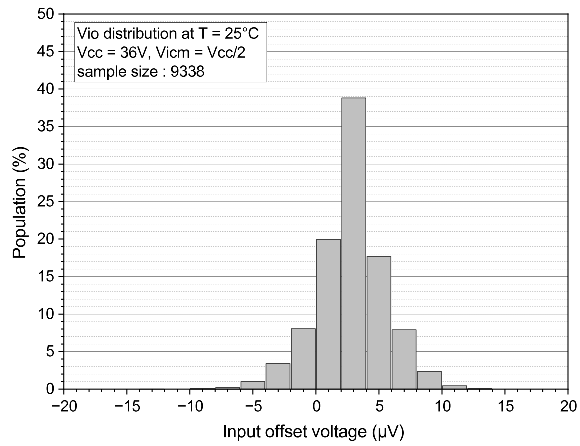


Figure 6. Input offset voltage vs. input common mode voltage at V_{CC} = 5 V

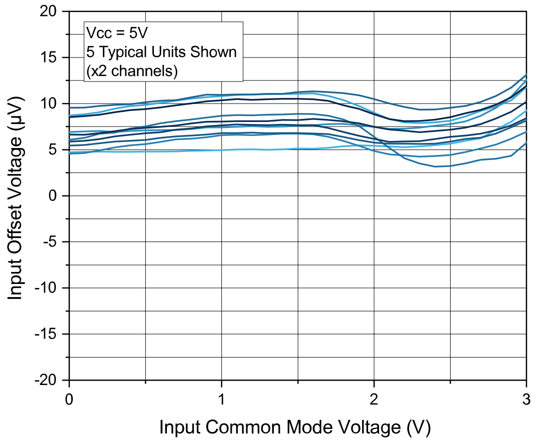


Figure 7. Input offset voltage vs. input common mode voltage at V_{CC} = 12 V

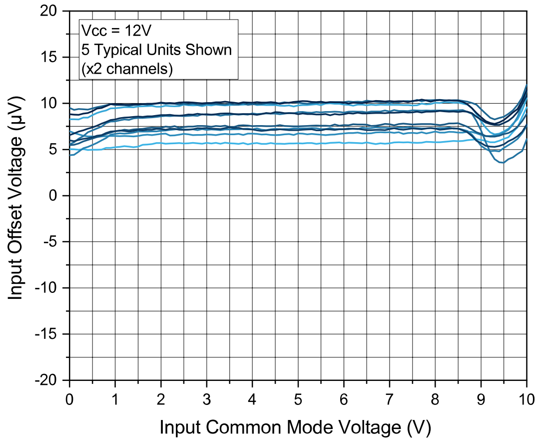


Figure 8. Input offset voltage vs. input common mode voltage at V_{CC} = 36 V

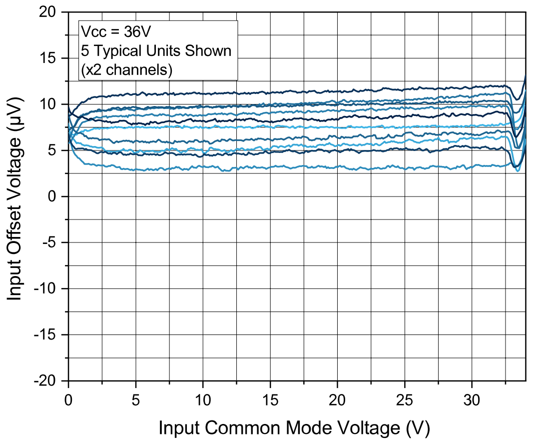


Figure 9. Input offset voltage vs. supply voltage

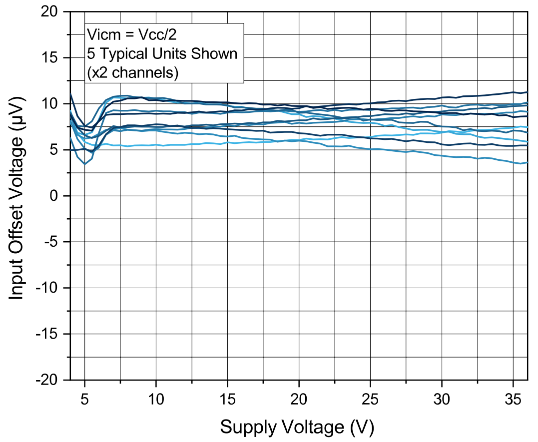


Figure 10. Input offset voltage vs. temperature

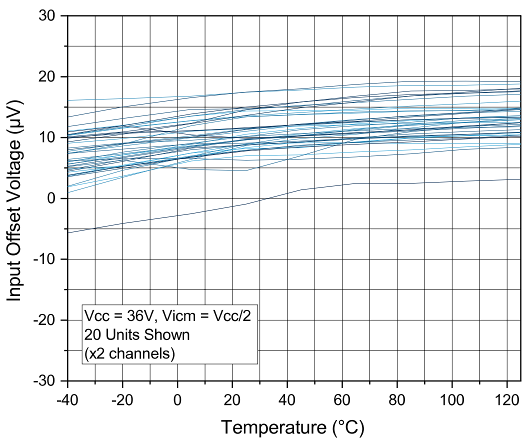


Figure 11. Input offset drift distribution

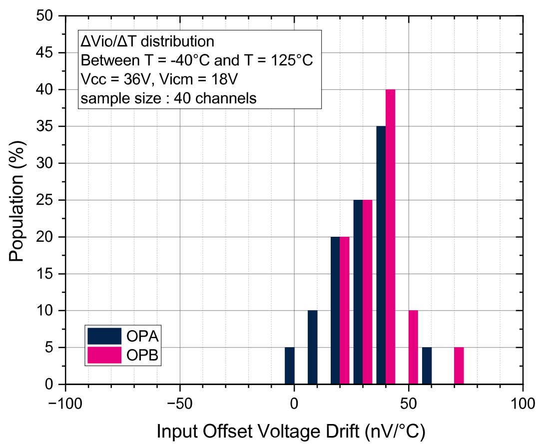


Figure 12. Supply current vs. input common mode voltage at V_{CC} = 5 V

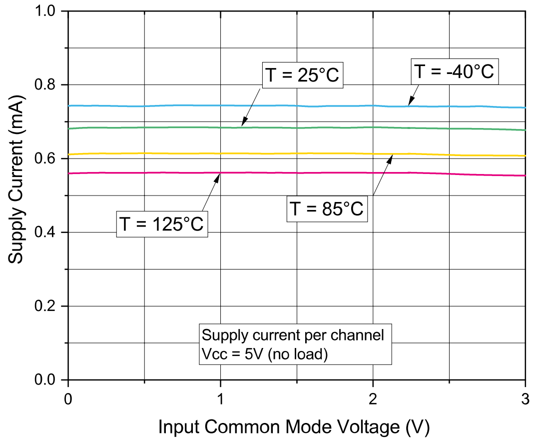


Figure 13. Supply current vs. input common mode voltage at V_{CC} = 12 V

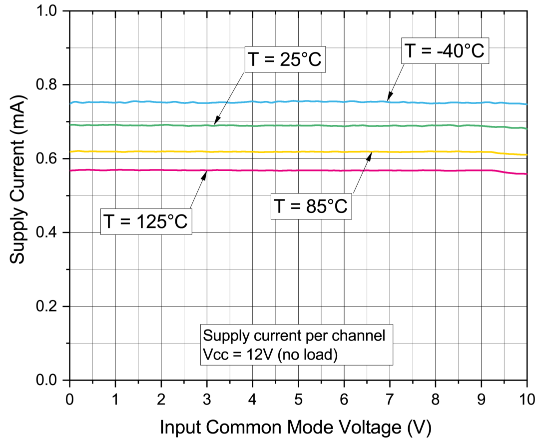


Figure 14. Supply current vs. input common mode voltage at V_{CC} = 36 V

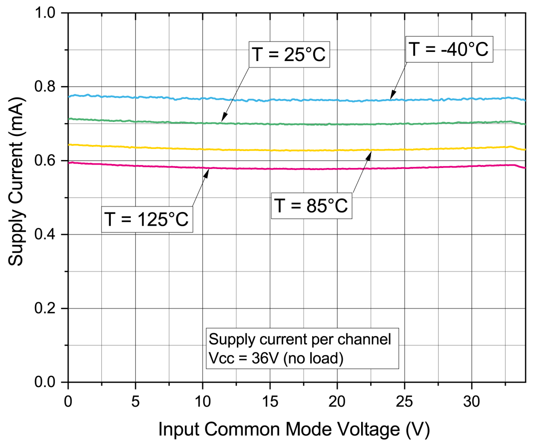


Figure 15. Supply current vs. supply voltage

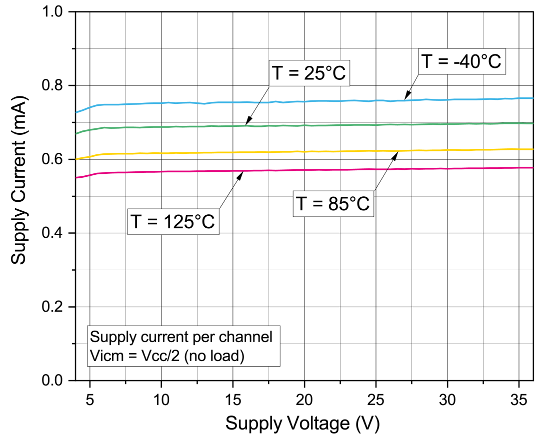


Figure 16. Input bias current vs. input common mode voltage at V_{CC} = 5 V

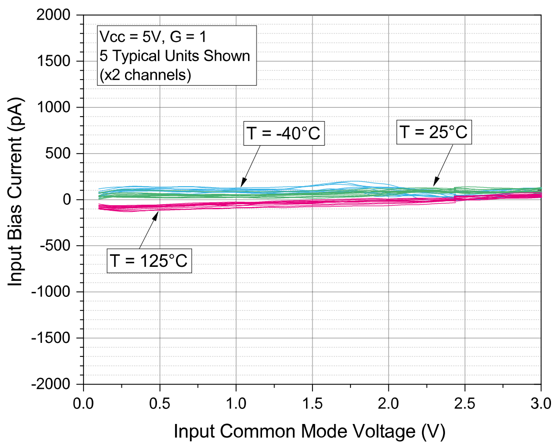


Figure 17. Input bias current vs. input common mode voltage at V_{CC} = 12 V

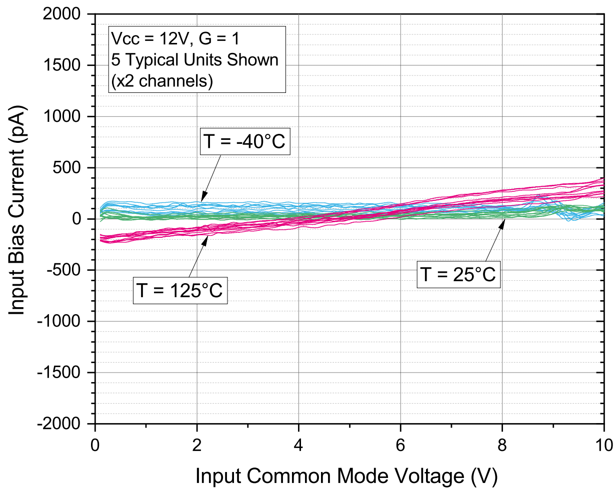


Figure 18. Input bias current vs. input common mode voltage at V_{CC} = 36 V

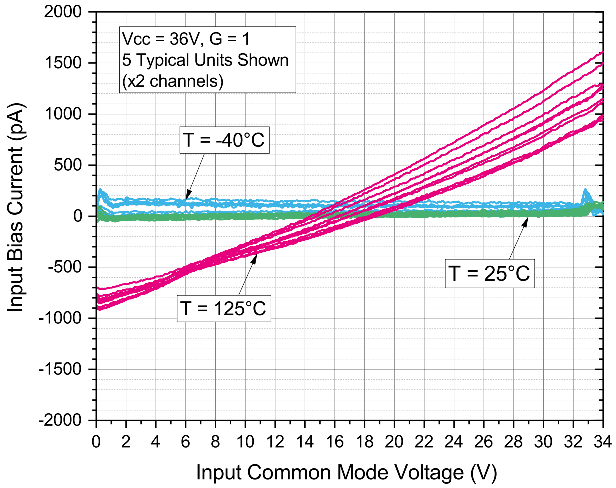


Figure 19. Output current vs. output voltage at V_{CC} = 5 V

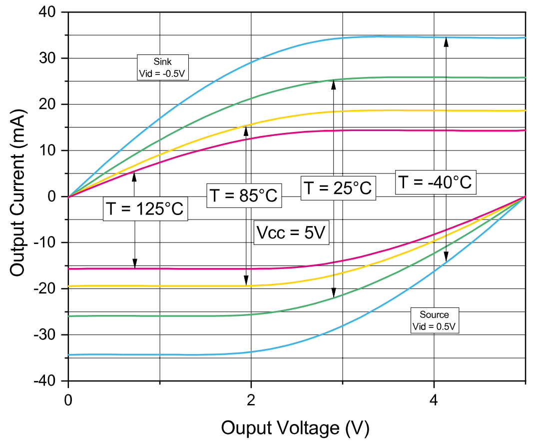


Figure 20. Output current vs. output voltage at V_{CC} = 12 V

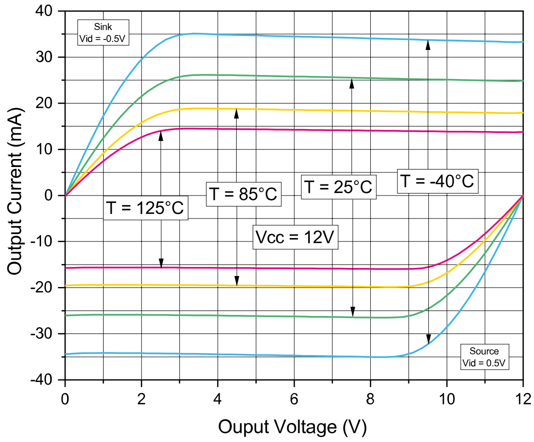


Figure 21. Output current vs. output voltage at V_{CC} = 36 V

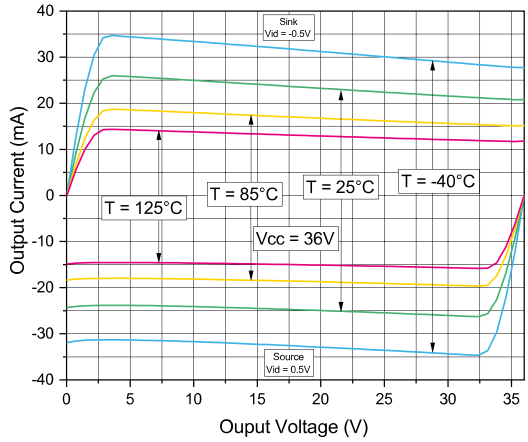


Figure 22. Output linearity at V_{CC} = 36 V

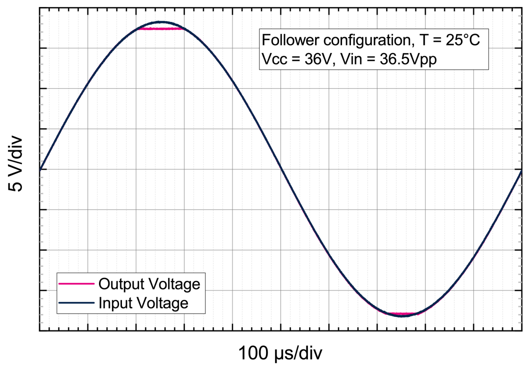


Figure 23. CMRR and PSRR vs. frequency at V_{CC} = 5 V

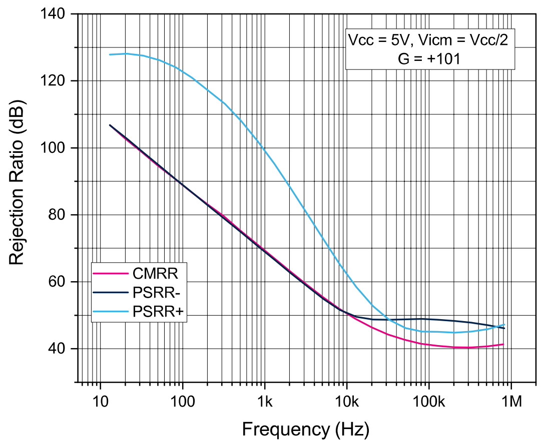


Figure 24. CMRR and PSRR vs. frequency at V_{CC} = 12 V

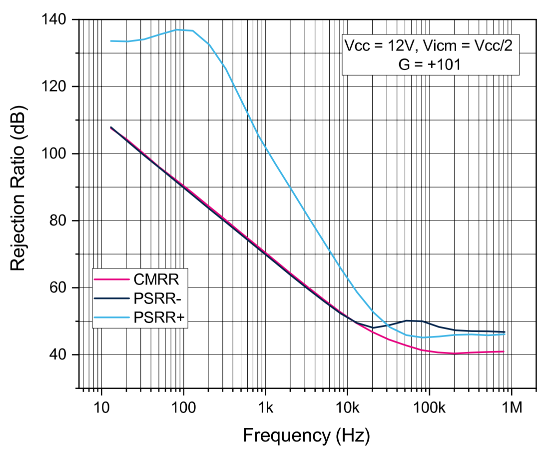


Figure 25. CMRR and PSRR vs. frequency at V_{CC} = 36 V

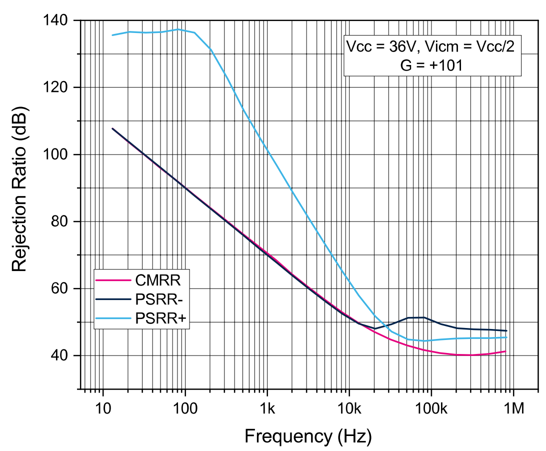


Figure 26. Bode plot at V_{CC} = 5 V

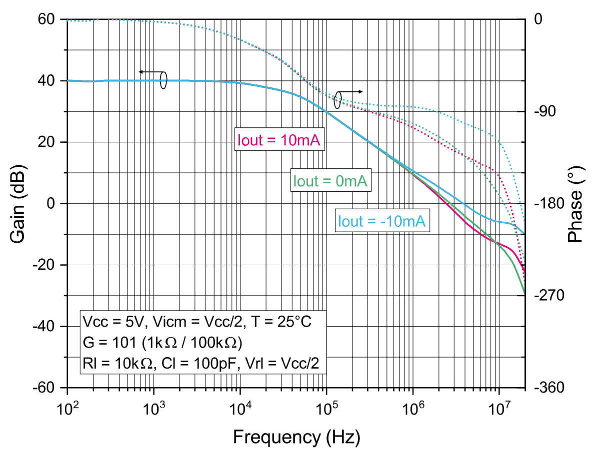


Figure 27. Bode plot at V_{CC} = 36 V

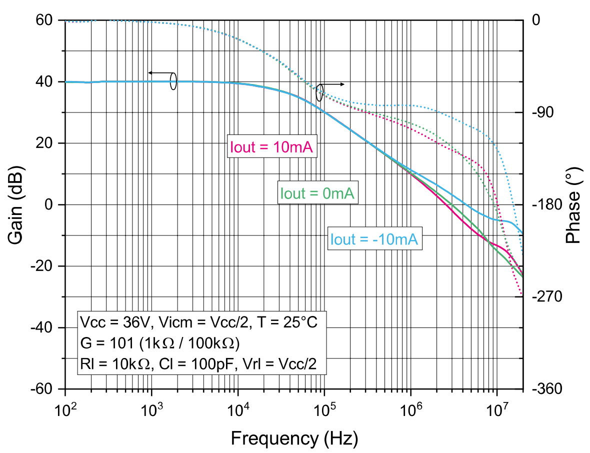


Figure 28. Slew rate vs. input common mode voltage at V_{CC} = 5 V

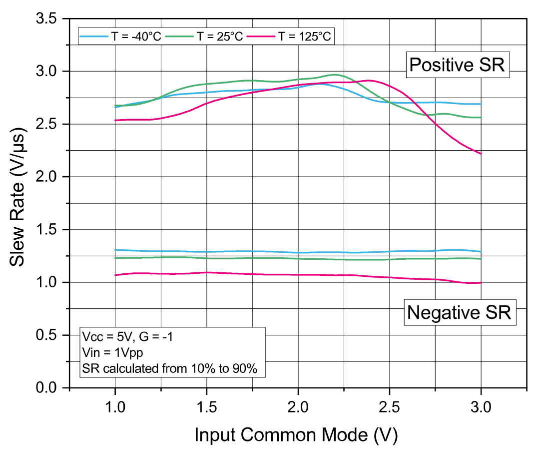


Figure 29. Slew rate vs. input common mode voltage at V_{CC} = 36 V

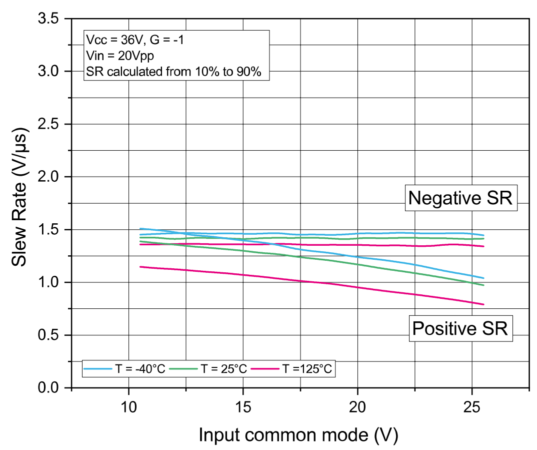


Figure 30. Output voltage vs. input voltage at V_{CC} = 5 V

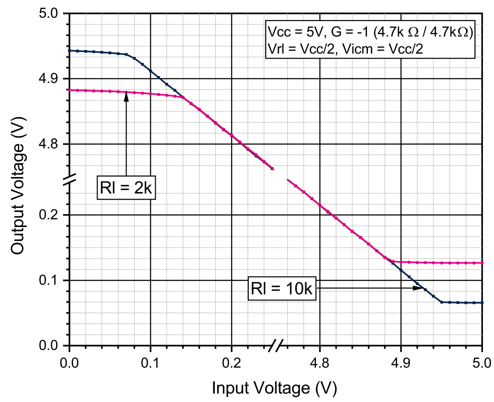


Figure 31. Output voltage vs. input voltage at V_{CC} = 36 V

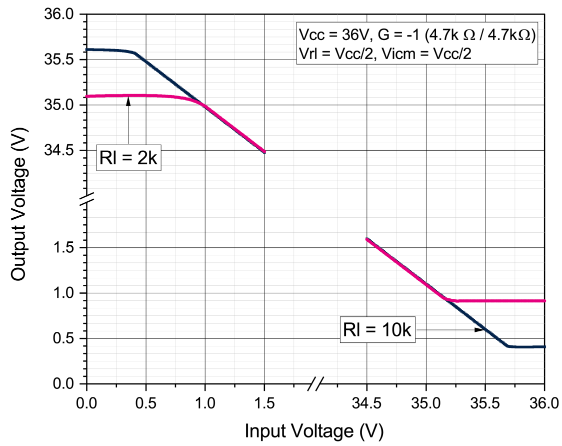


Figure 32. Output drop voltage V_{OH} vs. supply voltage

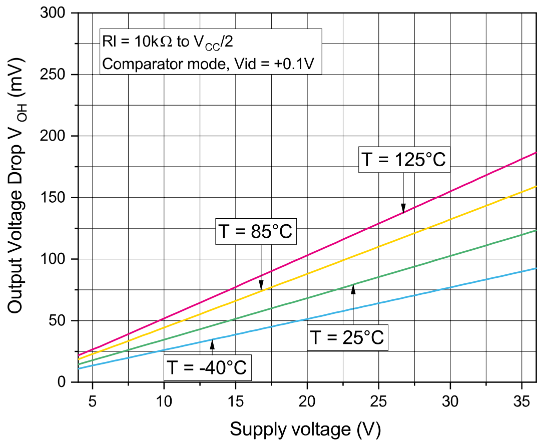


Figure 33. Output drop voltage V_{OL} vs. supply voltage

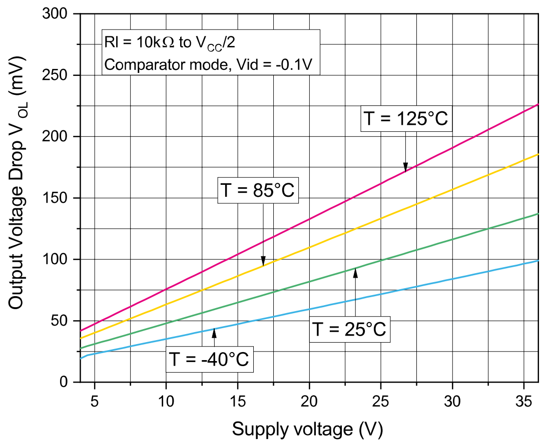


Figure 34. Noise vs. time at V_{CC} = 36 V

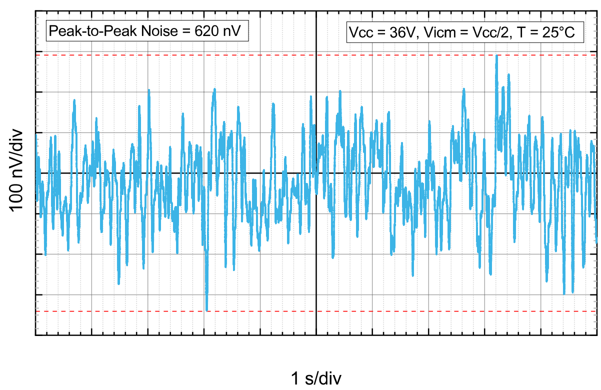


Figure 35. Voltage noise density vs. frequency

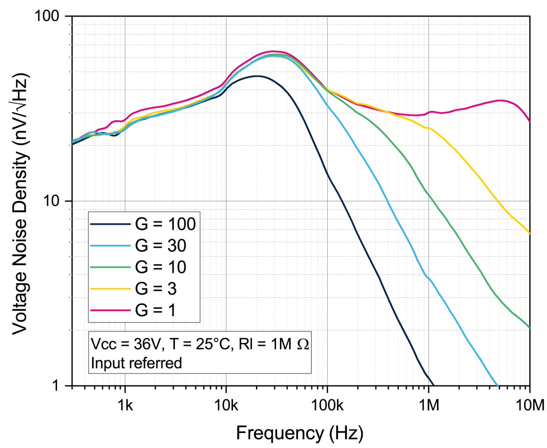


Figure 36. Small signal response at V_{CC} = 36 V

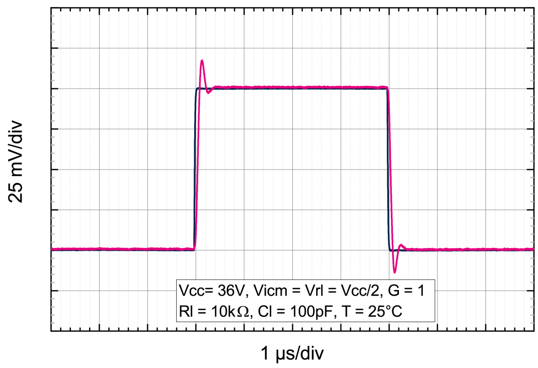


Figure 37. Large signal response at V_{CC} = 36 V

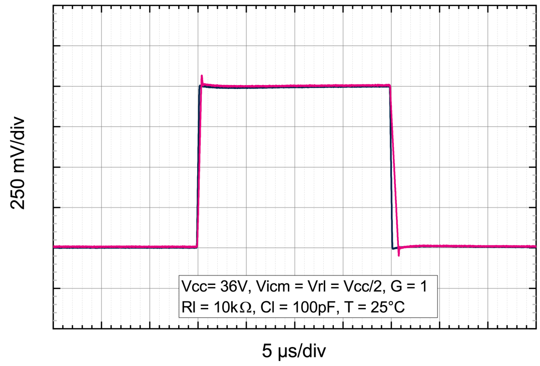


Figure 38. Settling time on negative input step

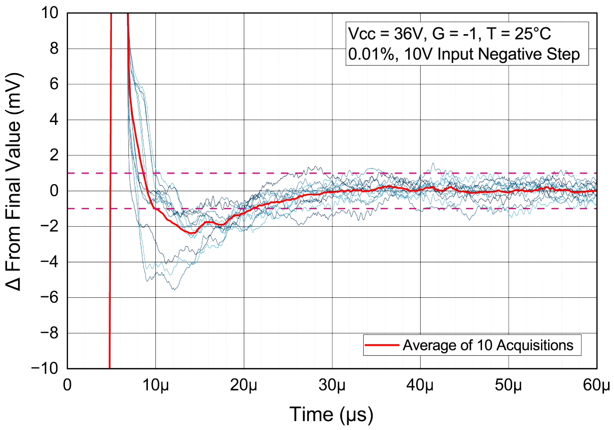


Figure 39. Settling time on positive input step

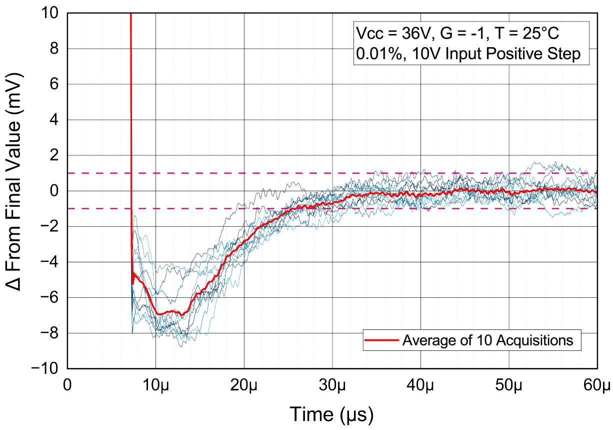


Figure 40. Small step overshoot vs. load capacitance

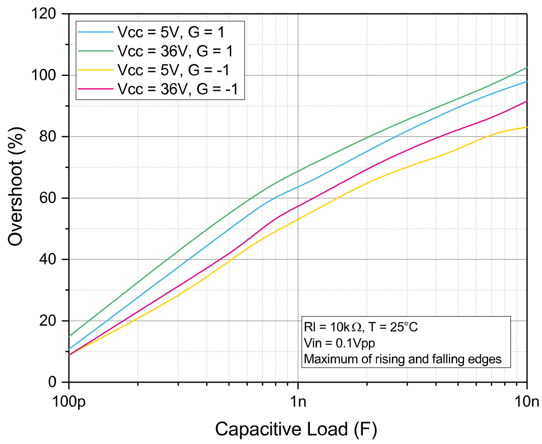
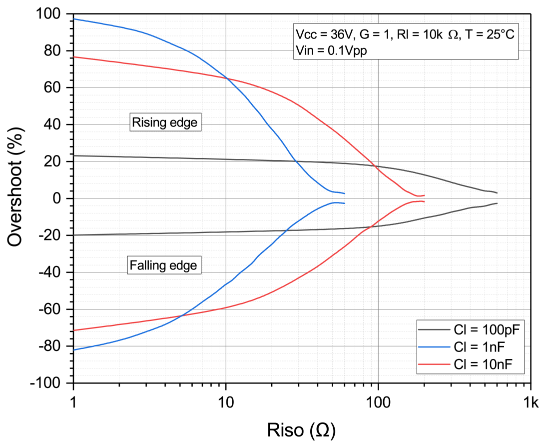


Figure 41. Small step overshoot vs. R_{iso}



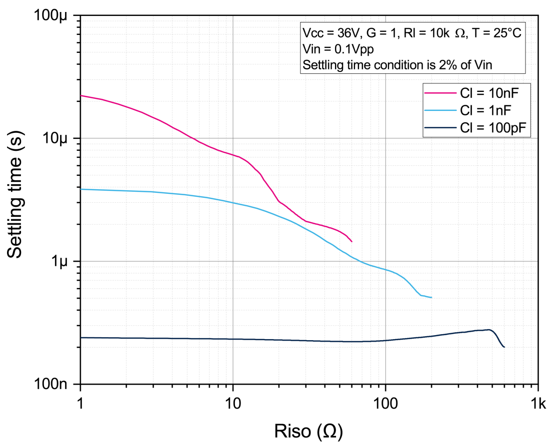


Figure 42. Settling time vs. R_{iso}

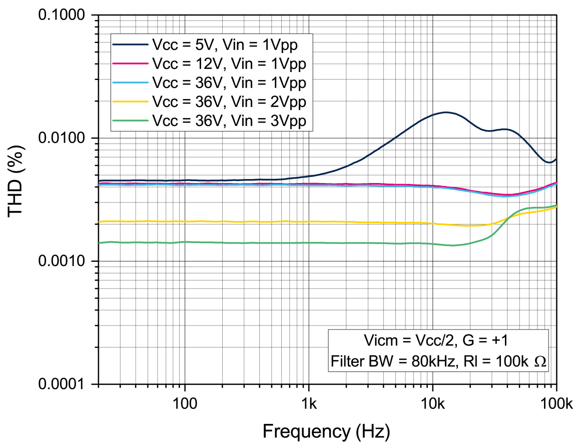


Figure 43. THD vs. frequency

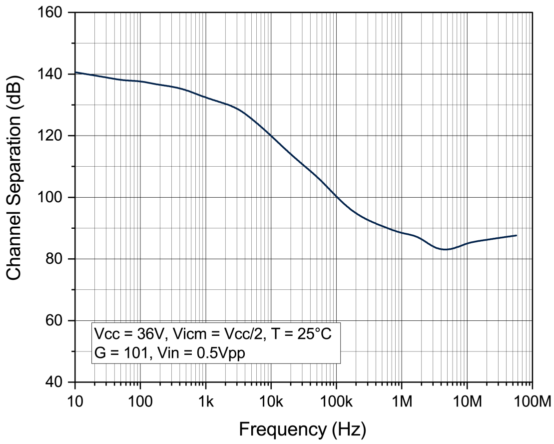


Figure 44. Channel separation vs. frequency

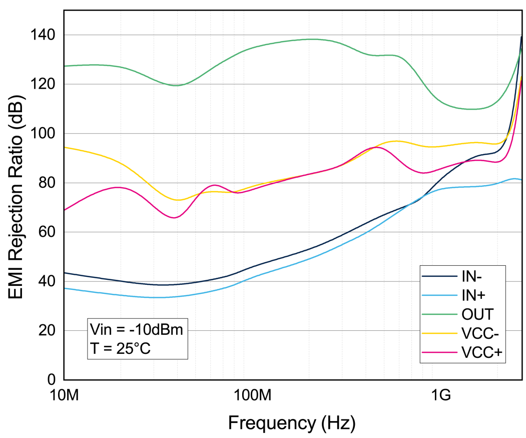


Figure 45. EMI rejection vs. frequency

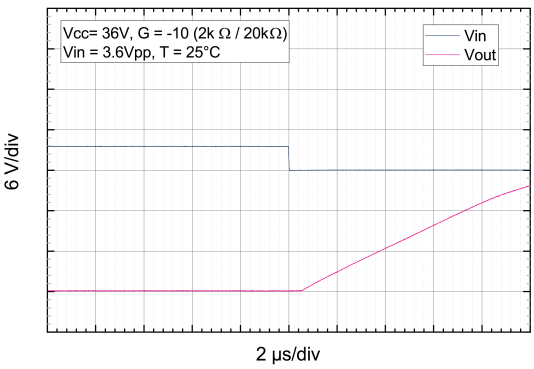


Figure 46. Positive overvoltage recovery

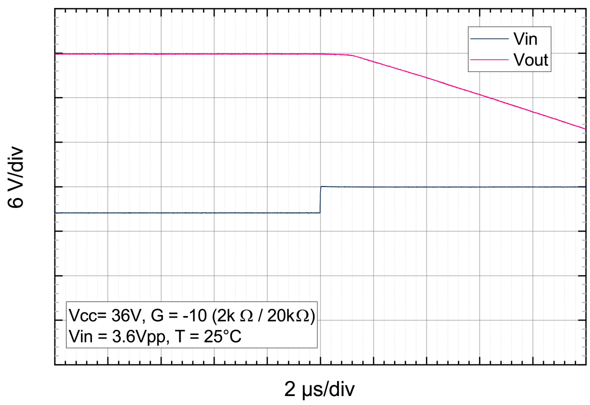
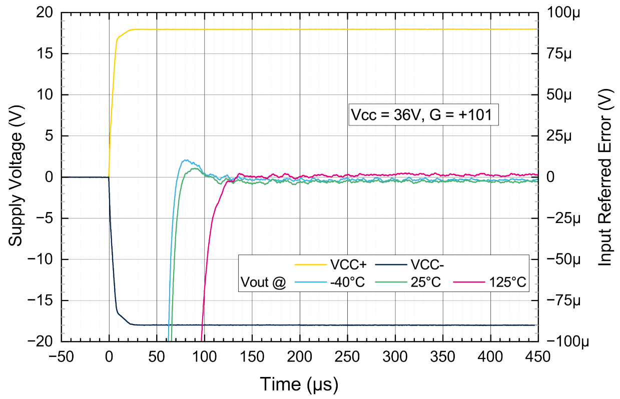


Figure 47. Negative overvoltage recovery

Figure 48. Startup behavior at V_{CC} = 36 V



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 SO8 package information

Figure 49. SO8 package outline

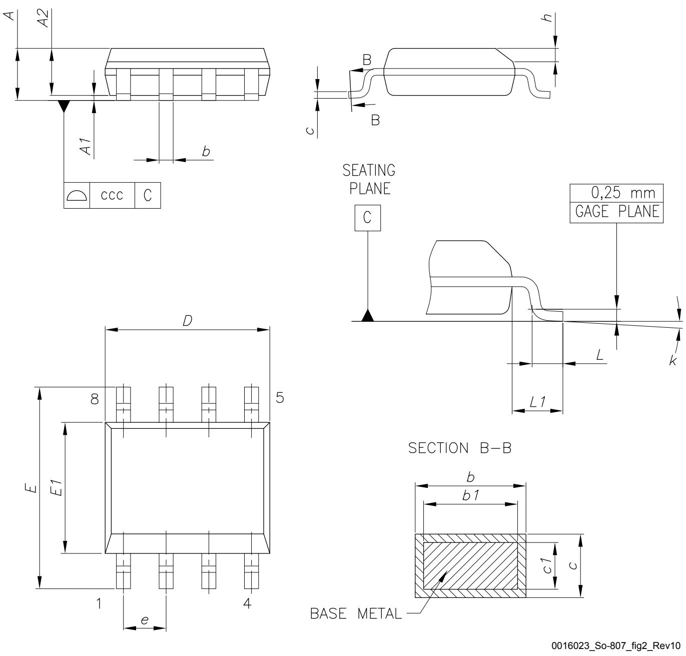
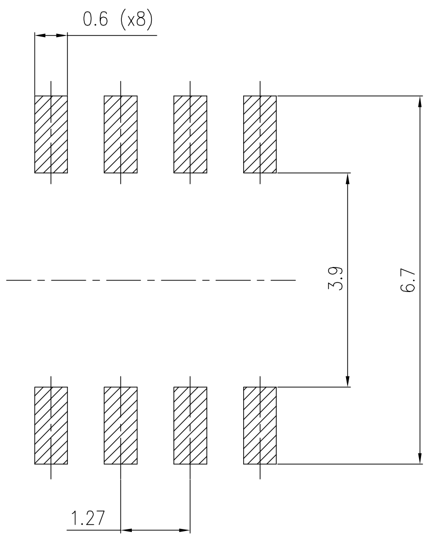


Table 7. SO8 package mechanical data

Dim	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 50. SO8 recommended footprint



5.2 MiniSO8 package information

Figure 51. MiniSO8 package outline

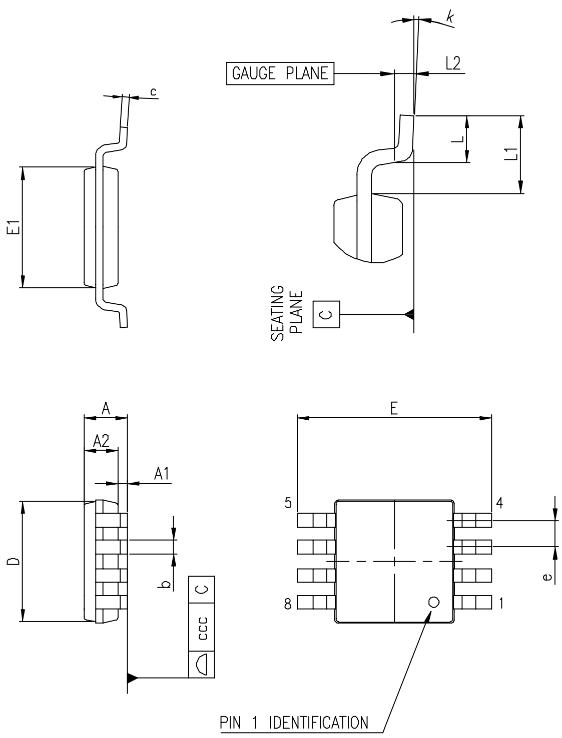
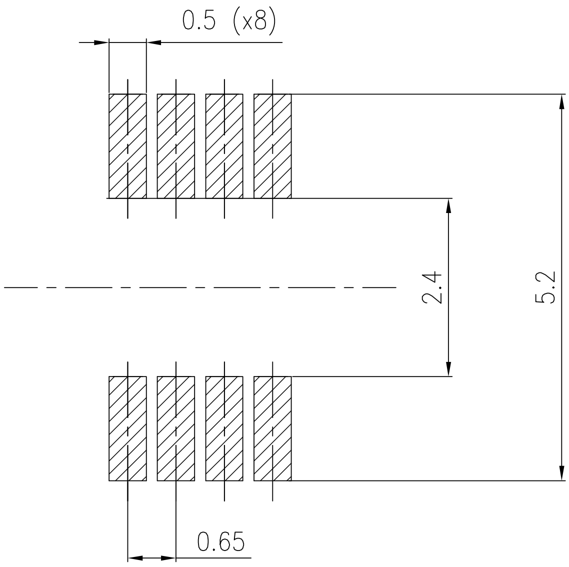


Table 8. MiniSO8 package mechanical data

Dim	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

Figure 52. MiniSO8 recommended footprint



6 Ordering information

Table 9. Order code

Order code	Package	Packing	Marking
TSB182IDT	SO8	Tape and reel	TSB182I
TSB182IYDT (1)			TSB182IY
TSB182IST	MiniSO8		K238
TSB182IYST (1)			K239

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 10. Document revision history

Date	Revision	Changes
07-Jul-2023	1	Initial release.

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