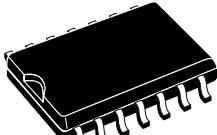


Automotive grade, low-power quad voltage comparator

Features



SO14



TSSOP14

- AEC-Q100 qualified 
- Wide single supply voltage range or dual supplies +2 V to +36 V or ± 18 V to ± 18 V
- Very low supply current 1 mA (typ., all channels), essentially independent of supply voltage
- Low input bias current: 20 nA typ.
- Low input offset current: ± 5 nA typ.
- Input common-mode voltage range includes negative rail
- Low output saturation voltage: 250 mV typ. ($I_O = 4$ mA)
- Input voltage range can exceed the positive supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs



QFN16 3x3
wettable flank

Applications

- Level shifters
- Sampling circuits
- Peak & zero crossing detectors
- Threshold detectors
- Automotive

Description

Maturity status link

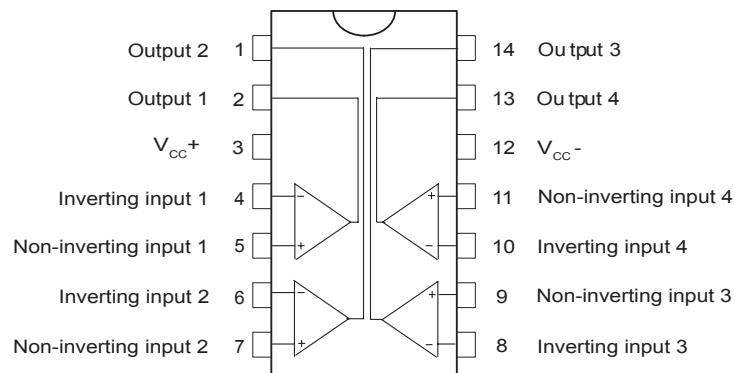
[LM2901B](#)

The LM2901B consists of four independent low-power voltage comparators designed specifically to operate from a single supply over a wide range of voltages. It is fully specified at 5 V and 36 V single supply voltage operation, however operation from dual power supplies is also possible.

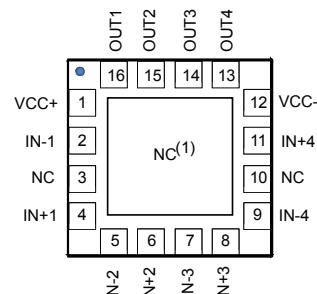
The B-grade version of the LM2901 comparators offers an increased maximum operating voltage of 40 V and improved electrical characteristics.

1 Pin configuration

Figure 1. Pin connections (top view)



SO14 and TSSOP14



QFN16 3 x 3

2 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
Vcc	Supply voltage ⁽¹⁾	±20 or 40	V
Vid	Differential input voltage ⁽²⁾	±40	
Vin	Input voltage	-0.3 to 40	
Iin	Input current ⁽³⁾	10	mA
	Output sinking current	20	
	Duration of output short circuit to ground ⁽⁴⁾	Infinite	s
Tstg	Storage temperature range	-65 to 150	°C
Tj	Maximum junction temperature	150	
Rthja	Thermal resistance junction to ambient ⁽⁵⁾ SO-14 TSSOP-14 QFN16	105 100 45	°C/W
Rthjc	Thermal resistance junction to case ⁽⁵⁾ SO-14 TSSOP-14 QFN16	31 32 14	
ESD	HBM: human body model ⁽⁶⁾ MM: machine model ⁽⁷⁾ CDM: charged device model ⁽⁸⁾	500 100 1500	V

1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. Input current must be limited by a resistor in series with the inputs to keep Vin in the range of the specified AMR.
4. Short-circuits from the output to Vcc+ can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
5. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
6. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
7. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
8. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
Vcc	Supply voltage	2 to 36	V
Vicm	Common-mode input voltage range ⁽¹⁾ Tamb = 25 °C Common-mode input voltage range Tmin ≤ Tamb ≤ Tmax	Vcc- to Vcc+ - 1.5, max. Vcc- + 32 Vcc- to Vcc+ - 2, max. Vcc- + 32	
T	Operating free-air temperature range	-40 to 125	°C

1. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator provides a proper output state. The low input voltage state must not be less than -0.3 V (or 0.3 V below the negative power supply, if used).

3 Electrical characteristics

$V_{CC+} = 5 \text{ V}$ and 36 V , $V_{CC-} = 0 \text{ V}$, $V_O = 1.4 \text{ V}$, R_L connected to ground, $T = 25^\circ\text{C}$ (unless otherwise specified).

Table 3. Electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input offset voltage ⁽¹⁾ $T_{min} < T < T_{max}$			4 5	mV
I_{IB}	Input bias current ⁽²⁾ $T_{min} < T < T_{max}$		20	150 200	nA
I_{IO}	Input offset current $T_{min} < T < T_{max}$		5	30 40	nA
A_{VD}	$V_{CC} = 15 \text{ V}$, $R_L = 15 \text{ k}\Omega$, $V_O = 1$ to 11 V		200		V / mV
I_{CC}	Supply current, all comparators, no load $V_{CC} = 5 \text{ V}$ $T_{min} < T < T_{max}$ $V_{CC} = 36 \text{ V}$ $T_{min} < T < T_{max}$		0.8 1.2	2 2.5 2.5	mA
V_{OL}	Low-level output voltage $V_{CC} = 5 \text{ V}$, $V_{ID} = -1 \text{ V}$, $I_{SINK} = 4 \text{ mA}$ $T_{min} < T < T_{max}$ $V_{CC} = 36 \text{ V}$, $V_{ID} = -1 \text{ V}$, $I_{SINK} = 4 \text{ mA}$ $T_{min} < T < T_{max}$		250 250	350 350 600 600	mV
I_{OH}	High-level output current $V_{CC} = V_O = 36 \text{ V}$, $V_{ID} = 1 \text{ V}$ $T_{min} < T < T_{max}$		0.1	1	nA µA
I_{SINK}	Output sink current $V_{ID} = -1 \text{ V}$, $V_O = 1.5 \text{ V}$ $V_{CC} = 5 \text{ V}$ $T_{min} < T < T_{max}$ $V_{CC} = 36 \text{ V}$ $T_{min} < T < T_{max}$	8 7 11 10	17 10 22 13		mA
t_{res}	Small signal response time $R_L = 5.1 \text{ k}\Omega$ to V_{CC} ⁽³⁾ $V_{CC} = 5 \text{ V}$ $V_{CC} = 36 \text{ V}$		1.0 0.9		µs
t_{rel}	Large signal response time ⁽⁴⁾ TTL input ($V_{ref} = +1.4 \text{ V}$, $R_L = 5.1 \text{ k}\Omega$ to V_{CC}) Output signal at 50% of final value Output signal at 95% of final value			500 1	ns µs

- At output switch point, $V_O \approx 1.4 \text{ V}$, $RS = 0 \Omega$ with V_{CC} from 5 V to 36 V , and over the full input common-mode range (0 V to $V_{CC+} - 1.5 \text{ V}$, max. $V_{CC-} + 32 \text{ V}$).
- The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading charge exists on the reference of input lines.
- The response time specified is for a 100 mV input step with 5 mV overdrive.

-
- 4. Maximum values are guaranteed by design and evaluation.

4 Typical performance characteristics

Figure 2. Supply current vs. supply voltage

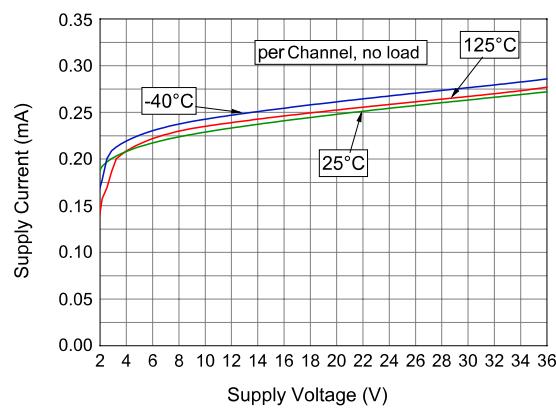


Figure 3. Input offset voltage vs. supply voltage at $V_{icm} = V_{cc}/2$

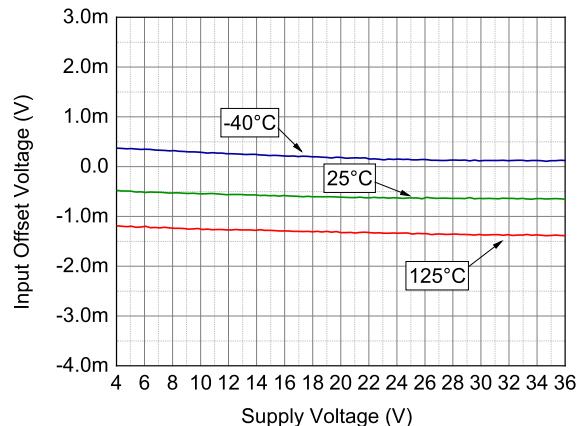


Figure 4. Input offset voltage vs. common-mode voltage at $V_{cc} = 36$ V

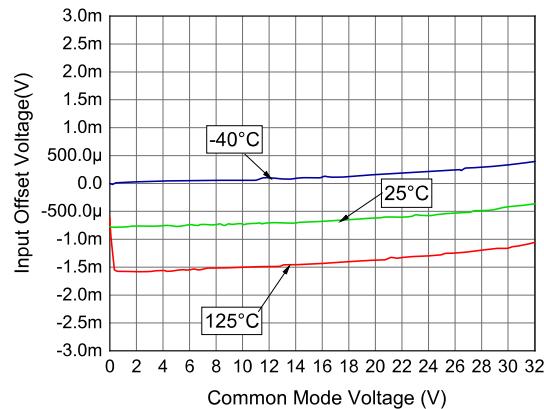


Figure 5. Input bias current vs. supply voltage at $V_{icm} = V_{cc}/2$

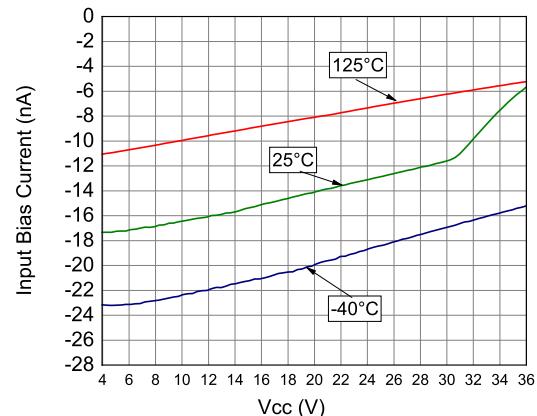


Figure 6. Input bias current vs. common-mode voltage at $V_{cc} = 36\text{ V}$

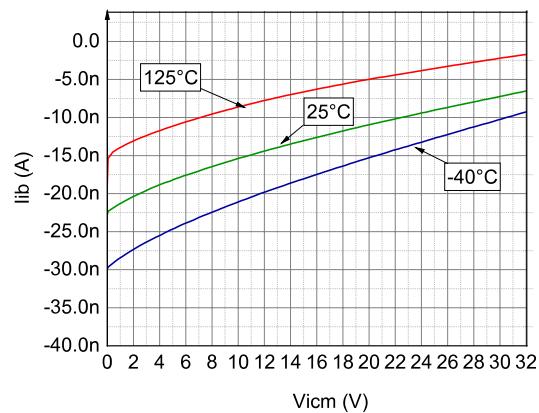


Figure 7. Output saturation voltage vs. output current

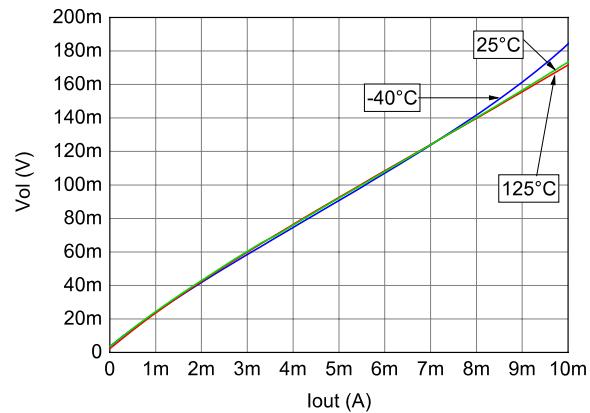


Figure 8. Output saturation current vs. output voltage at $V_{cc} = 36\text{ V}$

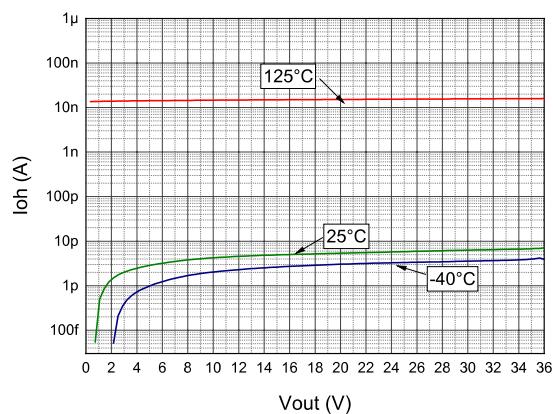


Figure 9. Positive step response

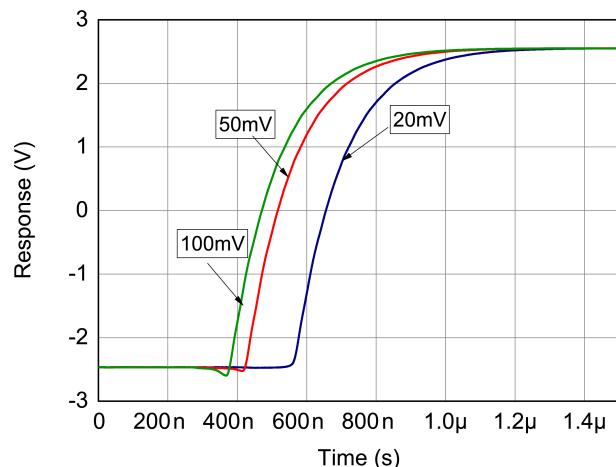


Figure 10. Negative step response

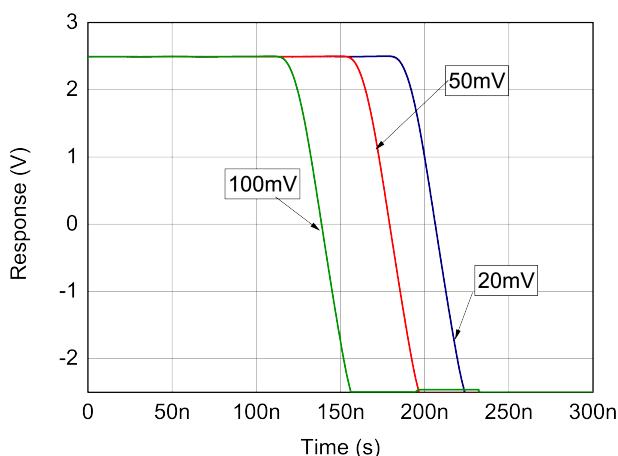


Figure 11. Propagation delay vs. overdrive for positive steps at $V_{cc} = 36\text{ V}$

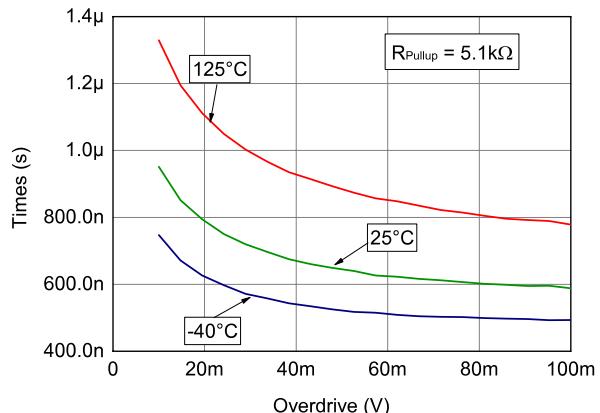
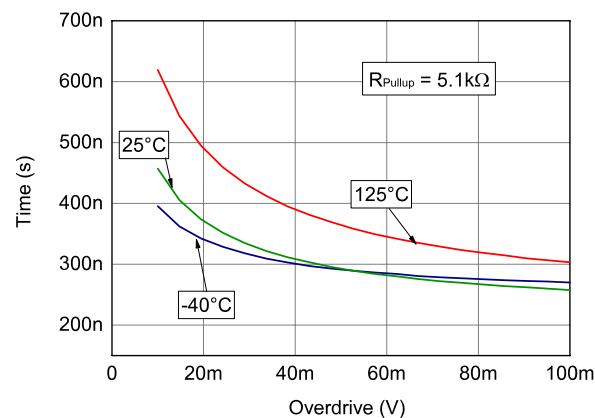


Figure 12. Propagation delay vs. overdrive for negative steps at V_{CC} = 36 V

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 SO-14 package information

Figure 13. SO-14 package outline

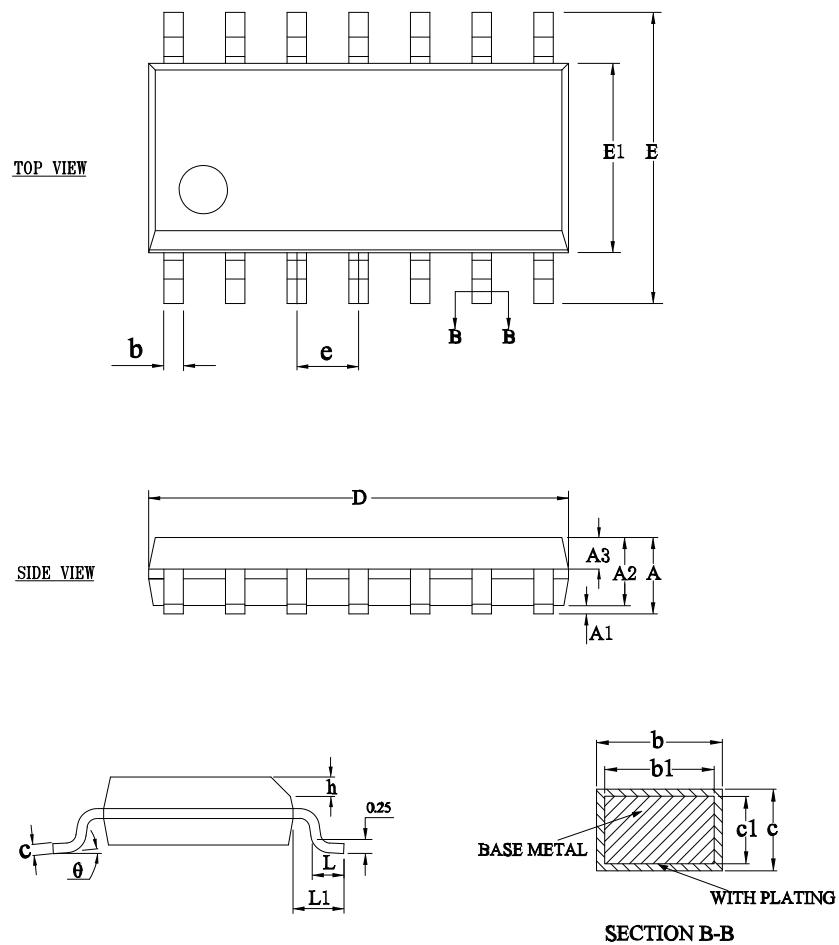
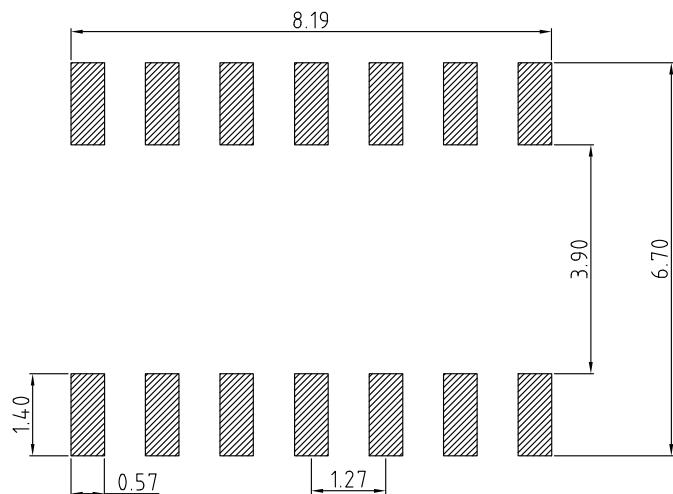


Table 4. SO-14 package mechanical data

Dim.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.225	0.004		0.009
A2	1.30	1.40	1.50	0.051	0.055	0.059
A3	0.60	0.65	0.70	0.024	0.026	0.028
b	0.39		0.47	0.015		0.019
b1	0.38	0.41	0.44	0.015	0.016	0.017
c	0.20		0.24	0.008		0.009
c1	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	8.55	8.65	8.75	0.337	0.341	0.344
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010		0.020
L	0.50		0.80	0.020		0.031
L1	1.05 REF			0.041 REF		
θ	8° (max)					

Figure 14. SO-14 recommended footprint

5.2 TSSOP-14 package information

Figure 15. TSSOP-14 package outline

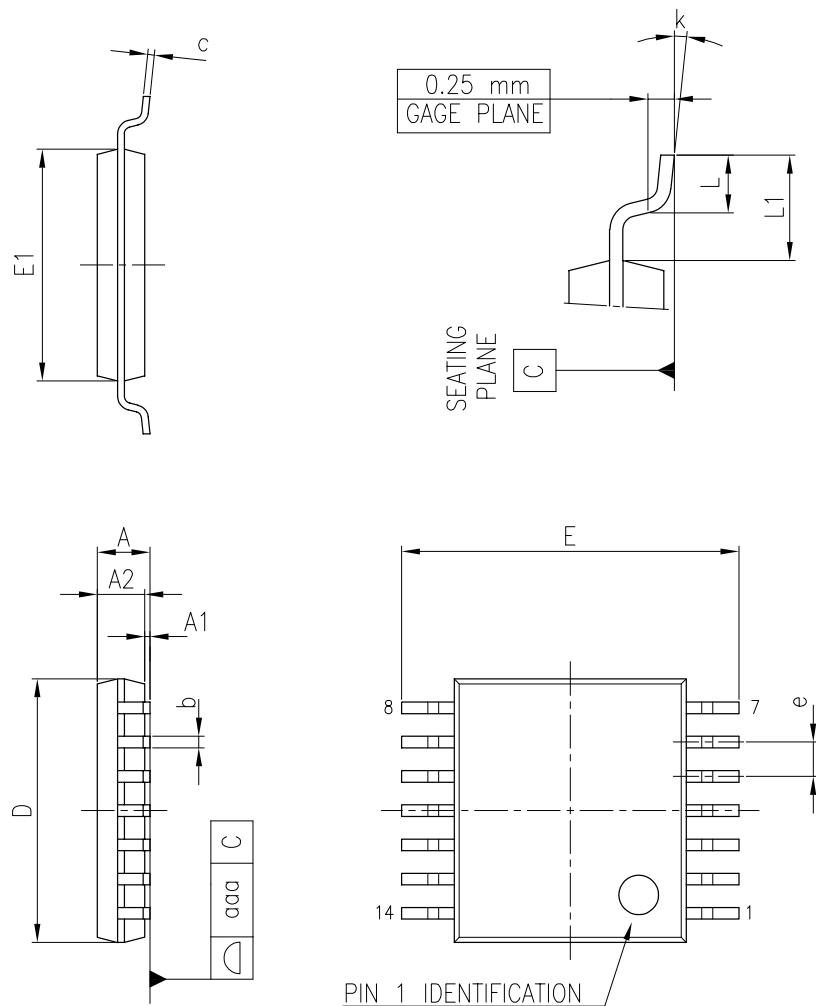
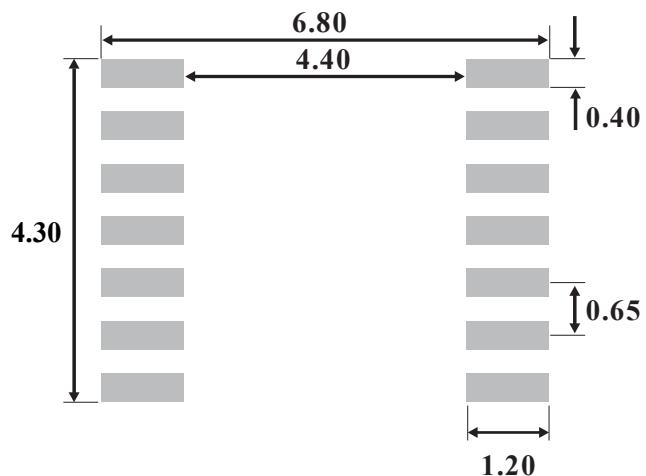


Table 5. TSSOP-14 package mechanical data

Dim.	Dimension					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.25 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	8° (max)					
aaa			0.10			0.004

Figure 16. TSSOP-14 recommended footprint



5.3 QFN16 3x3 wettable flank package information

Figure 17. QFN16 3x3 mm wettable flank drawing outline

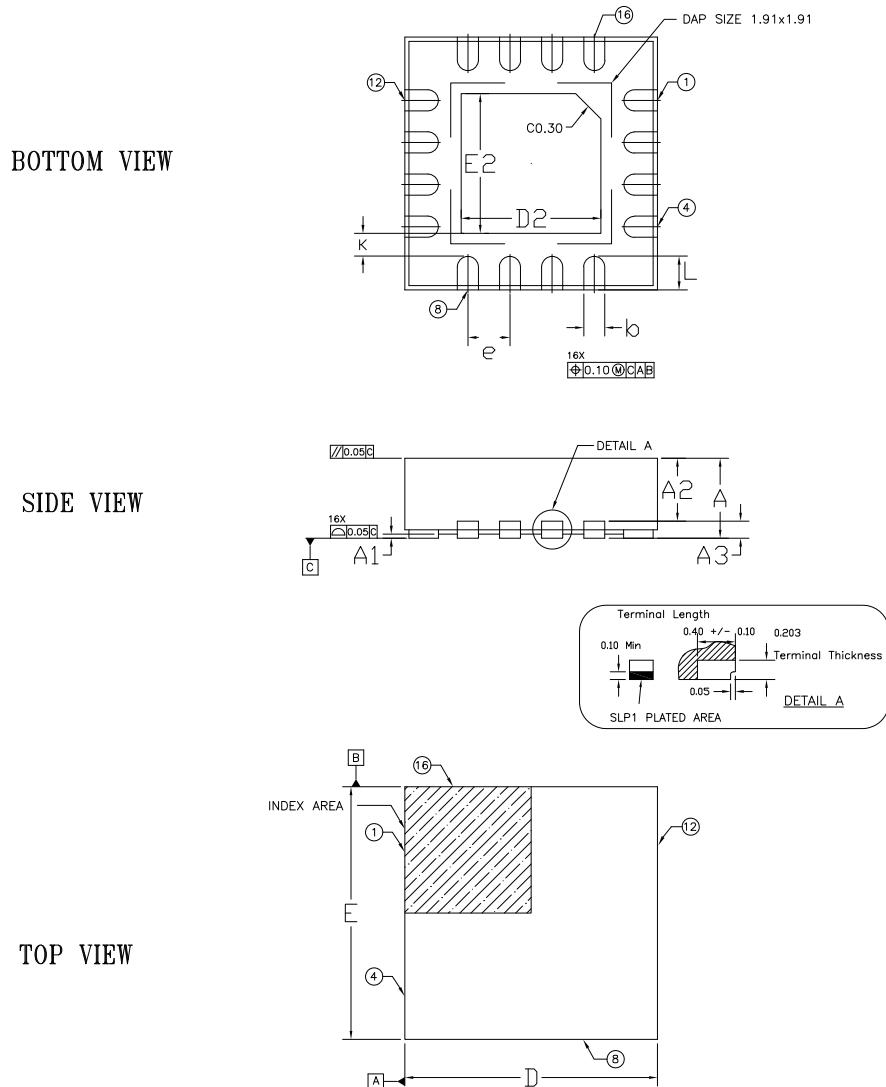
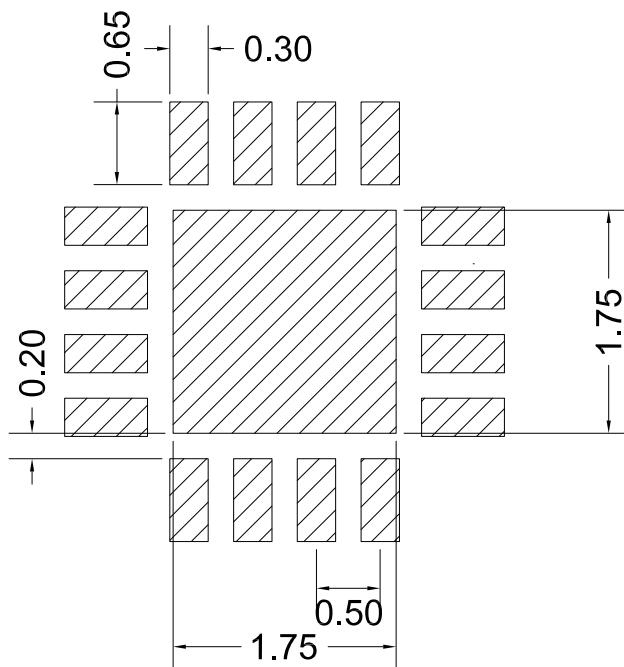


Table 6. QFN16 3x3 wettable flank mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0,90	0,95	1,00	0,035	0,037	0,039
A1	0,00		0,05	0,000		0,002
A2		0,75			0,030	
A3		0,20			0,008	
b	0,20	0,25	0,30	0,008	0,010	0,012
D		3,00			0,118	
E		3,00			0,118	
e		0,50			0,020	
D2	1,56	1,66	1,76	0,061	0,065	0,069
E2	1,56	1,66	1,76	0,061	0,065	0,069
K		0,27			0,011	
L	0,30	0,40	0,50	0,012	0,016	0,020

Figure 18. QFN16 3x3 wettable flank recommended footprint



6 Ordering information

Table 7. Order code

Order code	Temperature range	Package	Packaging	Marking
LM2901BYDT ⁽¹⁾	-40 to +125 °C	SO-14	Tape & reel	LM2901BY
LM2901BYPT ⁽¹⁾		TSSOP-14		LM2901BY
LM2901BYQ5T ⁽¹⁾		QFN16 wf		K432

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

Revision history

Table 8. Document revision history

Date	Revision	Changes
21-Jul-2023	1	Initial release.

Contents

1	Pin configuration	2
2	Maximum ratings	3
3	Electrical characteristics	4
4	Typical performance characteristics	6
5	Package information	9
5.1	SO-14 package information	9
5.2	TSSOP-14 package information	11
5.3	QFN16 3x3 wettable flank package information	13
6	Ordering information	15
	Revision history	16

List of tables

Table 1.	Absolute maximum ratings	3
Table 2.	Operating conditions	3
Table 3.	Electrical characteristics	4
Table 4.	SO-14 package mechanical data	10
Table 5.	TSSOP-14 package mechanical data	12
Table 6.	QFN16 3x3 wettable flank mechanical data	14
Table 7.	Order code	15
Table 8.	Document revision history	16

List of figures

Figure 1.	Pin connections (top view)	2
Figure 2.	Supply current vs. supply voltage	6
Figure 3.	Input offset voltage vs. supply voltage at $V_{icm} = V_{cc}/2$	6
Figure 4.	Input offset voltage vs. common-mode voltage at $V_{cc} = 36\text{ V}$	6
Figure 5.	Input bias current vs. supply voltage at $V_{icm} = V_{cc}/2$	6
Figure 6.	Input bias current vs. common-mode voltage at $V_{cc} = 36\text{ V}$	7
Figure 7.	Output saturation voltage vs. output current	7
Figure 8.	Output saturation current vs. output voltage at $V_{cc} = 36\text{ V}$	7
Figure 9.	Positive step response.	7
Figure 10.	Negative step response	7
Figure 11.	Propagation delay vs. overdrive for positive steps at $V_{cc} = 36\text{ V}$	7
Figure 12.	Propagation delay vs. overdrive for negative steps at $V_{cc} = 36\text{ V}$	8
Figure 13.	SO-14 package outline	9
Figure 14.	SO-14 recommended footprint	10
Figure 15.	TSSOP-14 package outline	11
Figure 16.	TSSOP-14 recommended footprint	12
Figure 17.	QFN16 3x3 mm wettable flank drawing outline	13
Figure 18.	QFN16 3x3 wettable flank recommended footprint	14

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved