

Operational Amplifier

Excellent EMI Immunity

High Output Drive Rail-to-Rail Input/Output

CMOS Operational Amplifier

BD87522FJ-LB BD87524FV-LB

General Description

This product guarantees long time support in industrial market. And it is suitable for usage of industrial applications.
 BD87522FJ-LB and BD87524FV-LB is Rail-to-Rail Input/Output CMOS operational amplifier. An operating voltage range is wide with 4 V to 15 V. This operational amplifier is the most suitable for industrial requirements such as sensor amplifier, battery-powered equipment and so on because it has features of high output drive. Furthermore, they have the advantage of EMI tolerance. It makes easier replacing with conventional products or simpler designing EMI.

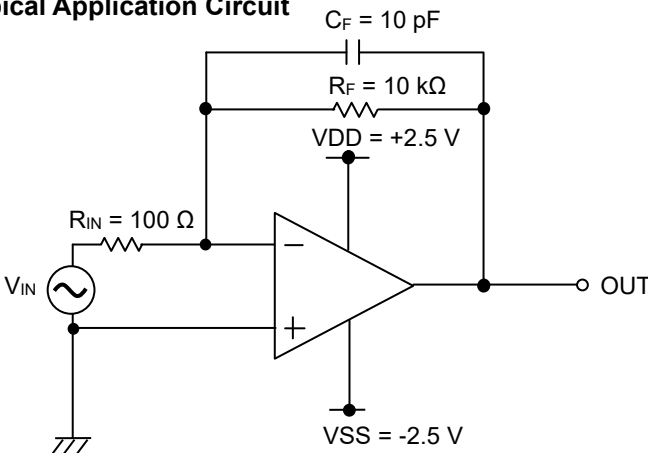
Features

- EMARMOUR™ Series
- Long Time Support Product for Industrial Applications
- Rail-to-Rail Input/Output
- Wide Operating Supply Voltage Range
- High Slew Rate
- High Output Drive

Applications

- Industrial Equipment
- Various Sensor Amplifier
- Battery-Powered Equipment
- Current Detection Amplifier
- ADC Peripheral Circuits, Buffer
- Photodiode Peripheral Circuits
- Various Amplifier

Typical Application Circuit



$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

Key Specifications

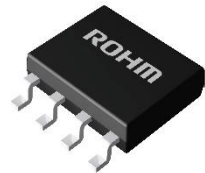
- Operating Supply Voltage Range
 - Single Supply: 4.0 V to 15.0 V
 - Dual Supply: ±2.0 V to ±7.5 V
- Operating Temperature Range: -40 °C to +125 °C
- Input Offset Voltage: 1 mV(max)
- Output Current (V_{OUT} = 0.5 V): 16.5 mA (Typ)

Package

- SOP-J8
- SSOP-B14

W (Typ) x D (Typ) x H (Max)

- 4.9 mm x 6.0 mm x 1.65 mm
- 5.0 mm x 6.4 mm x 1.35 mm



SOP-J8



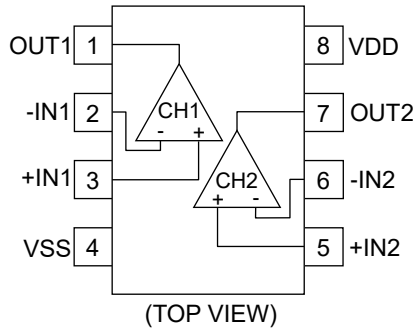
SSOP-B14

EMARMOUR™ is a trademark or a registered trademark of ROHM Co., Ltd.

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

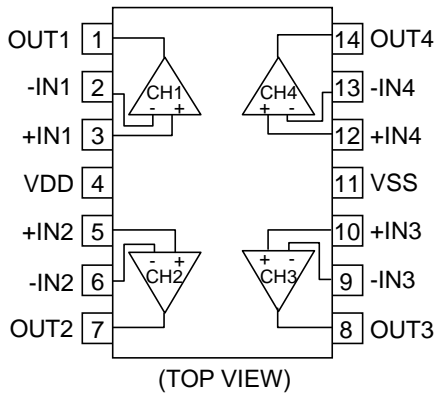
Pin Configuration

BD87522FJ-LB (SOP-J8)



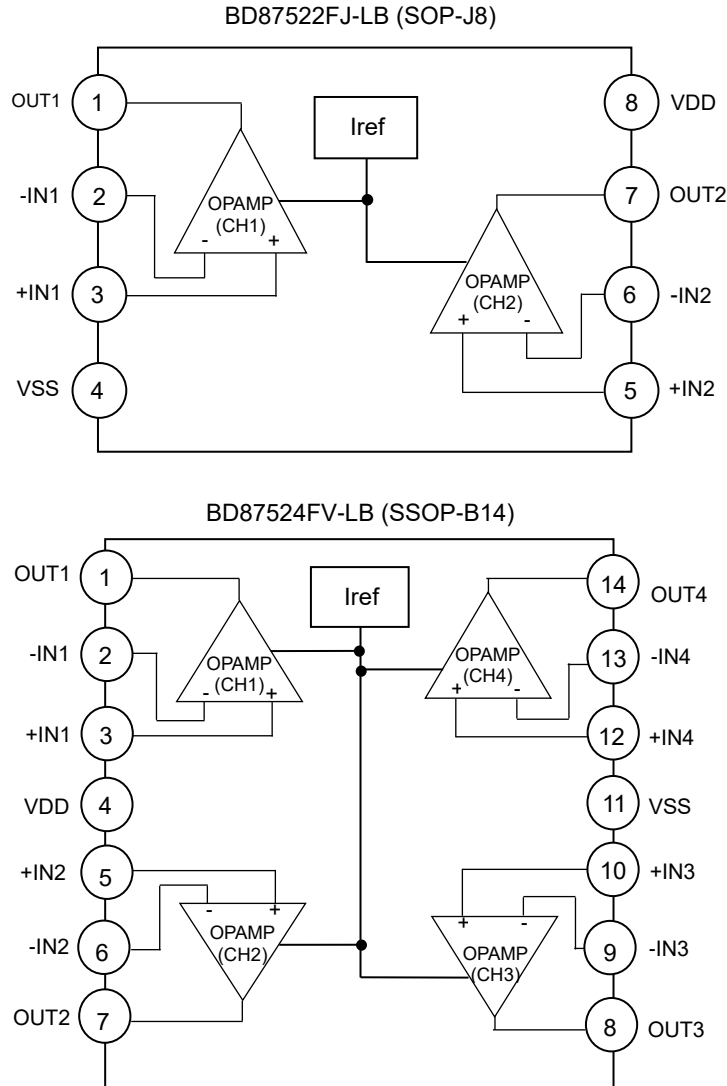
Pin No.	Pin Name
1	OUT1
2	-IN1
3	+IN1
4	VSS
5	+IN2
6	-IN2
7	OUT2
8	VDD

BD87524FV-LB (SSOP-B14)



Pin No.	Pin Name
1	OUT1
2	-IN1
3	+IN1
4	VDD
5	+IN2
6	-IN2
7	OUT2
8	OUT3
9	-IN3
10	+IN3
11	VSS
12	+IN4
13	-IN4
14	OUT4

Block Diagram



Description of Blocks

1. OPAMP:
This block is a Rail-to-Rail output operational amplifier with class-AB input/output circuit and differential input stage.
2. Iref:
This block supplies reference current which is needed to operate OPAMP block.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V _{DD} -V _{SS}	15.5	V
Differential Input Voltage ^(Note 1)	V _{ID}	V _{DD} -V _{SS}	V
Common-mode Input Voltage Range	V _{ICMR}	(V _{SS} - 0.3) to (V _{DD} + 0.3)	V
Input Current	I _I	±10	mA
Maximum Junction Temperature	T _{Jmax}	150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) The differential input voltage indicates the voltage difference between inverting input and non-inverting input.
The input pin voltage is set to V_{SS} or more.

Thermal Resistance^(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 4)	2s2p ^(Note 5)	
SOP-J8				
Junction to Ambient	θ _{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	18	11	°C/W
SSOP-B14				
Junction to Ambient	θ _{JA}	159.6	92.8	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	13	9	°C/W

(Note 2) Based on JESD51-2A(Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	V _{DD}	4.0 ±2.0	-	15.0 ±7.5	V
Operating Temperature	T _{opr}	-40	+25	+125	°C

Function Explanation

1. EMARMOUR™

EMARMOUR™ is the brand name given to ROHM products developed by leveraging proprietary technologies covering layout, process, and circuit design to achieve ultra-high noise immunity that limits output voltage fluctuation to ± 300 mV or less across the entire noise frequency band during noise evaluation testing under the international ISO11452-2 standard. This unprecedented noise immunity reduces design load while improving reliability by solving issues related to noise in the development of vehicle electrical systems.

Electrical Characteristics

○BD87522FJ-LB (Unless otherwise specified $V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Offset Voltage	V_{IO}	-	0.1	1	mV	Absolute value, $V_{ICM} = 0\text{ V}$
		-	-	2		Absolute value, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{ICM} = 0\text{ V}$
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	2	10	$\mu\text{V}/^\circ\text{C}$	Absolute value, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Input Offset Current	I_{IO}	-	1	-	pA	Absolute value
Input Bias Current	I_B	-	1	-	pA	Absolute value
Common-mode Input Voltage Range	V_{ICMR}	V_{SS}	-	V_{DD}	V	-
Supply Current	I_{DD}	-	3.95	6.5	mA	$G = 0\text{ dB}$, No load
		-	-	8		$G = 0\text{ dB}$, No load, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Output Voltage High	V_{OH}	-	50	100	mV	$I_{OUT} = 1\text{ mA}$, $V_{OH} = V_{DD} - V_{OUT}$
		-	-	150		$I_{OUT} = 1\text{ mA}$, $V_{OH} = V_{DD} - V_{OUT}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
		-	260	350		$I_{OUT} = 5\text{ mA}$, $V_{OH} = V_{DD} - V_{OUT}$
		-	-	450		$I_{OUT} = 5\text{ mA}$, $V_{OH} = V_{DD} - V_{OUT}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Output Voltage Low	V_{OL}	-	30	100	mV	$I_{OUT} = 1\text{ mA}$
		-	-	150		$I_{OUT} = 1\text{ mA}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
		-	140	200		$I_{OUT} = 5\text{ mA}$
		-	-	300		$I_{OUT} = 5\text{ mA}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Output Source Current (Note 1)	I_{OH}	-	9.3	-	mA	$V_{OUT} = V_{DD} - 0.5\text{ V}$, Absolute value
		4	-	-		$V_{OUT} = V_{DD} - 0.5\text{ V}$, Absolute value, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Output Sink Current ^(Note 1)	I_{OL}	-	16.5	-	mA	$V_{OUT} = V_{SS} + 0.5\text{ V}$, Absolute value
		9	-	-		$V_{OUT} = V_{SS} + 0.5\text{ V}$, Absolute value, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Large Signal Voltage Gain	A_v	100	110	-	dB	-
		86	-	-		$-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Common-mode Rejection Ratio	CMRR	70	85	-	dB	-
		65	-	-		$-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Power Supply Rejection Ratio	PSRR	75	90	-	dB	-
		75	-	-		$-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Slew Rate	SR	1.6	2.4	-	$\text{V}/\mu\text{s}$	$R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$
		1.2	-	-		$R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Input-Referred Noise Voltage Density	V_n	-	50	-	$\text{nV}/\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$
		-	25	-		$f = 10\text{ kHz}$

(Note 1) Consider the power dissipation of the IC under high temperature environment when selecting the output current value. When the output pin is short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

Electrical Characteristics - continued

○BD87524FV-LB (Unless otherwise specified $V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Offset Voltage	V_{IO}	-	0.1	1	mV	Absolute value, $V_{ICM} = 0\text{ V}$
		-	-	2		Absolute value, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{ICM} = 0\text{ V}$
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	2	10	$\mu\text{V}/^\circ\text{C}$	Absolute value, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Input Offset Current	I_{IO}	-	1	-	pA	Absolute value
Input Bias Current	I_B	-	1	-	pA	Absolute value
Common-mode Input Voltage Range	V_{ICMR}	V_{SS}	-	V_{DD}	V	-
Supply Current	I_{DD}	-	7.9	13.0	mA	$G = 0\text{ dB}$, No load
		-	-	16		$G = 0\text{ dB}$, No load, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Output Voltage High	V_{OH}	-	50	100	mV	$I_{OUT} = 1\text{ mA}$, $V_{OH} = V_{DD} - V_{OUT}$
		-	-	150		$I_{OUT} = 1\text{ mA}$, $V_{OH} = V_{DD} - V_{OUT}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
		-	260	350		$I_{OUT} = 5\text{ mA}$, $V_{OH} = V_{DD} - V_{OUT}$
		-	-	450		$I_{OUT} = 5\text{ mA}$, $V_{OH} = V_{DD} - V_{OUT}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Output Voltage Low	V_{OL}	-	30	100	mV	$I_{OUT} = 1\text{ mA}$
		-	-	150		$I_{OUT} = 1\text{ mA}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
		-	140	200		$I_{OUT} = 5\text{ mA}$
		-	-	300		$I_{OUT} = 5\text{ mA}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Output Source Current (Note 1)	I_{OH}	-	9.3	-	mA	$V_{OUT} = V_{DD} - 0.5\text{ V}$, Absolute value
		4	-	-		$V_{OUT} = V_{DD} - 0.5\text{ V}$, Absolute value, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Output Sink Current ^(Note 1)	I_{OL}	-	16.5	-	mA	$V_{OUT} = V_{SS} + 0.5\text{ V}$, Absolute value
		9	-	-		$V_{OUT} = V_{SS} + 0.5\text{ V}$, Absolute value, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Large Signal Voltage Gain	A_v	100	110	-	dB	-
		86	-	-		$-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Common-mode Rejection Ratio	CMRR	70	85	-	dB	-
		65	-	-		$-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Power Supply Rejection Ratio	PSRR	75	90	-	dB	-
		75	-	-		$-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Slew Rate	SR	1.6	2.4	-	$\text{V}/\mu\text{s}$	$R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$
		1.2	-	-		$R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$
Input-Referred Noise Voltage Density	V_n	-	50	-	$\text{nV}/\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$
		-	25	-		$f = 10\text{ kHz}$

(Note 1) Consider the power dissipation of the IC under high temperature environment when selecting the output current value. When the output pin is short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

Typical Performance Curves

$V_{SS} = 0\text{ V}$

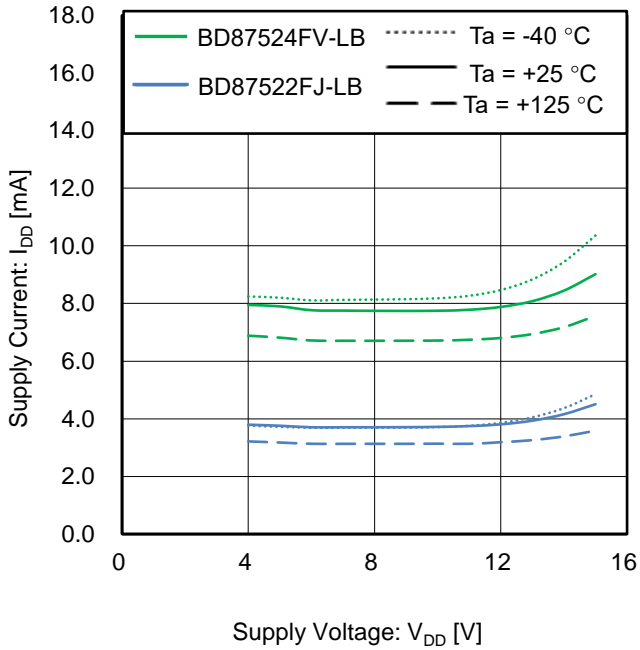


Figure 1. Supply Current vs Supply Voltage

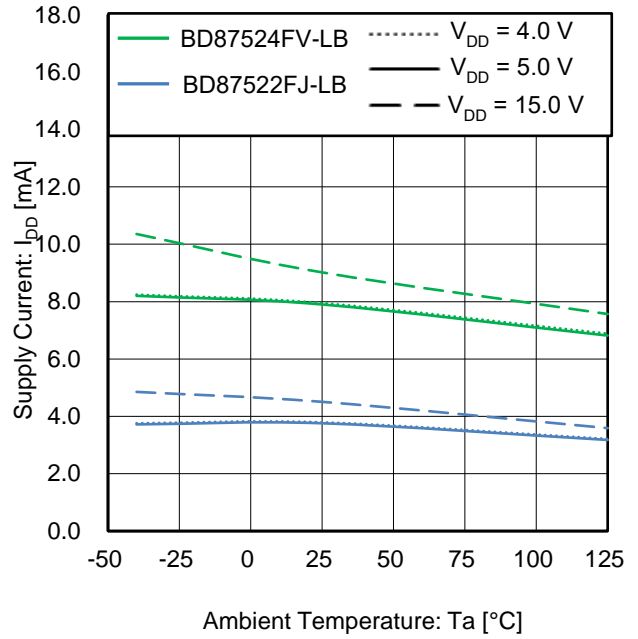


Figure 2. Supply Current vs Ambient Temperature

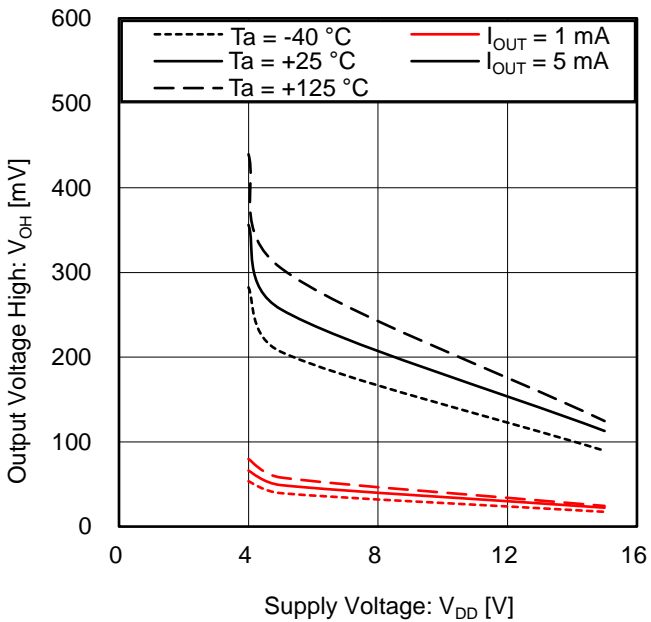


Figure 3. Output Voltage High vs Supply Voltage
($V_{OH} = V_{DD} - V_{OUT}$)

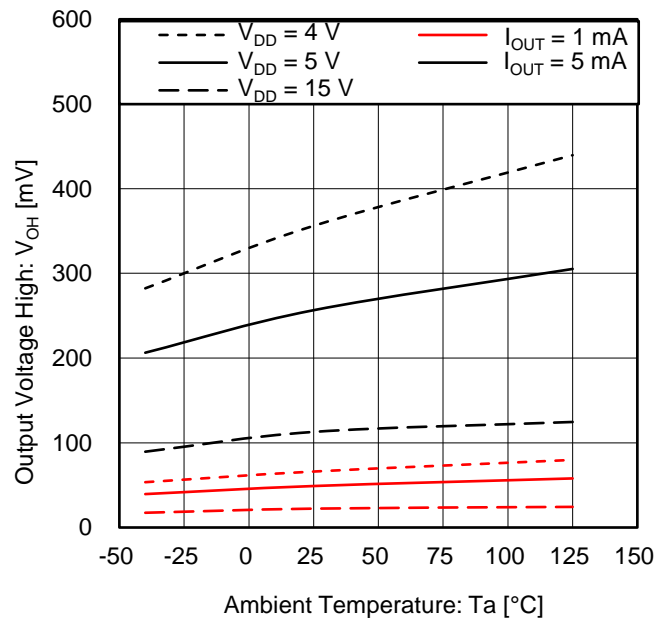


Figure 4. Output Voltage High vs Ambient Temperature
($V_{OH} = V_{DD} - V_{OUT}$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

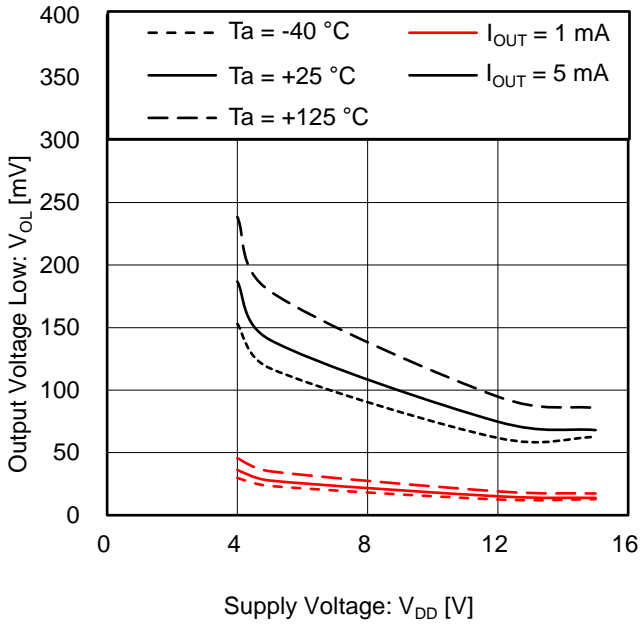


Figure 5. Output Voltage Low vs Supply Voltage

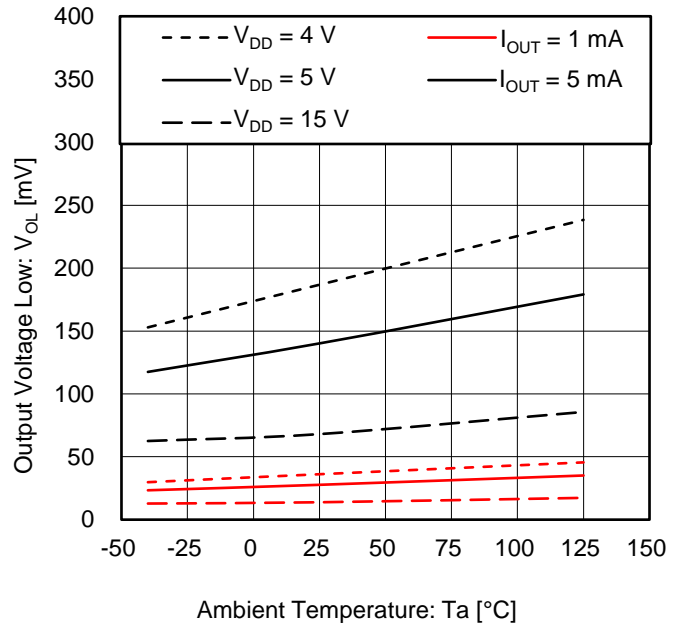


Figure 6. Output Voltage Low vs Ambient Temperature

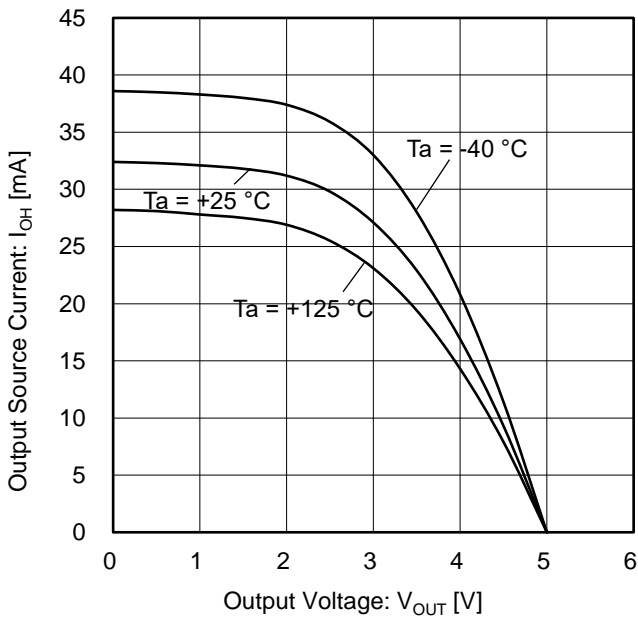


Figure 7. Output Source Current vs Output Voltage ($V_{DD} = 5\text{ V}$)

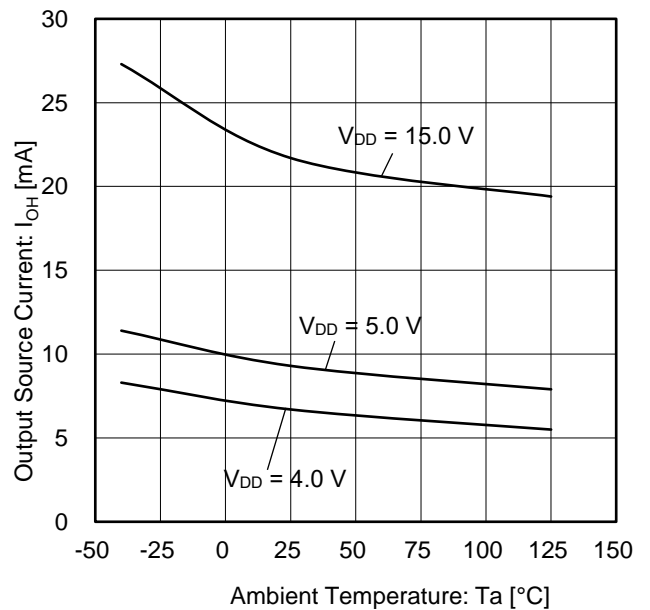


Figure 8. Output Source Current vs Ambient Temperature ($V_{OUT} = V_{DD} - 0.5\text{ V}$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

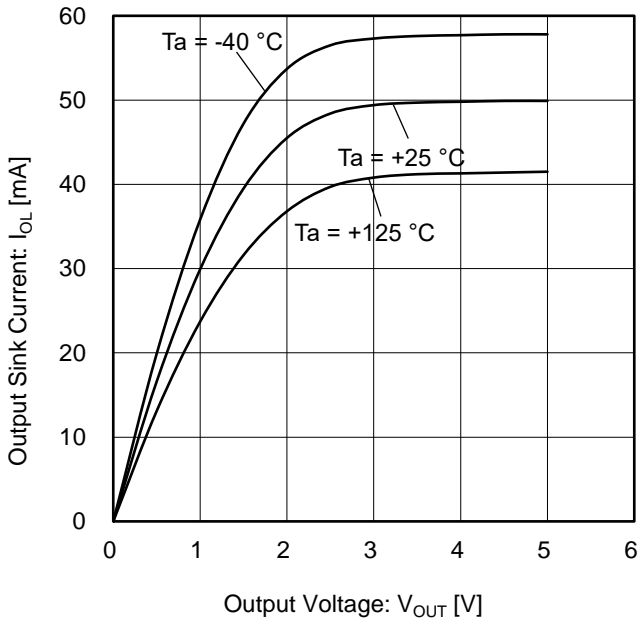


Figure 9. Output Sink Current vs Output Voltage ($V_{DD} = 5\text{ V}$)

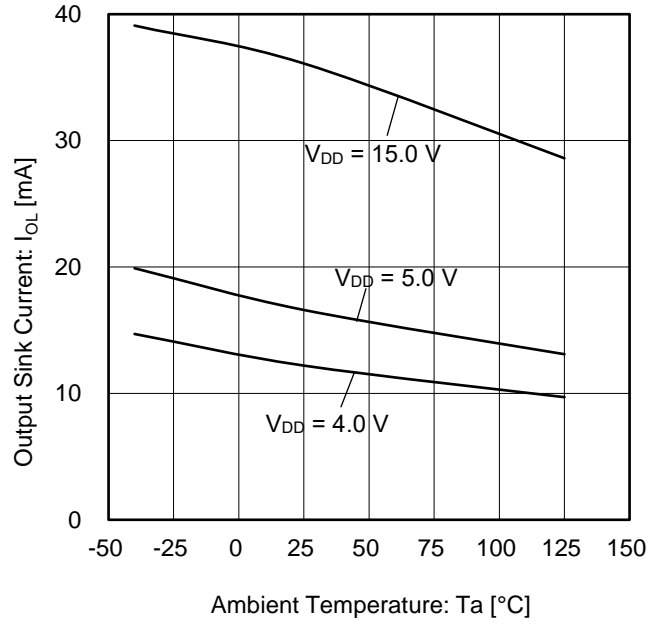


Figure 10. Output Sink Current vs Ambient Temperature ($V_{OUT} = V_{SS} + 0.5\text{ V}$)

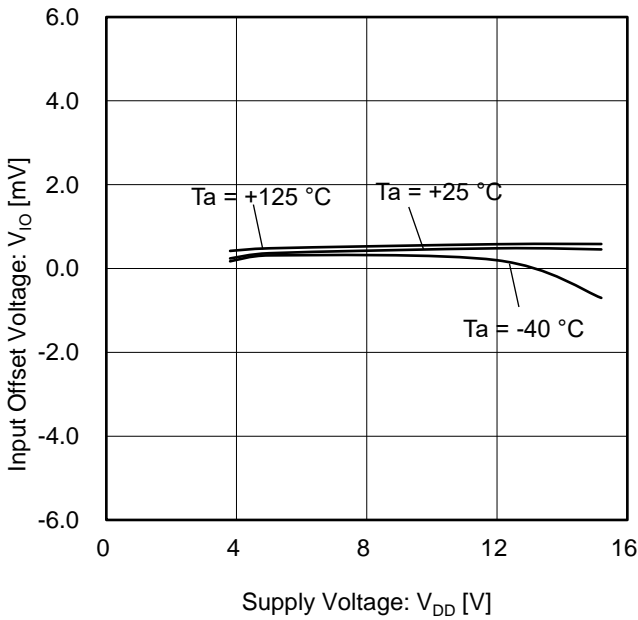


Figure 11. Input Offset Voltage vs Supply Voltage ($V_{ICM} = V_{DD}/2$, $E_K = -V_{DD}/2$)

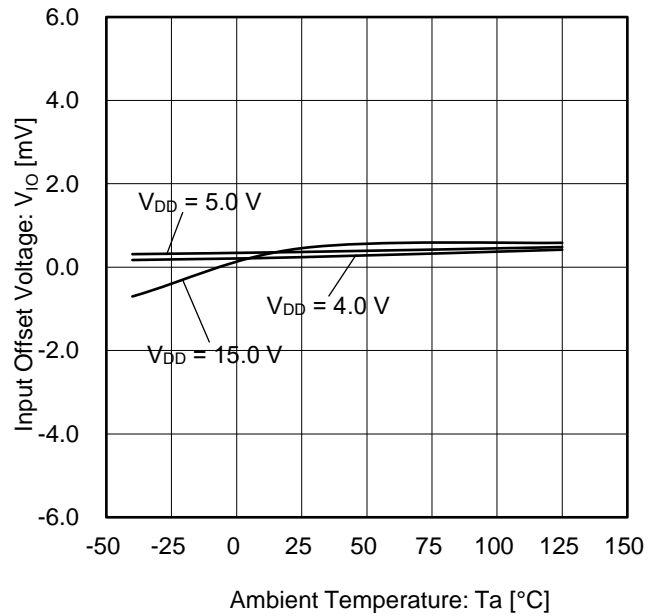


Figure 12. Input Offset Voltage vs Ambient Temperature ($V_{ICM} = V_{DD}/2$, $E_K = -V_{DD}/2$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

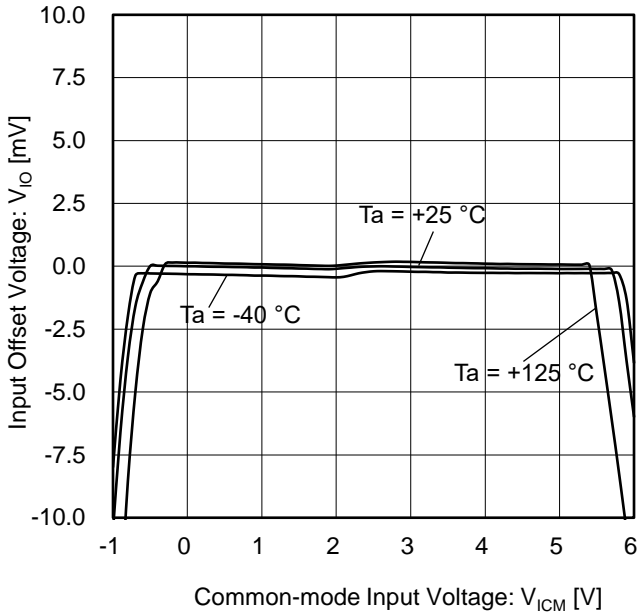


Figure 13. Input Offset Voltage vs Common-mode Input Voltage ($V_{DD} = 5\text{ V}$)

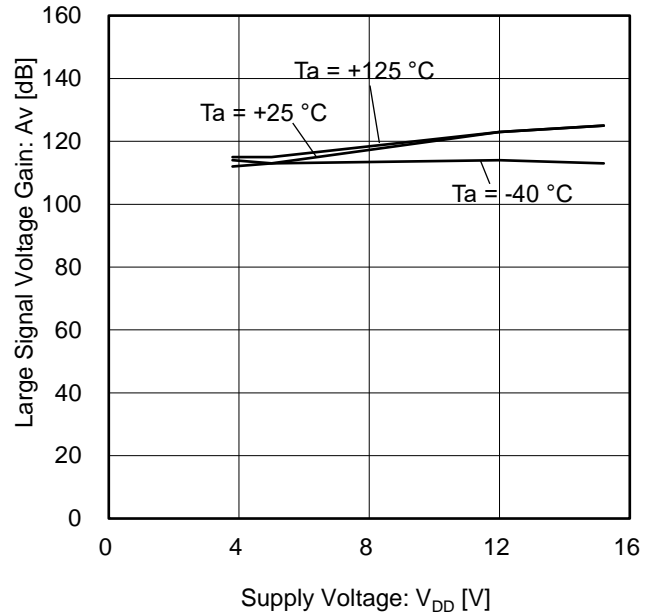


Figure 14. Large Signal Voltage Gain vs Supply Voltage

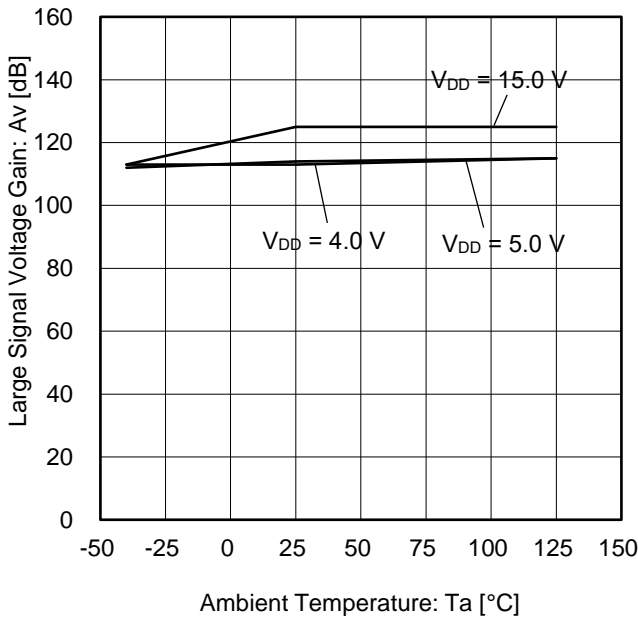


Figure 15. Large Signal Voltage Gain vs Ambient Temperature

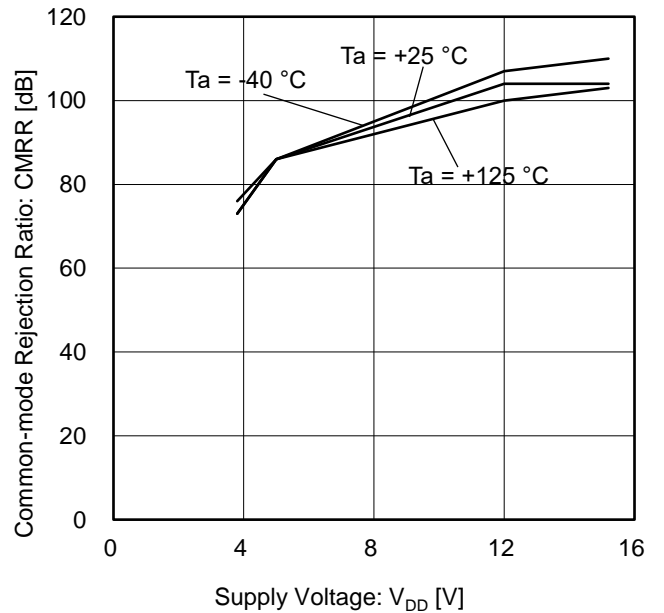


Figure 16. Common-mode Rejection Ratio vs Supply Voltage

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

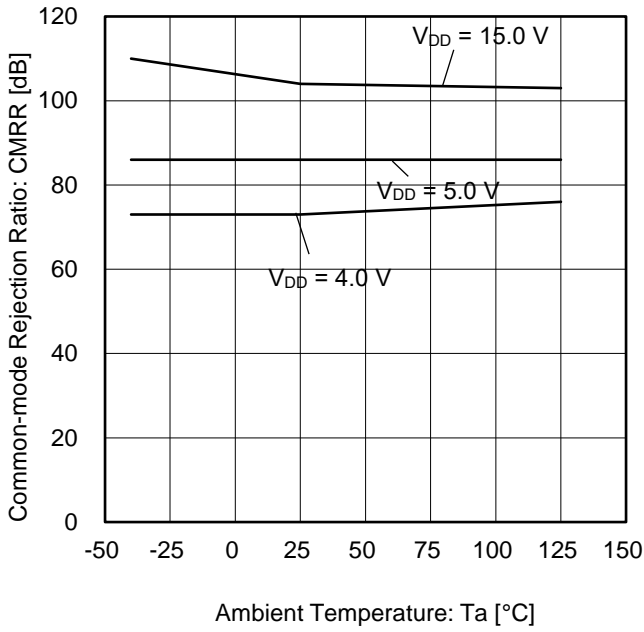


Figure 17. Common-mode Rejection Ratio vs Ambient Temperature

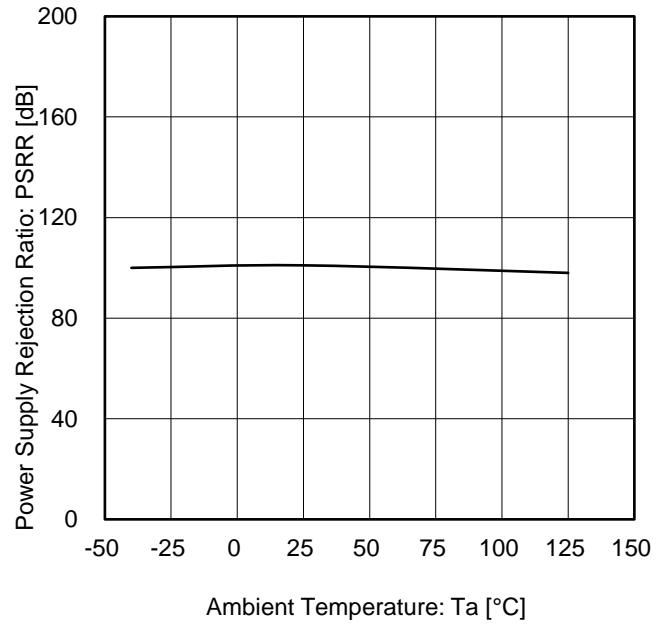


Figure 18. Power Supply Rejection Ratio vs Ambient Temperature

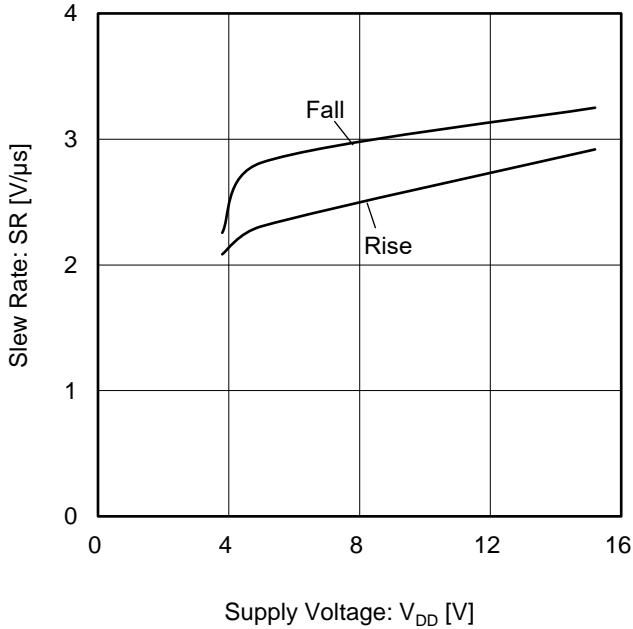


Figure 19. Slew Rate vs Supply Voltage ($T_a = 25\text{ °C}$)

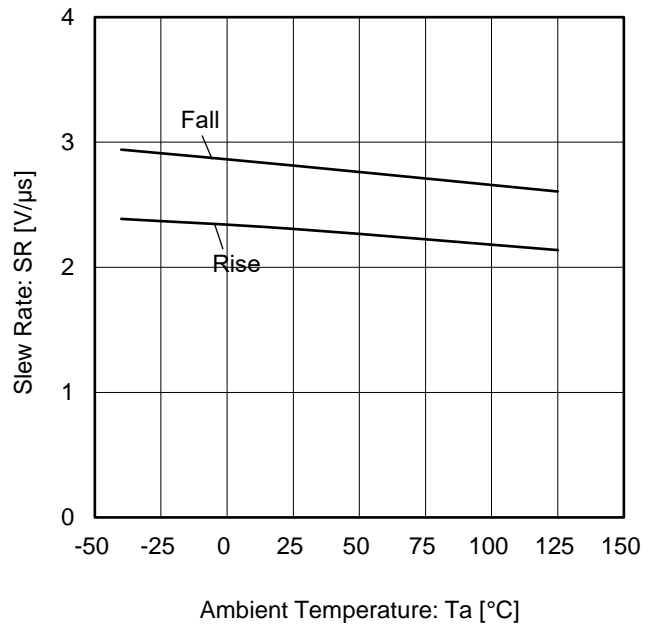


Figure 20. Slew Rate vs Ambient Temperature ($V_{DD} = 5\text{ V}$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Application Information

EMI Immunity

BD87522FJ-LB and BD87524FV-LB have high tolerance for electromagnetic interference from the outside because they have EMI filter, and the EMI design is simple. They are most suitable to replace from conventional products. The data of the IC simple substance on ROHM board are as follows. The test condition is based on ISO11452-2.

<Test Condition> Based on ISO11452-2
 Test Circuit: Voltage Follower
 V_{DD} : 12 V
 V_{IN+} : 6 V
 Test Method: Substituted Law
 (Progressive Wave)
 Field Intensity: 200 V/m
 Test Wave: CW (Continuous Wave)
 Frequency: 200 MHz – 1000 MHz (2 % step)

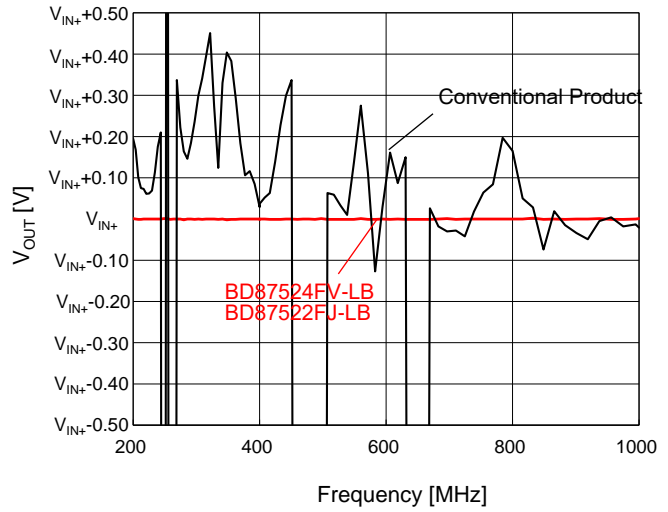


Figure 21. EMI Characteristics

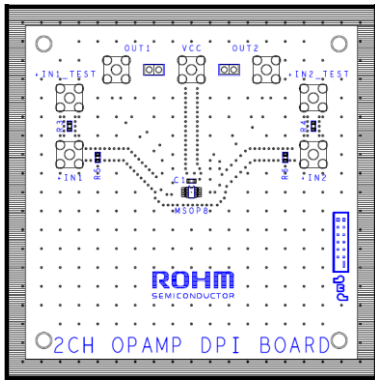


Figure 22. EMI Evaluation Board (BD87522FJ-LB)

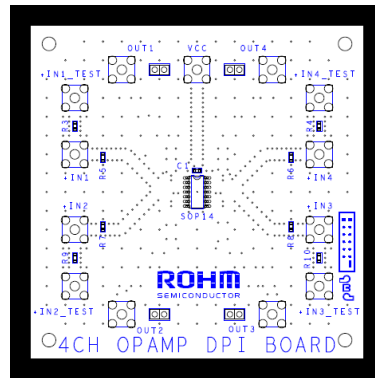


Figure 23. EMI Evaluation Board (BD87524FV-LB)

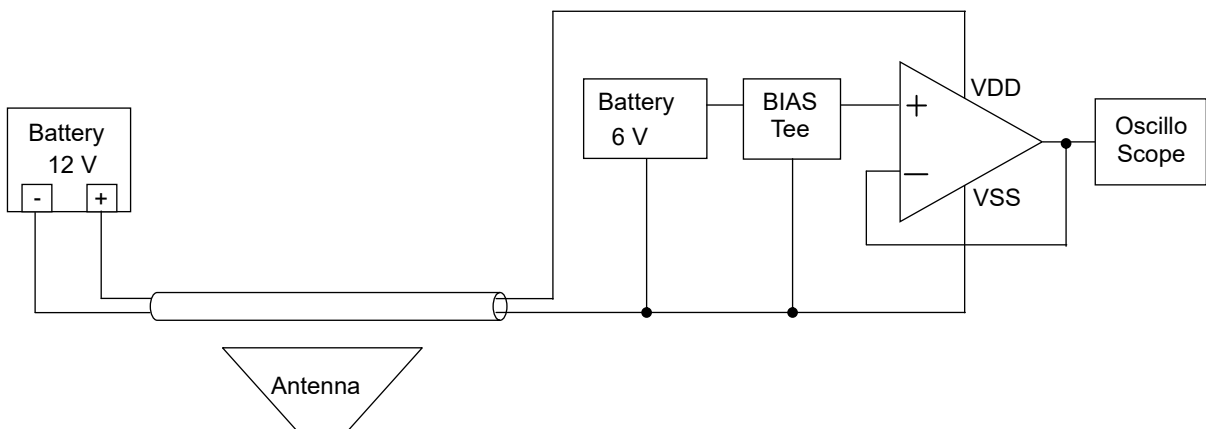


Figure 24. Measurement Circuit of EMI Evaluation

(Note) The above data is obtained using typical IC simple substance on ROHM board. These values are not guaranteed. Design and Evaluate in actual application before use.

Application Information - continued

1. Unused Circuits

When there are unused circuits, it is recommended that they are connected as in right figure, and set the non-inverting input pin to electric potential within the input common-mode voltage range (V_{ICMR}).

2. Input Voltage

Applying $V_{DD} + 0.3$ V to the input pin is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure circuit operation. Note that the circuit operates normally only when the input voltage is within the common-mode input voltage range of the electric characteristics.

3. Power Supply (single/dual)

The Op-Amp operates when the voltage is supplied between the VDD and VSS pin. Therefore, the single supply Op-Amp can be used as dual supply Op-Amp as well.

4. Output Capacitor

When the VDD pin is shorted to VSS (GND) electric potential in a state where electric charge is accumulated in the external capacitor that is connected to the output pin, the accumulated electric charge flow through parasitic elements or pin protection elements inside the circuit and discharges to the VDD pin. It may cause damage to the elements inside the circuit (thermal destruction). When using this IC as an application circuit which does not constitute a negative feedback circuit and does not occur the oscillation by an output capacitive load such as a voltage comparator, connect a capacitor of 0.1 μ F or less to the output pin to prevent IC damage caused by the accumulation of electric charge as mentioned above.

5. Oscillation by Output Capacitor

Pay attention to the oscillation by capacitive load in designing an application which constitutes a negative feedback loop circuit with this IC.

6. Handling the IC

Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuations of the electrical characteristics due to the piezo resistance effects. Pay attention to defecting or bending the board.

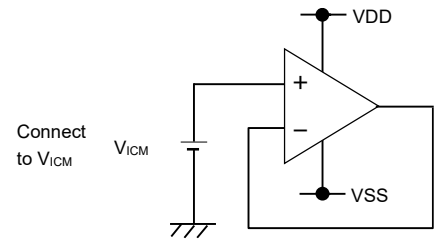


Figure 25. Example of application unused circuit processing

Application Examples

○Voltage Follower

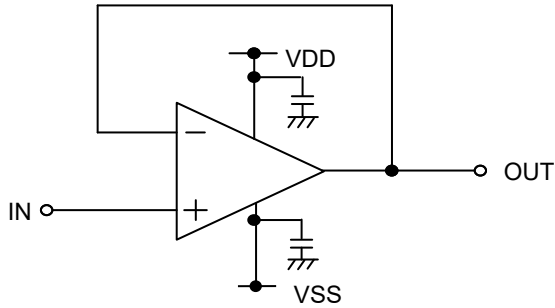


Figure 26. Voltage Follower Circuit

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage (V_{OUT}) due to high input impedance and low output impedance. Computation for output voltage (V_{OUT}) is shown below.

$$V_{OUT} = V_{IN}$$

○Inverting Amplifier

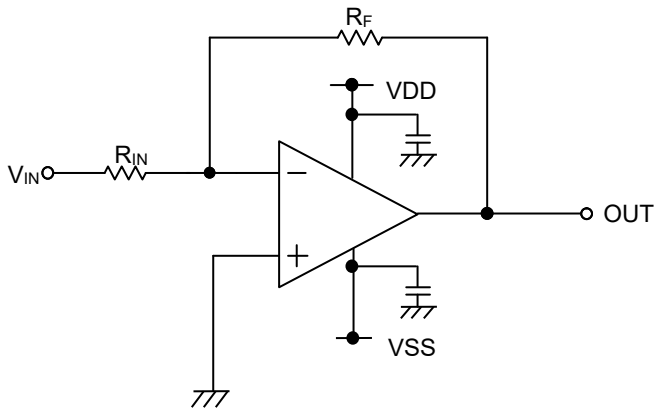


Figure 27. Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain which depends on the ratio of R_{IN} and R_F , and then it outputs phase-inverted voltage. The output voltage is shown in the next expression.

$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

This circuit has input impedance equal to R_{IN} .

○Non-inverting Amplifier

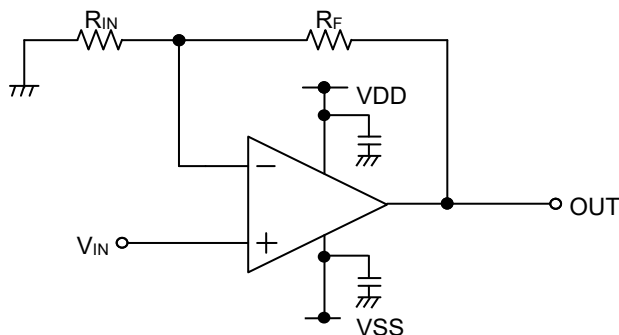


Figure 28. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R_{IN} and R_F . The output voltage (V_{OUT}) is in-phase with the input voltage (V_{IN}) and is shown in the next expression.

$$V_{OUT} = \left(1 + \frac{R_F}{R_{IN}}\right) V_{IN}$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

I/O Equivalence Circuits

○BD87522FJ-LB

Pin No.	Pin Name	Pin Description	Equivalent Circuit
1 7	OUT1 OUT2	Output	
2 3 5 6	-IN1 +IN1 +IN2 -IN2	Input	

○BD87524FV-LB

Pin No.	Pin Name	Pin Description	Equivalence Circuit
1 7 8 14	OUT1 OUT2 OUT3 OUT4	Output	
2 3 5 6 9 10 12 13	-IN1 +IN1 +IN2 -IN2 -IN3 +IN3 +IN4 -IN4	Input	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
 When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

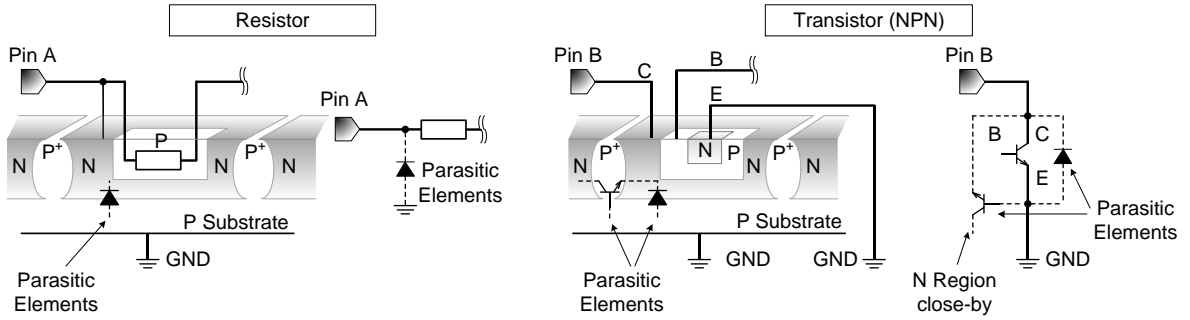
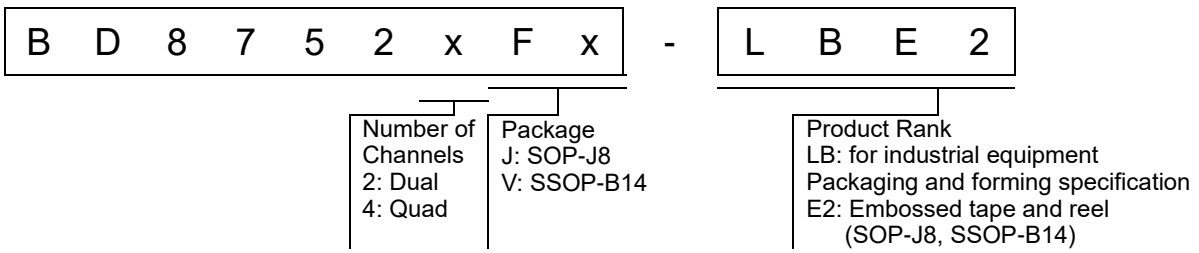


Figure 29. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

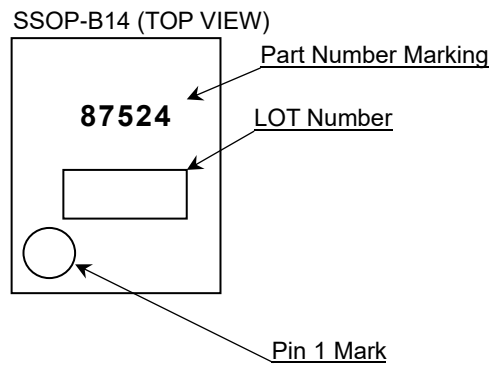
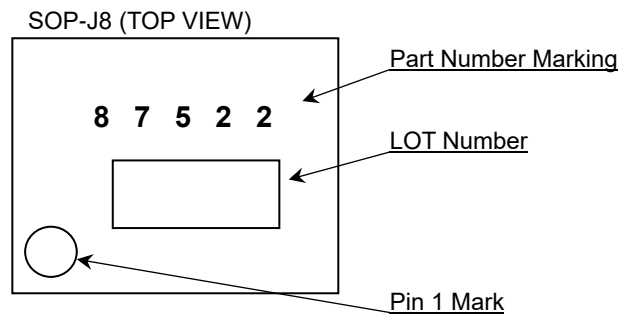
Ordering Information



Lineup

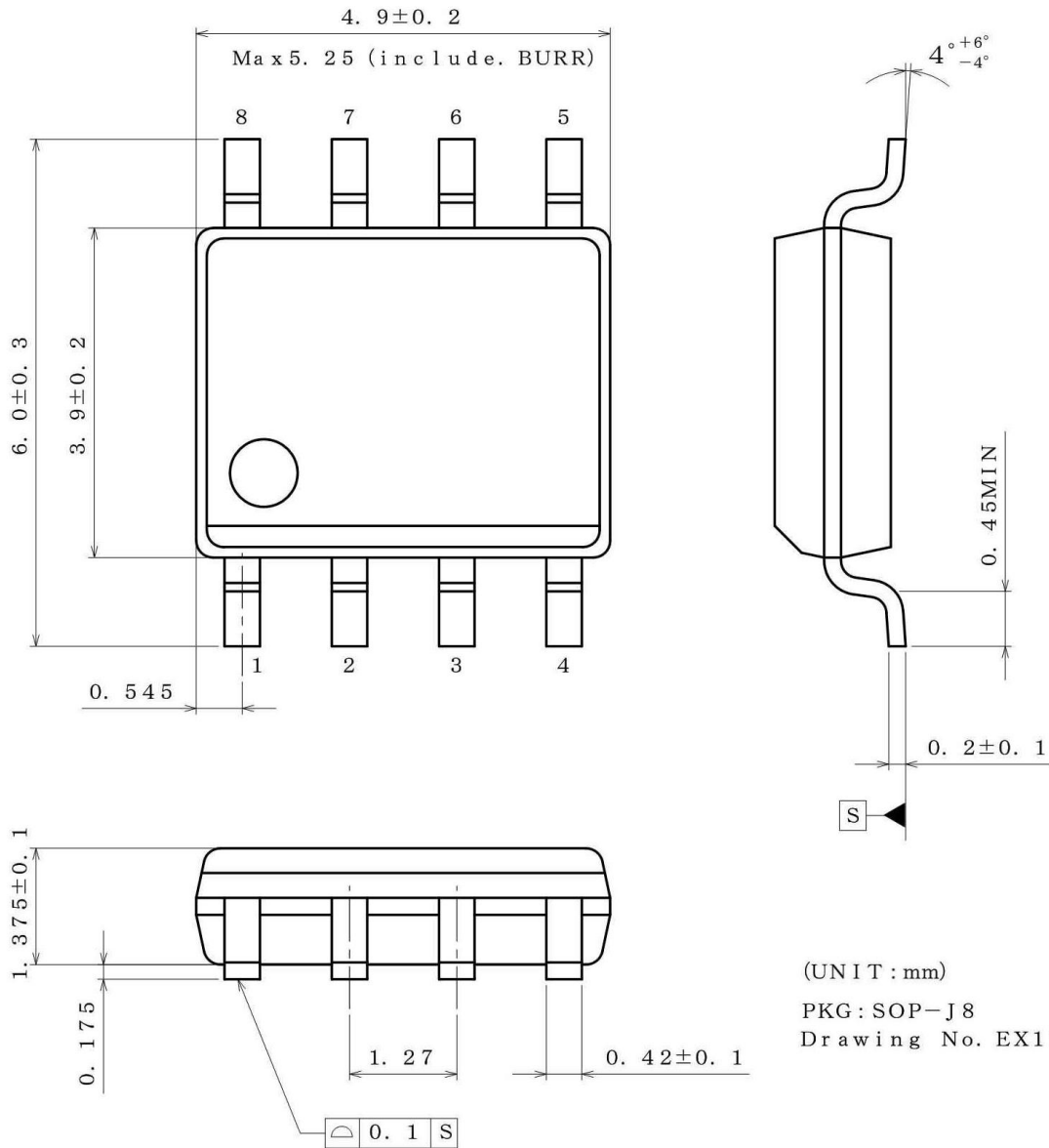
Number of Channels	Package		Orderable Part Number
Dual	SOP-J8	Reel of 2500	BD87522FJ-LBE2
Quad	SSOP-B14	Reel of 2500	BD87524FV-LBE2

Marking Diagram



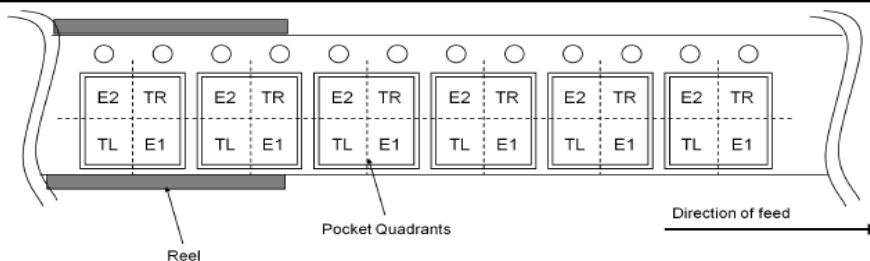
Physical Dimension and Packing Information

Package Name	SOP-J8
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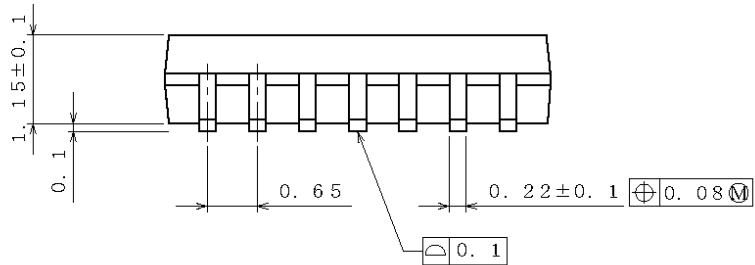
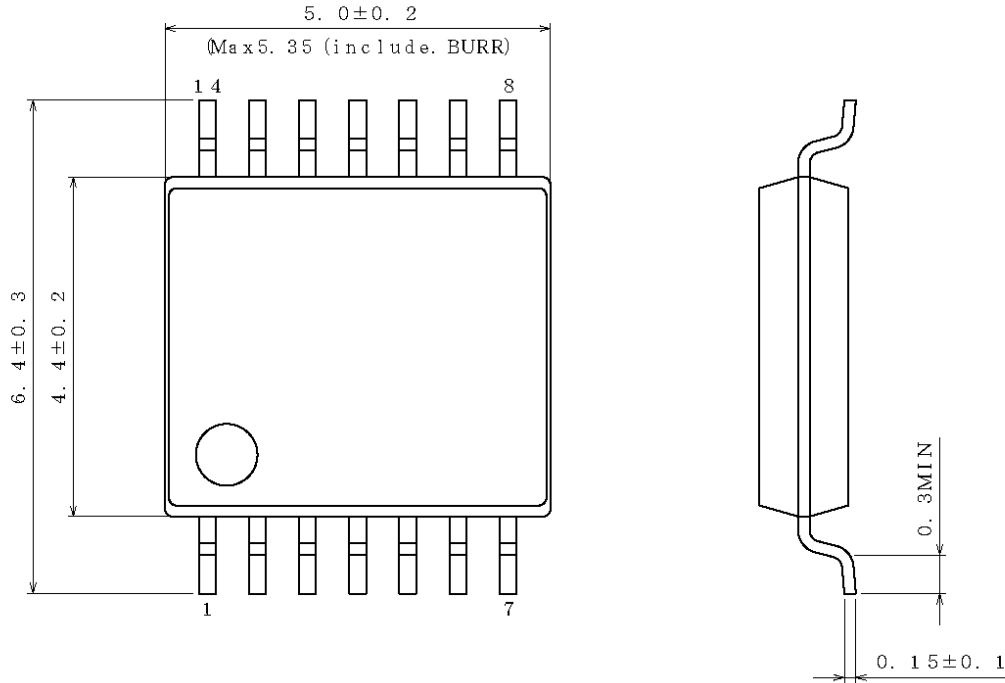
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Physical Dimension and Packing Information – continued

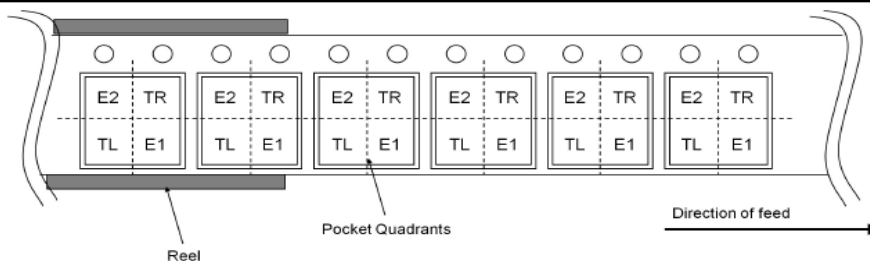
Package Name	SSOP-B14
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(UNIT : mm)
 PKG : SSOP-B14
 Drawing No. EX152-5002

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
15.Nov.2022	001	New Release
11.May.2023	002	Updated Lineup (BD87522FJ-LB)

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
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