

## Automotive MOSFET

## OptiMOS™ 5 Power-Transistor



## Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – enhancement mode – normal level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% avalanche tested
- Very low reverse recovery charge ( $Q_{rr}$ )

## Potential applications

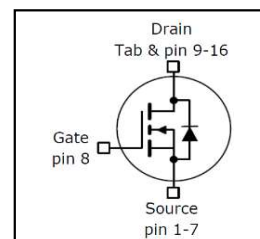
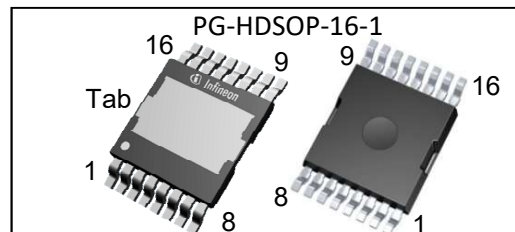
General automotive applications.

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.

## Product Summary

$V_{DS}$	120	V
$R_{DS(on)}$	1.8	m $\Omega$
$I_D$ (chip limited)	309	A



Type	Package	Marking
IAUTN12S5N018T	PG-HDSOP-16-1	5N12N018



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## Maximum ratings

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}$ , Chip limitation <sup>1,2)</sup>	309	A
		$V_{GS}=10\text{ V}$ , DC current <sup>3)</sup>	300	
		$T_a=100\text{ °C}$ , $V_{GS}=10\text{ V}$ , $R_{thJA}$ on top <sup>2,4)</sup>	85	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_c=25\text{ °C}$ , $t_p=100\text{ }\mu\text{s}$	1150	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=150\text{ A}$	510	mJ
Avalanche current, single pulse	$I_{AS}$	–	300	A
Gate source voltage	$V_{GS}$	–	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_c=25\text{ °C}$	358	W
Operating and storage temperature	$T_j, T_{stg}$	–	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	–	–	55/175/56	

## Thermal characteristics<sup>2)</sup>

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	Top	-	-	0.42	K/W
		Bottom (Pin 1-7)	-	9	-	
		Bottom (Pin 9-16)	-	3	-	
Thermal resistance, junction - ambient <sup>4)</sup>	$R_{thJA}$	Top	-	2.8	-	
		Bottom (through PCB)	-	40	-	

## Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

## Static characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$	120	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=270\text{ }\mu\text{A}$	2.6	3.1	3.6	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$	-	0.3	3	$\mu\text{A}$
		$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=100\text{ °C}^{2)}$	-	10	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7\text{ V}$ , $I_D=50\text{ A}$	-	2.0	2.8	m $\Omega$
		$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$	-	1.5	1.8	
Gate resistance <sup>2)</sup>	$R_G$	-	-	1.1	-	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

## Dynamic characteristics<sup>2)</sup>

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=60\text{ V}, f=1\text{ MHz}$	-	8260	10740	pF
Output capacitance	$C_{oss}$		-	2369	3080	
Reverse transfer capacitance	$C_{rss}$		-	45	68	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=60\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=3.5\ \Omega$	-	28	-	ns
Rise time	$t_r$		-	55	-	
Turn-off delay time	$t_{d(off)}$		-	45	-	
Fall time	$t_f$		-	53	-	

## Gate Charge Characteristics<sup>2)</sup>

Gate to source charge	$Q_{gs}$	$V_{DD}=60\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	43	55	nC
Gate to drain charge	$Q_{gd}$		-	23	35	
Gate charge total	$Q_g$		-	111	145	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V

## Reverse Diode

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ °C}$	-	-	309	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	-	-	1150	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$	-	0.85	0.95	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=60\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	45	67	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	34	68	

<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

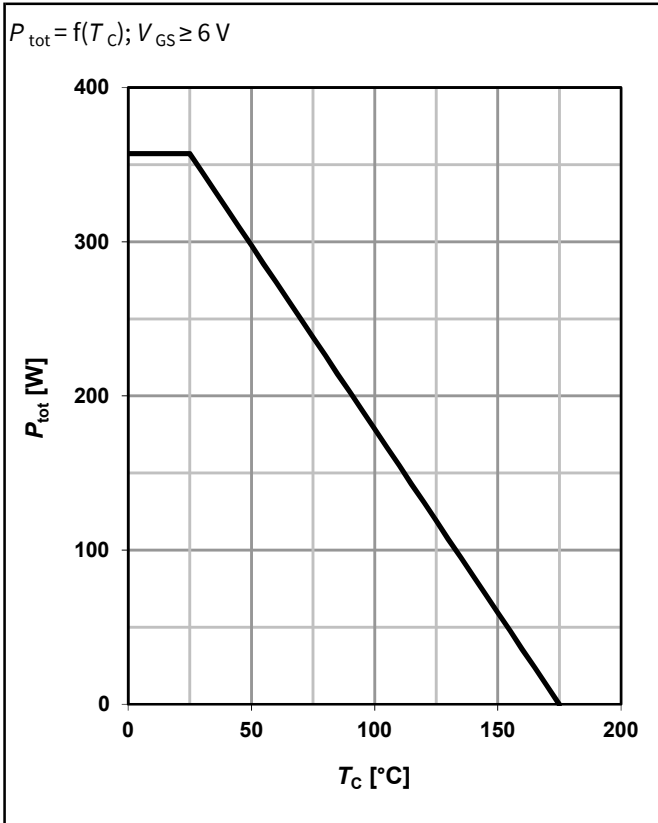
<sup>2)</sup> The parameter is not subject to production testing – specified by design.

<sup>3)</sup> Current is limited by chip.

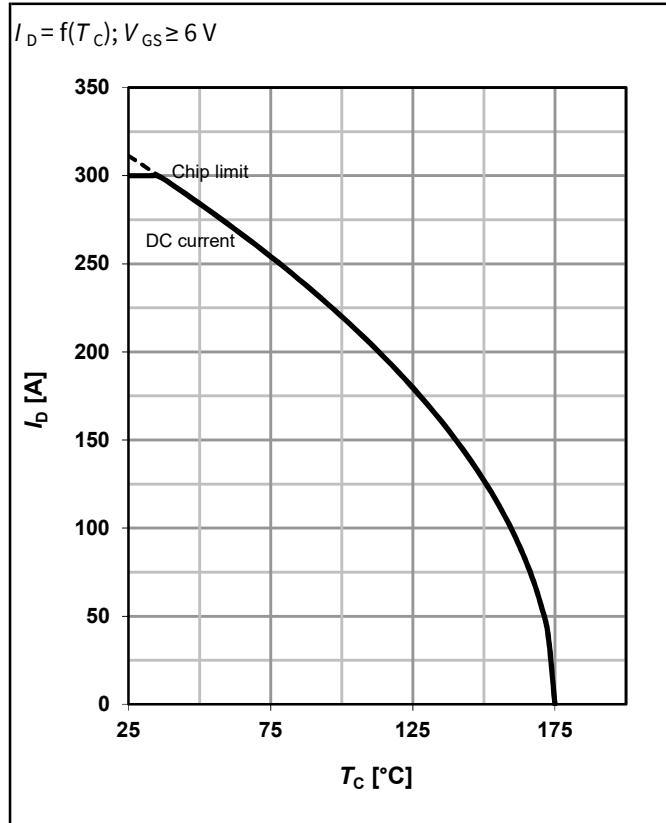
<sup>4)</sup> Device on a four-layer 2s2p FR4 PCB with topside cooling. Thermal insulation material is 100  $\mu\text{m}$  thick and has a conductivity of 0.7 W/m/K. Top surface of heat sink is fixed at ambient temperature. Bottom surface of PCB is left at free convection. Values may vary depending on the customer-specific design.

Electrical characteristics diagrams

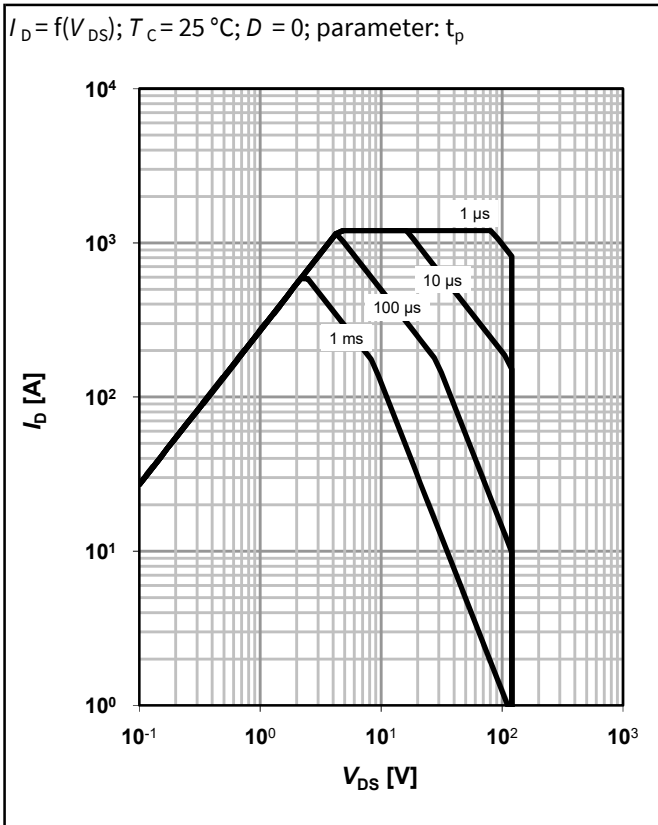
1 Power dissipation



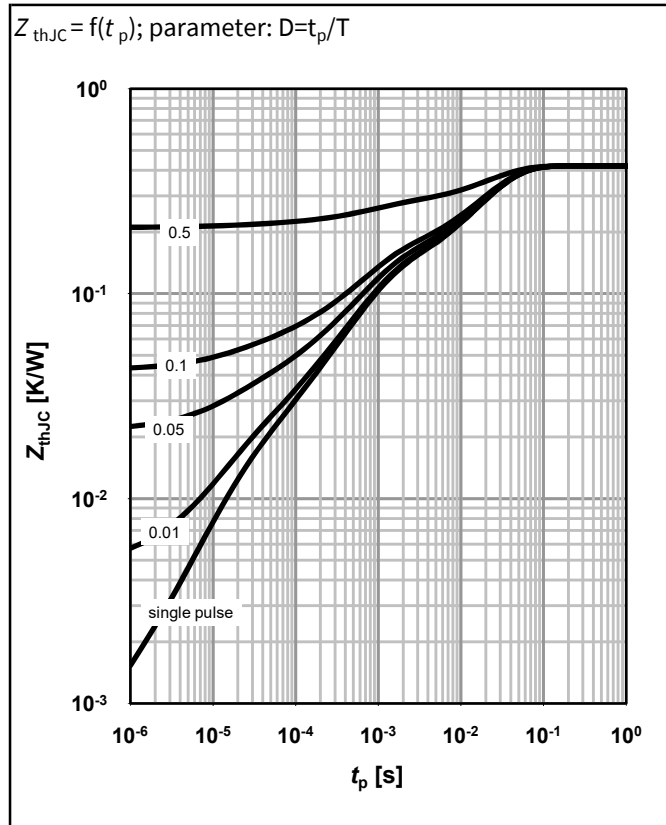
2 Drain current



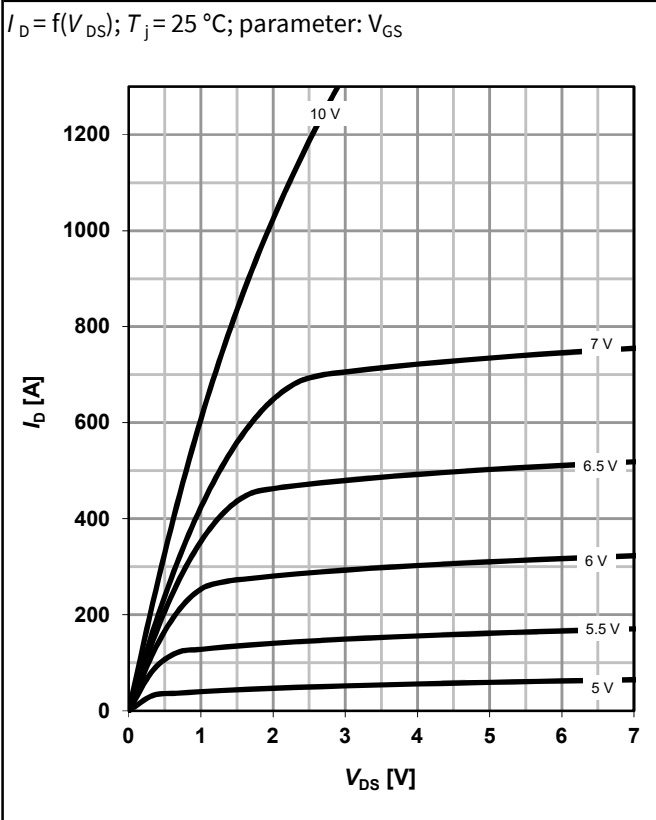
3 Safe operating area



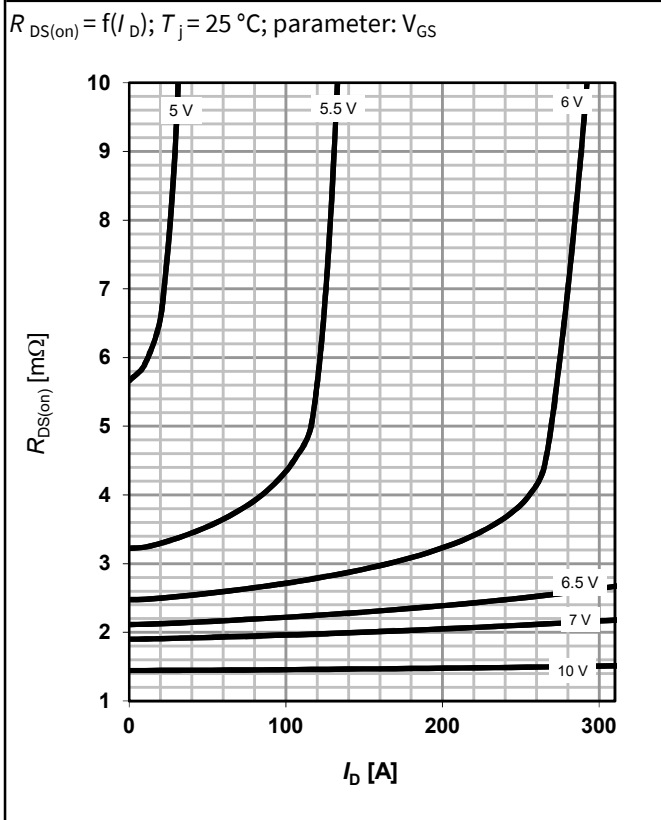
4 Max. transient thermal impedance



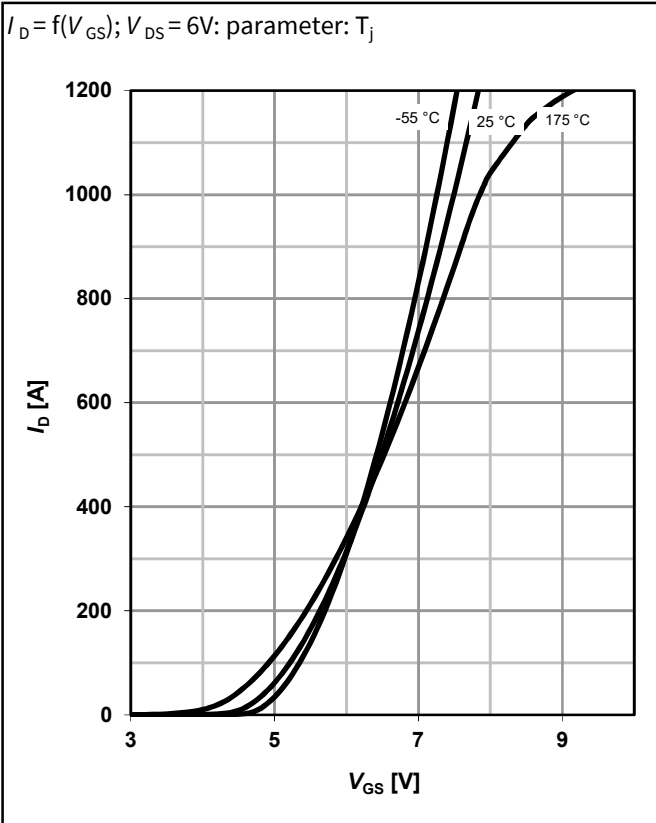
5 Typ. output characteristics



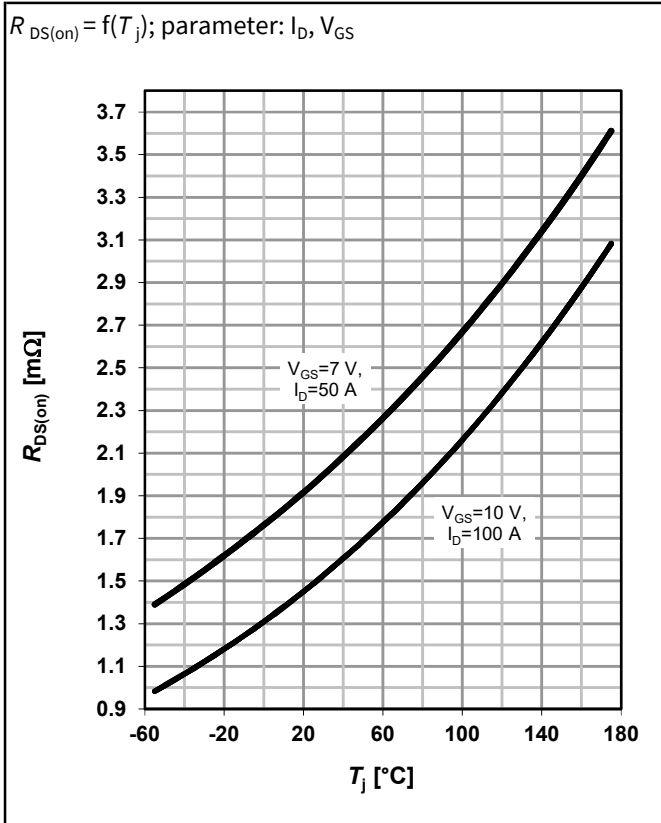
6 Typ. drain-source on-state resistance



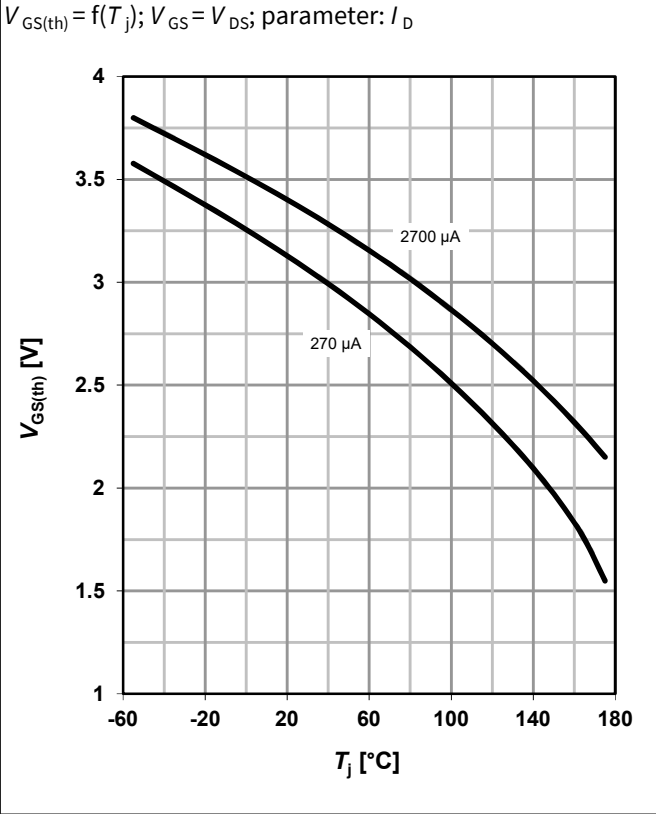
7 Typ. transfer characteristics



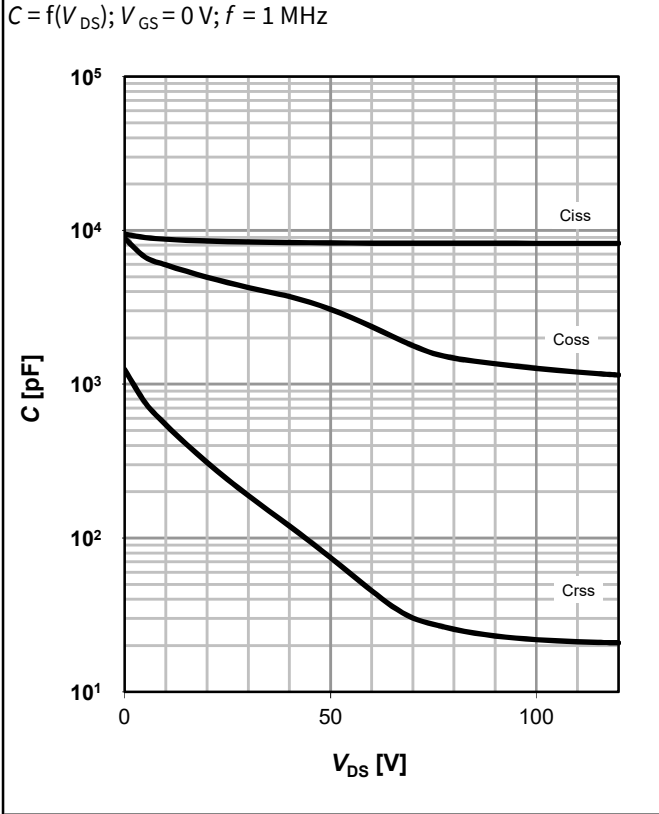
8 Typ. drain-source on-state resistance



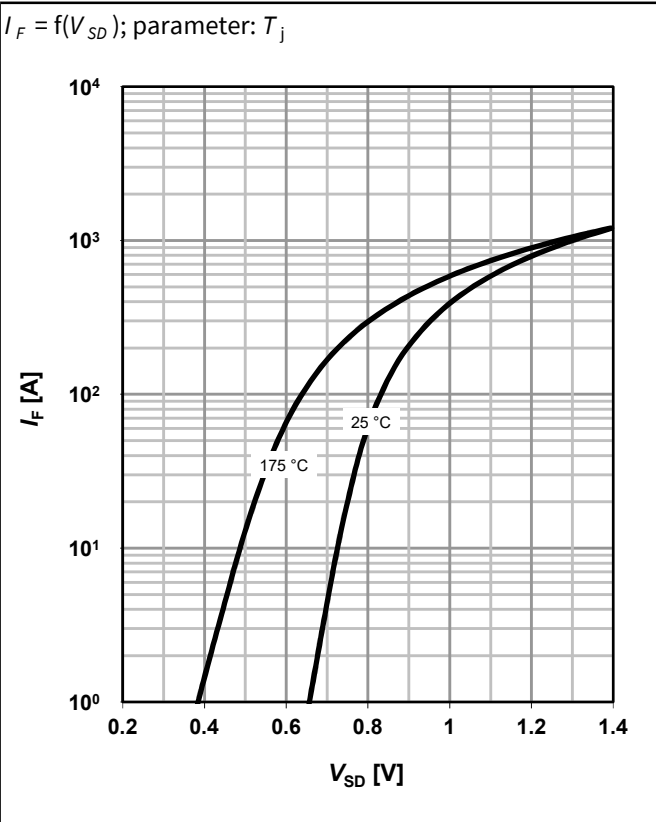
9 Typ. gate threshold voltage



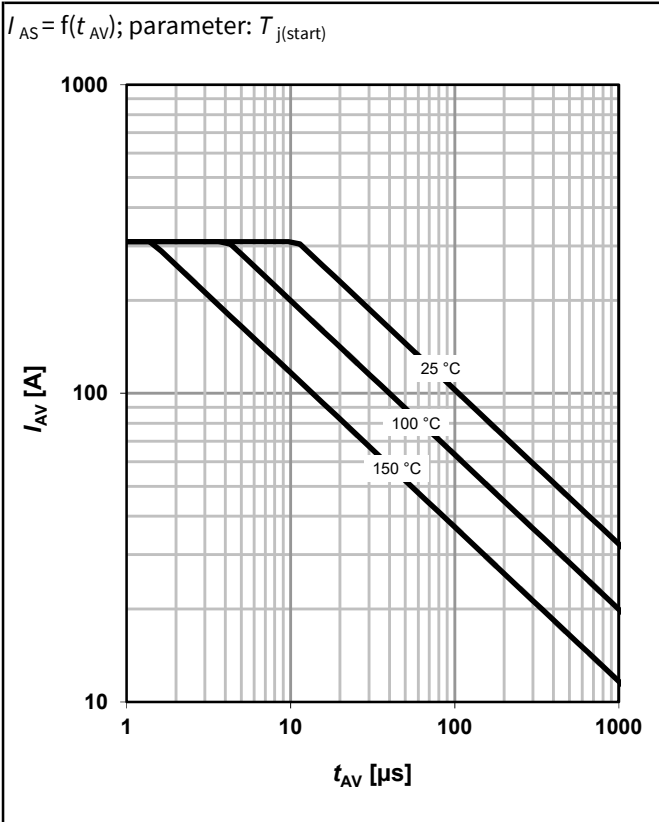
10 Typ. capacitances



11 Typical forward diode characteristics

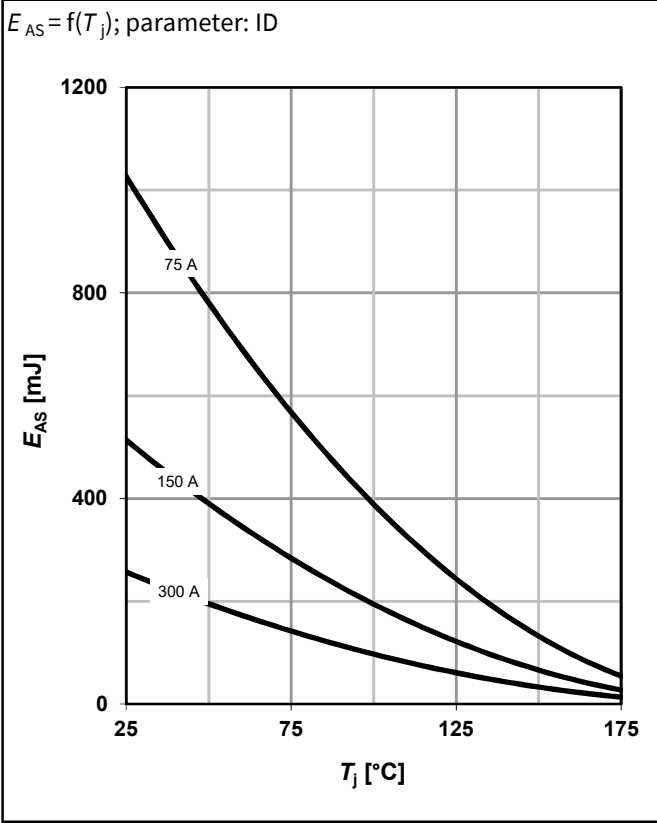


12 Typ. avalanche characteristics

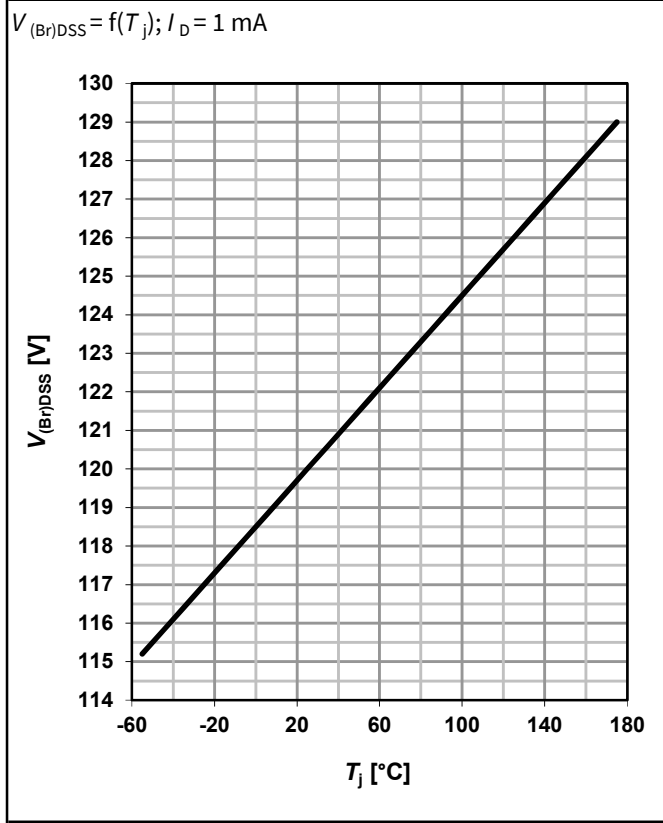




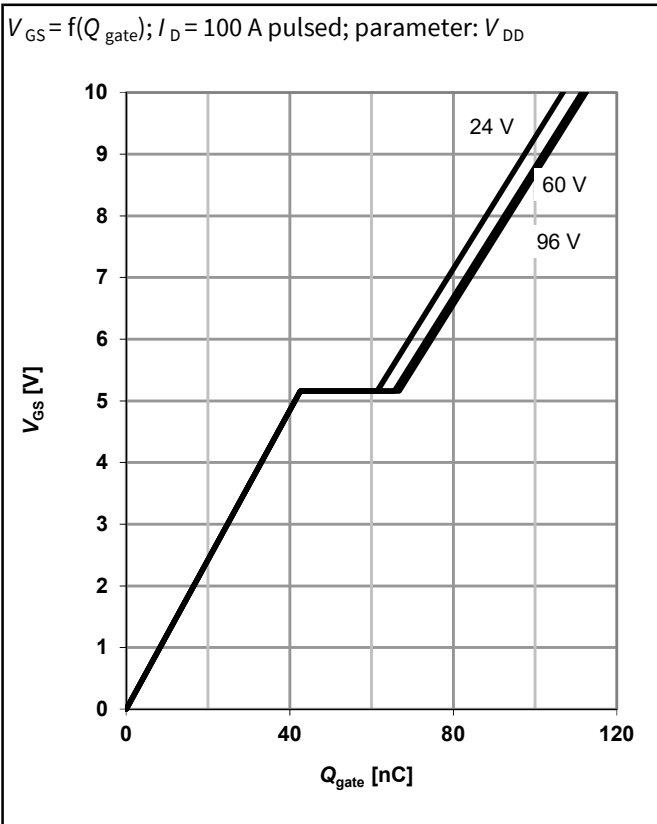
13 Typical avalanche energy



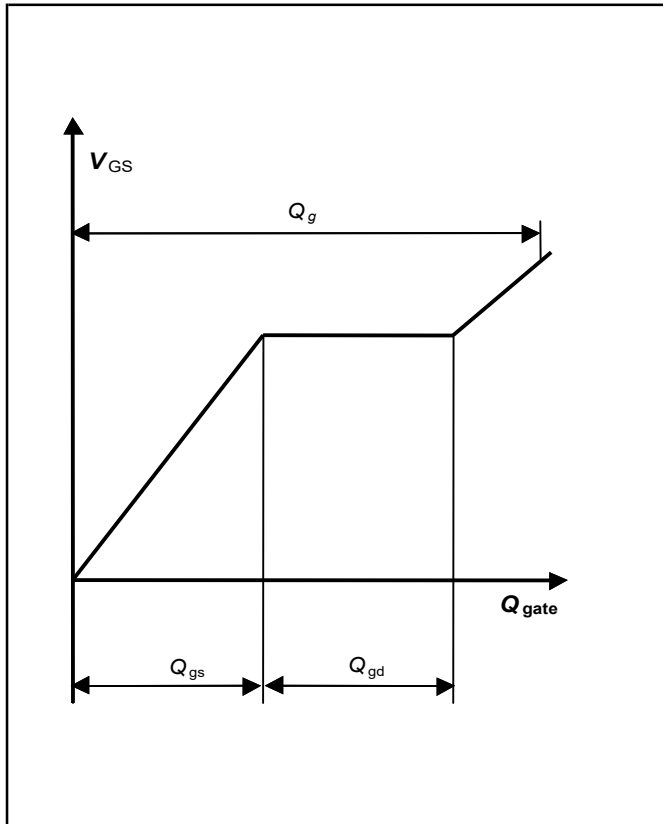
14 Drain-source breakdown voltage



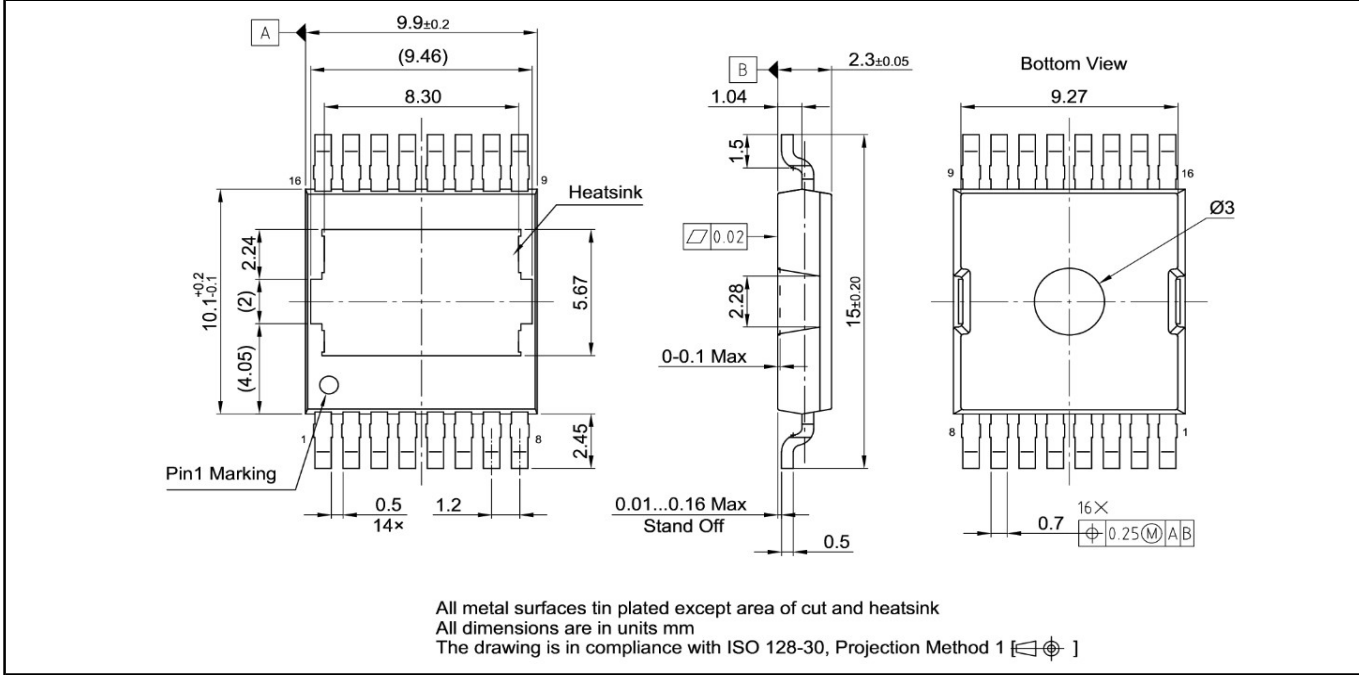
15 Typ. gate charge



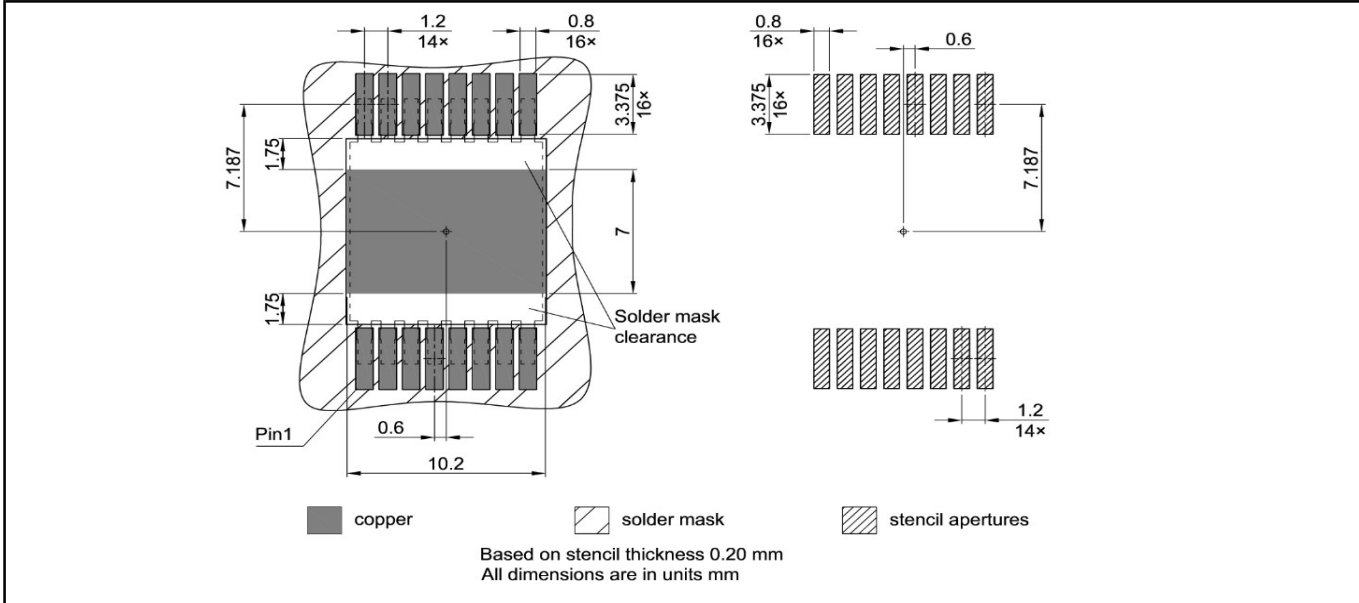
16 Gate charge waveforms



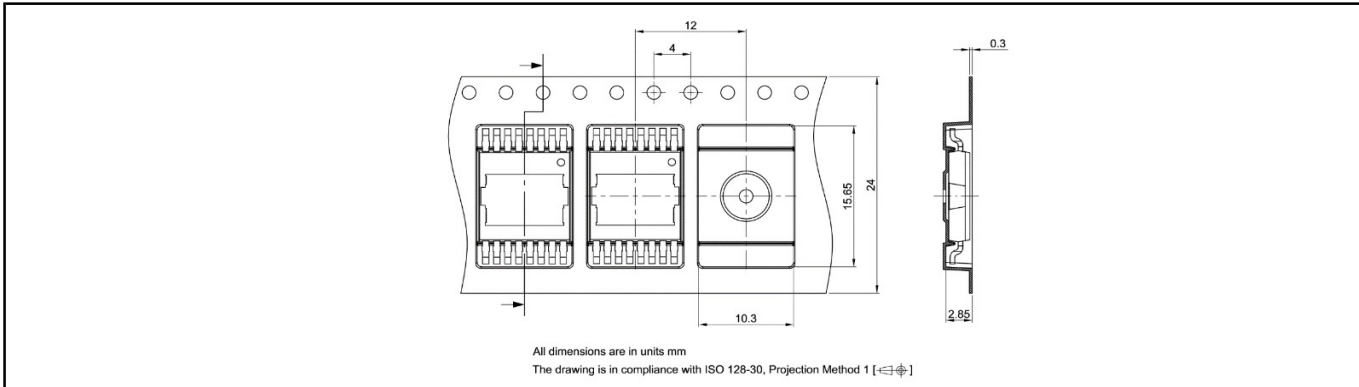
Package Outline



Footprint



Packaging



**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
Revision 1.0	2022-12-15	Final data sheet
Revision 1.01	2023-08-29	Reduced typical on-state resistance

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