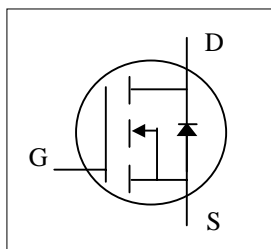


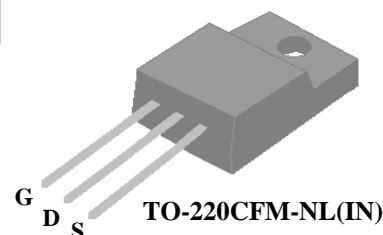
- ▼ 100% UIS Test
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free



$BV_{DSS}$	600V
$R_{DS(ON)}$	0.75 $\Omega$
$I_D^3$	10A

## Description

XP60AN750 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.



The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.

## Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	600	V
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	10	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	40	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	36.7	W
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	1.92	W
$E_{AS}$	Single Pulse Avalanche Energy <sup>4</sup>	32	mJ
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3.4	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	$^\circ\text{C}/\text{W}$

**Electrical Characteristics @ $T_j=25^{\circ}\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	600	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=5A$	-	-	0.75	$\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
$g_{fs}$	Forward Transconductance	$V_{DS}=20V, I_D=5A$	-	15	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=480V, V_{GS}=0V$	-	-	100	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	$\pm 1$	$\mu A$
$Q_g$	Total Gate Charge	$I_D=10A$	-	37	59.2	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=480V$	-	9	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	11	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=300V$	-	13	-	ns
$t_r$	Rise Time	$I_D=10A$	-	24	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=9.1\Omega$	-	48	-	ns
$t_f$	Fall Time	$V_{GS}=10V$	-	33	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	1680	2688	pF
$C_{oss}$	Output Capacitance	$V_{DS}=100V$	-	72	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	9	-	pF
$R_g$	Gate Resistance	$f=1.0\text{MHz}$	-	2.5	5	$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=5A, V_{GS}=0V$	-	-	1.5	V
$t_{rr}$	Reverse Recovery Time	$I_S=10A, V_{GS}=0V$	-	450	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	3.7	-	$\mu C$

**Notes:**

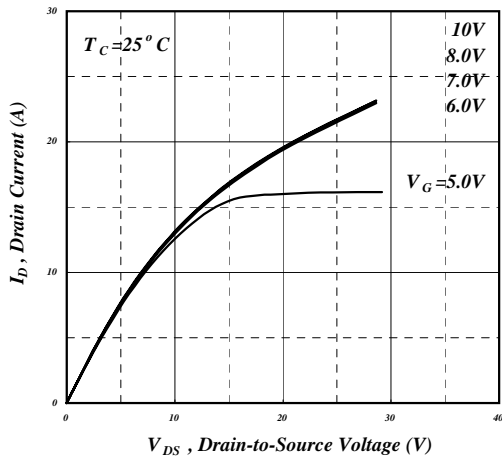
1. Pulse width limited by max. junction temperature.
2. Pulse test
3. Ensure that the junction temperature does not exceed  $T_{Jmax}$ .
4. Starting  $T_j=25^{\circ}\text{C}$ ,  $V_{DD}=90V$ ,  $L=1\text{mH}$ ,  $R_G=25\Omega$ ,  $V_{GS}=10V$

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

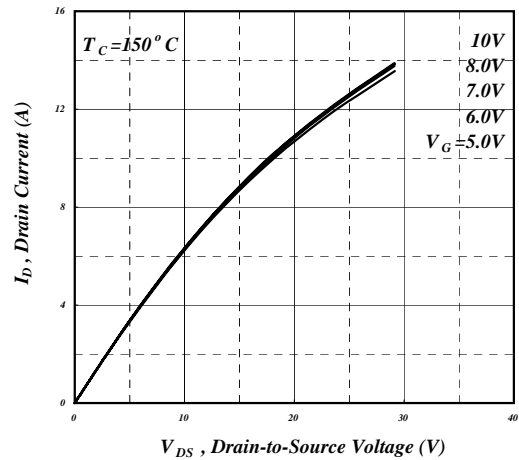
USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

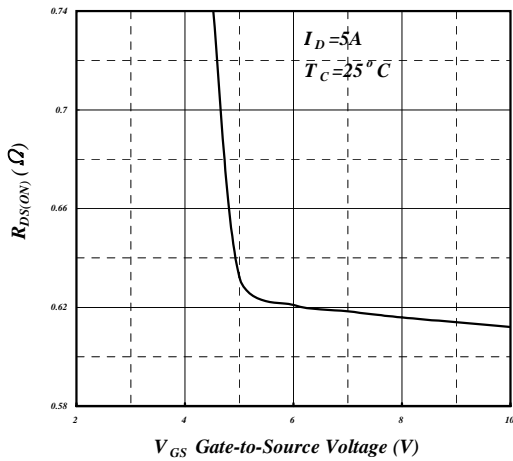
XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



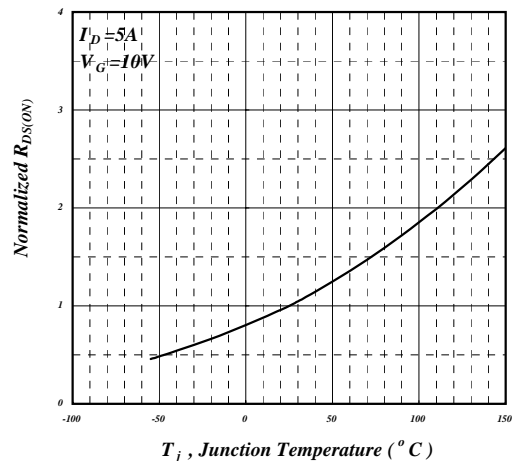
**Fig 1. Typical Output Characteristics**



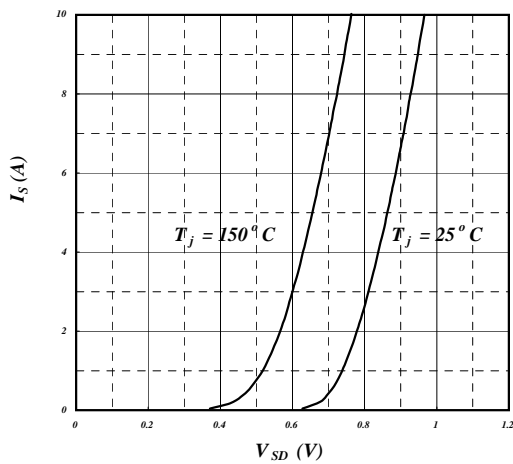
**Fig 2. Typical Output Characteristics**



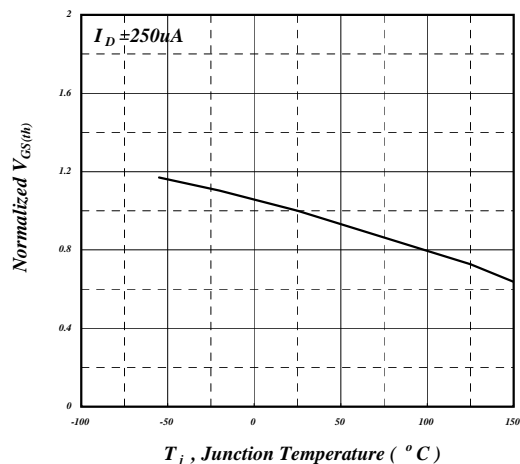
**Fig 3. On-Resistance v.s. Gate Voltage**



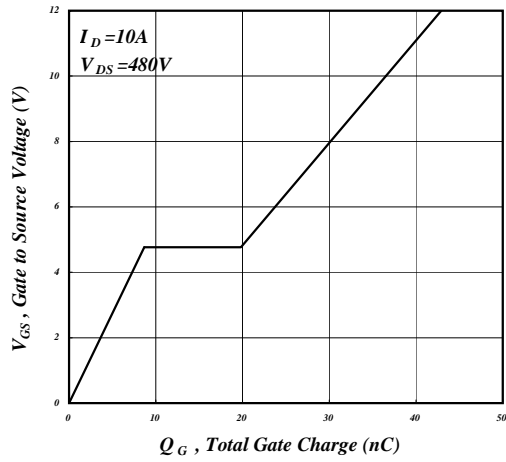
**Fig 4. Normalized On-Resistance v.s. Junction Temperature**



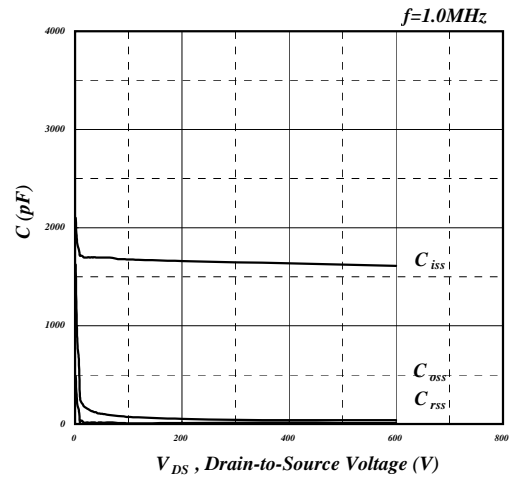
**Fig 5. Forward Characteristic of Reverse Diode**



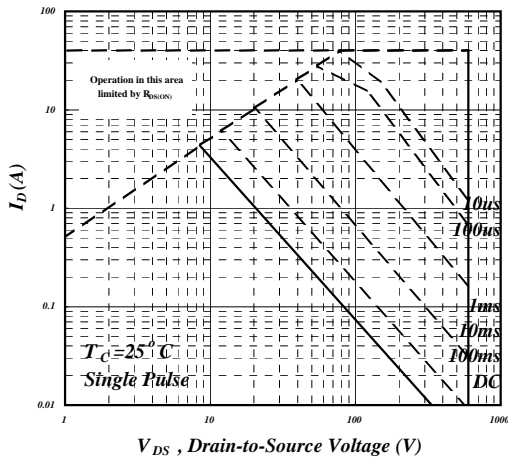
**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**



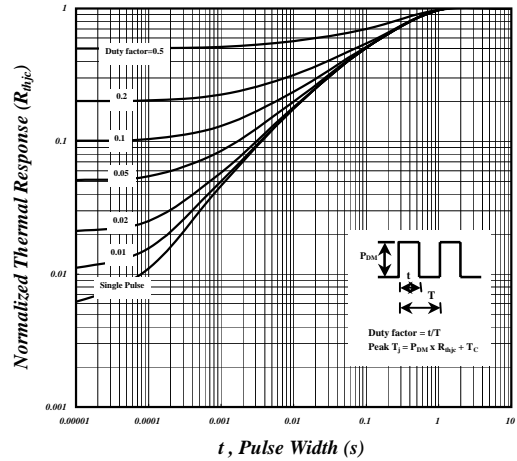
**Fig 7. Gate Charge Characteristics**



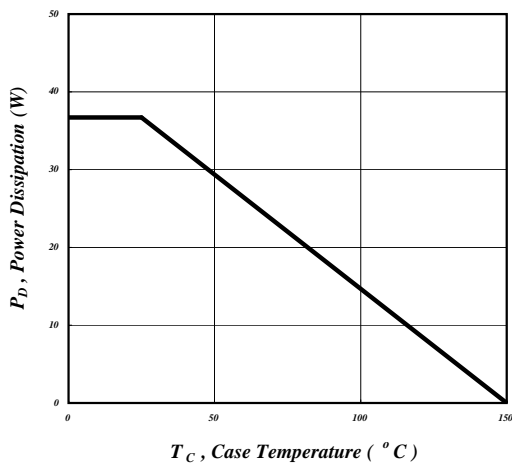
**Fig 8. Typical Capacitance Characteristics**



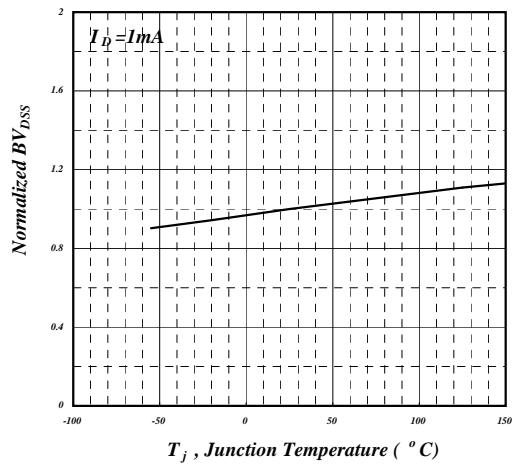
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**



**Fig 11. Total Power Dissipation**



**Fig 12. Normalized  $BV_{DS}$  v.s. Junction Temperature**

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**MARKING INFORMATION**

