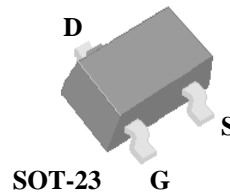


- ▼ Simple Drive Requirement
- ▼ Small Package Outline
- ▼ ESD Diode Protected
- ▼ RoHS Compliant & Halogen-Free

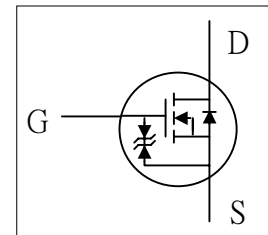


BV_{DSS}	600V
$R_{DS(ON)}$	72 Ω
I_D	53mA
HBM ESD	2KV

Description

XP60PN72 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The special design SOT-23 package with good thermal performance is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for voltage conversion or switch applications.



Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A=25^\circ\text{C}$	Drain Current ³ , V_{GS} @ 10V	53	mA
$I_D @ T_A=70^\circ\text{C}$	Drain Current ³ , V_{GS} @ 10V	43	mA
I_{DM}	Pulsed Drain Current ¹	300	mA
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	0.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	250	$^\circ\text{C}/\text{W}$

Electrical Characteristics @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	600	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =50mA	-	-	72	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	5	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =50mA	-	200	-	mS
I _{DSS}	Drain-Source Leakage Current	V _{DS} =480V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±30	uA
Q _g	Total Gate Charge ²	I _D =0.1A	-	2.5	4	nC
Q _{gs}	Gate-Source Charge	V _{DS} =200V	-	1	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	0.3	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =300V	-	10	-	ns
t _r	Rise Time	I _D =50mA	-	8	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	14	-	ns
t _f	Fall Time	V _{GS} =10V	-	77	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	50	80	pF
C _{oss}	Output Capacitance	V _{DS} =100V	-	9	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	5	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =0.05A, V _{GS} =0V	-	-	1.5	V

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Mounted on min. copper pad FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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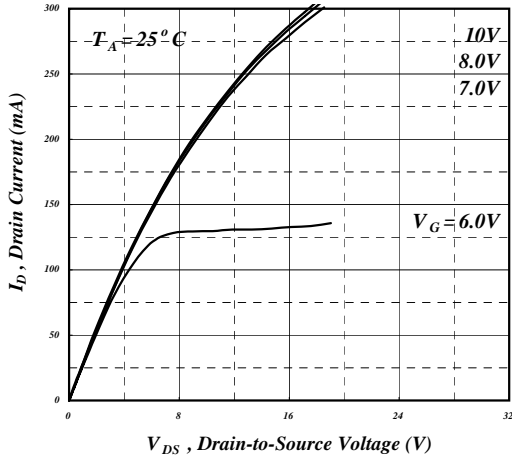


Fig 1. Typical Output Characteristics

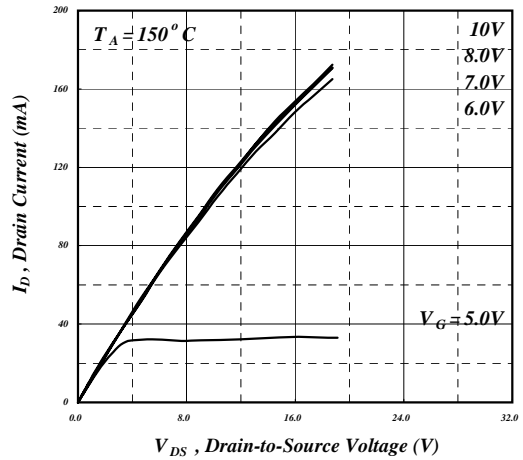


Fig 2. Typical Output Characteristics

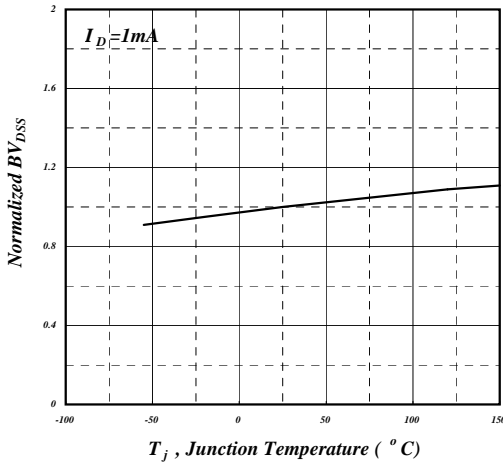


Fig 3. Normalized BV_{DS} v.s. Junction Temperature

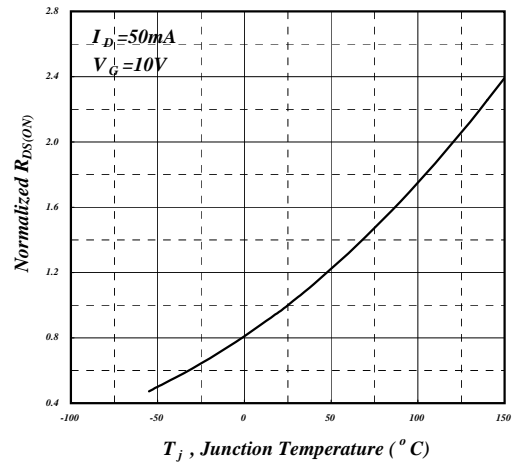


Fig 4. Normalized On-Resistance v.s. Junction Temperature

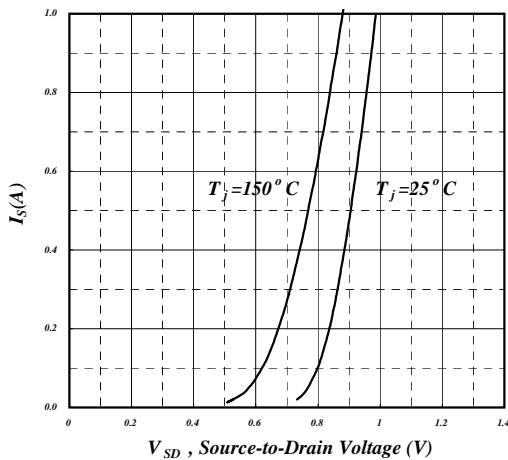


Fig 5. Forward Characteristic of Reverse Diode

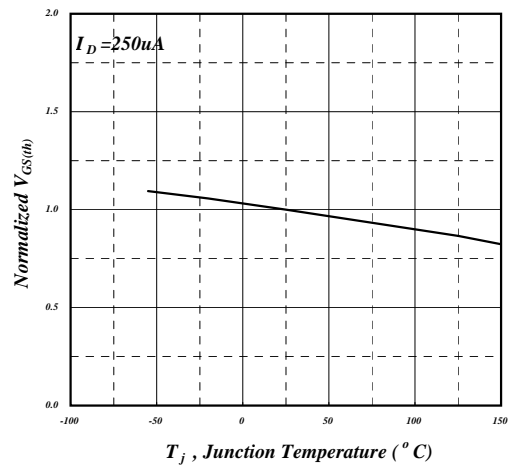


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

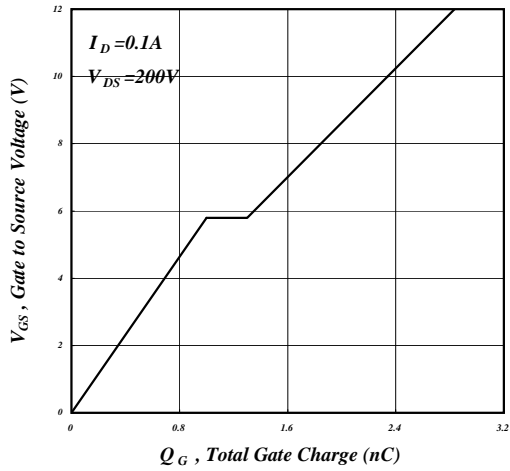


Fig 7. Gate Charge Characteristics

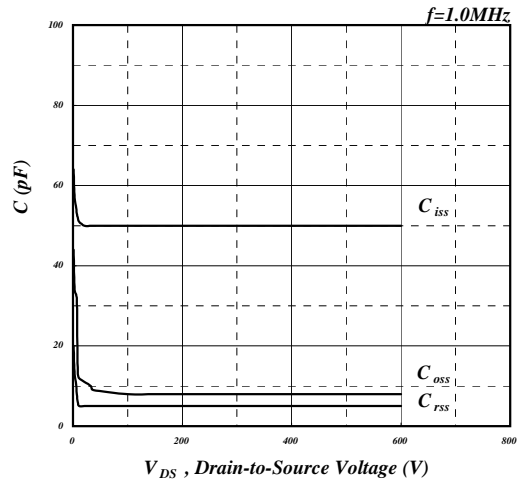


Fig 8. Typical Capacitance Characteristics

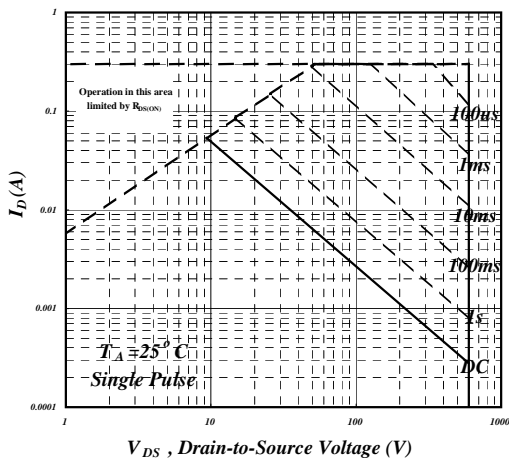


Fig 9. Maximum Safe Operating Area

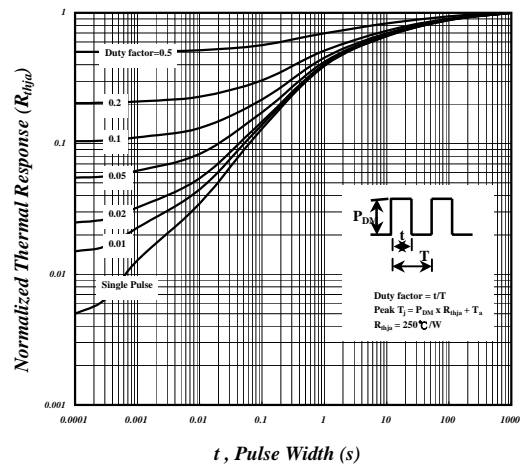


Fig 10. Effective Transient Thermal Impedance

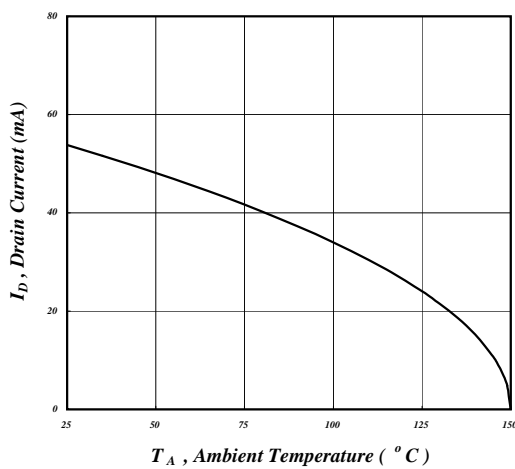


Fig 11. Drain Current v.s. Ambient Temperature

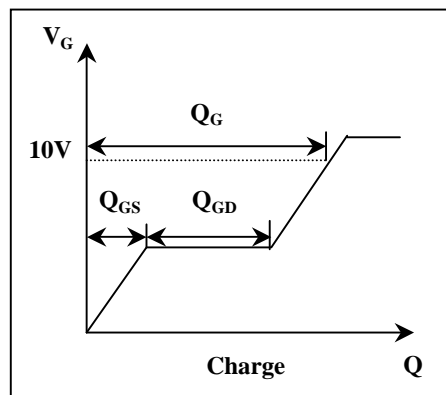
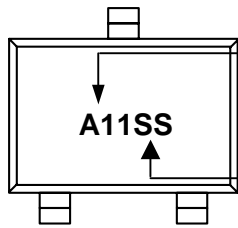


Fig 12. Gate Charge Circuit

MARKING INFORMATION



Part Number : A11

Date Code : SS

SS:2004,2008,2012,2016,2020,2024...

SS:2003,2007,2011,2015,2019,2023...

SS:2002,2006,2010,2014,2018,2022...

SS:2001,2005,2009,2013,2017,2021...