# Evaluating the AD4858 8-Channel Simultaneous Sampling, 20-Bit 1 MSPS Data Acquisition System

## FEATURES

- Full featured evaluation board for the AD4858
- Eight input channels available through SMA connectors
- On-board reference circuit and power supplies
- Standalone capability through FMC connector and/or test points
- PC software for control and data analysis of the time and frequency domain
- ZedBoard-compatible
- Compatible with other FMC controller boards

## EQUIPMENT NEEDED

- PC running Windows® 10 operating system or higher
- Digilent ZedBoard with 12 V wall adapter power supply
- Precision signal source
- SMA cables (inputs to evaluation board)
- USB cable

## SOFTWARE NEEDED

- ACE evaluation software
- AD4858 ACE plugin from plug-in manager

## GENERAL DESCRIPTION

The EVAL-AD4858FMCZ is designed to demonstrate the performance of the AD4858 and provide access to many included configuration options that are accessed via an easy to use ACE plug-in graphical interface. The AD4858 is a fully buffered, 8-channel simultaneous sampling, 20-bit, 1 MSPS data acquisition system (DAS) with differential, wide common mode range inputs.

The EVAL-AD4858FMCZ on-board components include also the following:

- The LTC6655 high precision, low drift, 4.096 V voltage reference (not used by default)
- The LT1761, low noise, 1.8 V, 2.5 V, and 5 V low dropouts (LDOs)
- The LT8330 low quiescent current ($I_Q$) boost converter

For full details on the AD4858, see the AD4858 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-AD4858FMCZ.

## EVALUATION BOARD KIT CONTENTS

- EVAL-AD4858FMCZ evaluation board
- Micro-SD memory card (with adapter) containing system board boot software and Linux OS

## EVALUATION BOARD PHOTOGRAPH

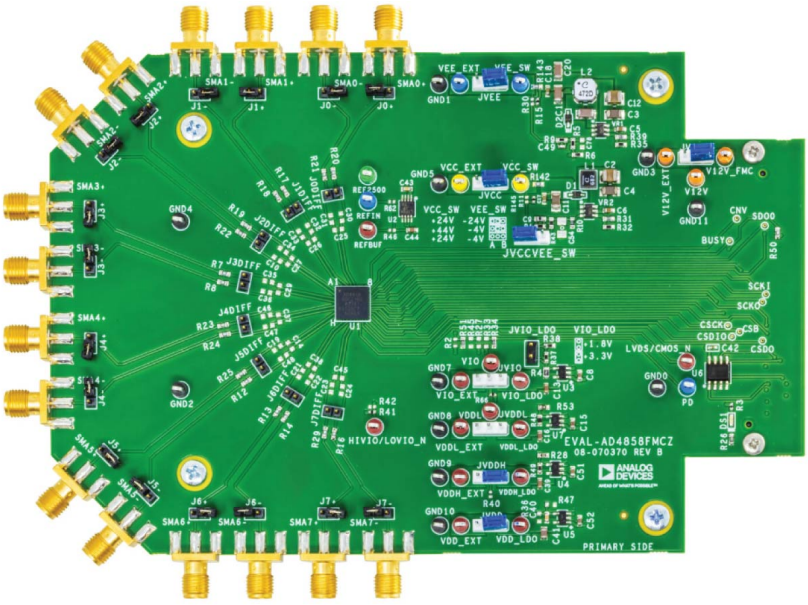


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*Figure 1. Evaluation Board Photograph*

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## REVISION HISTORY

**10/2023—Revision 0: Initial Version**

## QUICK START GUIDE

1. Download and install the ACE Software tool from the ACE download page, as per the Installing the ACE Evaluation Software section. If ACE is already installed, make sure you have the latest version by using **Check For Updates** option in the ACE sidebar, as shown in Figure 2.

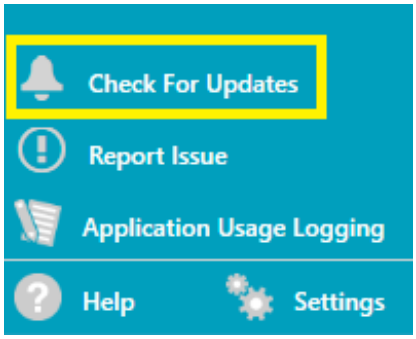


*Figure 2. Check For Updates Option in the ACE Sidebar*

2. Run the **ACE** software and select **Plug-in Manager** from the ACE sidebar to install the board plug-in that supports the product evaluation board and select **Available Packages**, as shown in Figure 3. You can use the search field to help filter the list of boards to find the relevant one. An ACE quickstart guide is available here at ACE Quickstart - Using ACE and Installing Plug-ins.

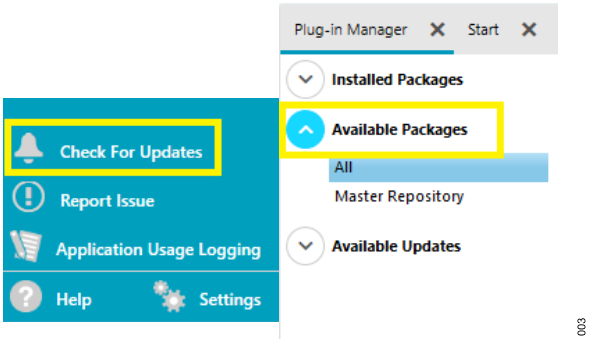


*Figure 3. Plug-in Manager Option in the Sidebar*

3. Insert the SD card into the SD card slot on the underside of the ZedBoard. If there is a need to reimage or create a new SD card, instructions are available at the following website: ADI Kuiper Linux with support for ACE Evaluation.
4. Ensure the ZedBoard boot configuration jumpers are set to use the SD card as shown in Figure 4. To avoid potential damage, ensure the VADJ SELECT jumper is set to the correct voltage for the EVAL-AD4858FMCZ.

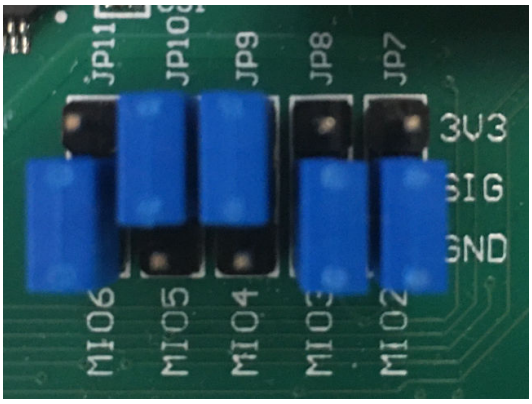


*Figure 4. ZedBoard Boot Configuration Jumpers*

5. Connect the AD4858 evaluation board to the FMC connector on the ZedBoard.
6. Connect the USB cable from the PC to the J13/USB OTG port, and connect the 12 V power supply to J20/DC input.
7. Slide the SW8/POWER switch in the ZedBoard to the on position. The green LD13/POWER LED turns on and is followed by the blue LD12/DONE LED (within the ZedBoard). The DS1 LED in the EVAL-AD4858FMCZ will also turn on.
8. The red LD7 LED blinks approximately 20 to 30 seconds later, indicating the boot process is complete.
9. Launch the **ACE software** from the **Analog Devices** folder in the **Windows Start** menu. The evaluation board appears on the **ACE Start** tab in the **Attached Hardware** view.

## EVALUATION BOARD HARDWARE

The AD4858 is a fully buffered, 8-channel simultaneous sampling, 20-bit 1 MSPS DAS with differential, wide common mode range inputs. The AD4858 has an on-chip low drift 4.096 V internal voltage reference, but, optionally, it also accepts an external reference applied through the REFIO pin and provided on-board (LTC6655). The device operates from different power rails, provided through on-board LDOs as described in Power Supplies section. An option to connect external supplies exists and is explained in Table 1.

### HARDWARE LINK OPTIONS

Table 1 details the link option functions and the default power link options. The EVAL-AD4858FMCZ can be powered from different sources, as described in the Power Supplies section. By default, the power supply required for the EVAL-AD4858FMCZ comes from the ZedBoard controller board. The power supply is regulated by the on-board regulators that generate the required bipolar supplies.

***Table 1. Jumper Details with Factory Default Setting***

| Link | Default Position | Function |
|---|---|---|
| JODIFF to J7DIFF | Not inserted | Offset Calibration Jumper. Inserting the JODIFF to J7DIFF jumper link allows short-circuiting the corresponding pair of inputs in order to measure the AD4858 offset and/or perform and offset calibration. |
| J0+ to J7+ | Not inserted | Analog Input to Ground Connection. Insert the J0+ to J7+ jumper link to connect to the AGND pin, the corresponding positive analog input. |
| J0− to J7− | Not inserted | Analog Input to Ground Connection. Insert the J0− to J7− jumper link to connect to the AGND pin, the corresponding negative analog input. |
| JV12V | A | The JV12V link selects the power supply source for the evaluation board.<br>In Position A, the unregulated supply to the on-board LDOs is taken from the ZedBoard 12 V supply.<br>In Position B, the unregulated external supply to the on-board LDOs is taken from the V12V_EXT connector. |
| JSHIFT | A | The JSHIFT link selects the power supply type for the AD4858.<br>In position A, the $V_{CC}$ pin = +24 V and the $V_{EE}$ pin = −24 V.<br>In position B, the $V_{CC}$pin = +44 V and the $V_{EE}$ pin = −4 V.<br>If not inserted, the $V_{CC}$ pin = +24 V and the $V_{EE}$ pin = −4 V. |
| JVCC | A | The JVCC link selects the $V_{CC}$ pin supply source.<br>In position A, the $V_{CC}$ pin is provided by the on board LT8330 DC/DC converter.<br>In position B, the $V_{CC}$ pin is provided though VCC_EXT connector. |
| JVEE | A | The JVEE link selects the $V_{EE}$ pin supply source.<br>In position A, the $V_{EE}$ pin is provided by the on board LT8330 DC-to-DC converter.<br>In position B, the $V_{EE}$ pin is provided though VEE_EXT connector. |
| JVDDH | A | The JVDDH link selects the $V_{DDH}$ pin supply source.<br>In position A, the $V_{DDH}$ pin is provided by the on board LT1761 2.5 V LDO.<br>In position B, the $V_{DDH}$ pin is provided though VDDH_EXT connector.<br>If not inserted, $V_{DDH}$ pin can be tied to the AGND pin by inserting an R40 resistor. To disable the internal LDO, tie the $V_{DDH}$ pin to the GND pin. With the regulator disabled, connect the $V_{DDL}$ pin to an external supply in the range of 1.71 V to 1.89 V through the JVDDL link. |
| JVDD | A | The JVDD link selects the $V_{DD}$ pin supply source.<br>In position A, the $V_{DD}$ pin is provided by the on board LT1761 5 V LDO.<br>In position B, the $V_{DD}$ pin is provided though VDD_EXT connector. |
| JVDDL | Not inserted | The JVDDL link selects the $V_{DDL}$ pin supply source.<br>In position A, the $V_{DDL}$ pin is provided by the on-board LT1761 1.8 V LDO. To use this configuration, tie the $V_{DDH}$ pin to ground through the JVDDH link.<br>In position B, the $V_{DDL}$ pin is provided though the VDDL_EXT connector. To use this configuration, tie the $V_{DDH}$ pin to ground through the JVDDH link.<br>If not inserted, the internal LDO is used for the JVDDH link to be in position A or B. |
| JVIO | Not inserted | The JVIO link selects the $V_{IO}$ pin supply source. If not inserted, the $V_{IO}$ pin is taken from the ZedBoard (default). Alternatively, the $V_{IO}$ pin can be supplied from either the on-board LDOs or an external supply.<br>In position A, the $V_{IO}$ pin is provided by the on board LT1761 LDO with an output voltage dependent on the JVIO_LDO link. The R66 resistor (shown in Figure 20) is unsoldered.<br>In position B, the $V_{IO}$ pin is provided though VIO_EXT connector. The R66 resistor is unsoldered.<br>Note the field programmable gate array (FPGA) image provided works at 2.5 V digital level, so use caution when changing the default position of the JVIO link jumper. |

## EVALUATION BOARD HARDWARE

*Table 1. Jumper Details with Factory Default Setting (Continued)*

| Link | Default Position | Function |
|---|---|---|
| JVIO_LDO | Not inserted | The JVIO_LDO link selects the LT1761 LDO output voltage when the JVIO link is in position B.<br>Inserted, the LT1761 output voltage is 3.3 V.<br>Not inserted, the LT1761 output voltage is 1.8 V. |

## EVALUATION BOARD HARDWARE

### CONNECTORS AND SOCKETS

The connectors and sockets on the EVAL-AD4858FMCZ are outlined in Table 2.

*Table 2. On-Board Connectors*

| Connector | Function |
|---|---|
| SMA0+ to SMA7+ | Positive analog input subminiature version A (SMA) to Channel 0 through Channel 7 |
| SMA0− to SMA7− | Negative analog input SMA to Channel 0 through Channel 7 |
| P1 | FPGA mezzanine card (FMC) connector |

### POWER SUPPLIES

The ZedBoard supplies 12 V to power the rails for the different components on the EVAL-AD4858FMCZ. The AD4858 uses the following five power supply pins:

- Positive high voltage power supply ( the $V_{CC}$ pin)
- Negative high voltage power supply (the $V_{EE}$ pin)
- Low voltage power supply (the $V_{DD}$ pin)
- 1.8 V power supply (the $V_{DDL}$ pin)
- Digital power supply (the $V_{IO}$ pin)

A combination of the LT8330 DC-to-DC converter and the LT1761 LDO generate all the needed supply rails on the board.

*Table 3. Default Power Supplies Available in EVAL-AD4858FMCZ*

| Power Supply (V) | Function | Component |
|---|---|---|
| +24 | $V_{CC}$ | LT8330 |
| −24 | $V_{EE}$ | LT8330 |
| +2.5 | $V_{DDH}$ | LT1761 |
| +5 | $V_{DD}$ | LT1761 |
| +1.8 | $V_{IO}$ | LT1761 |

### REFERENCE CIRCUIT

By default, the AD4858 in the EVAL-AD4858FMCZ uses the internal low noise, low drift (10 ppm/°C maximum), temperature compensated bandgap reference that is factory trimmed to 4.096 V and the internal reference buffer.

As an optional alternative, anLTC6655 high precision, low drift (2 ppm/°C maximum), 4.096 V voltage reference is also provided. This external reference can be used in two different configurations, as explained in the AD4858 data sheet and as follows:

- External reference with internal buffer. For this configuration, connect the external reference to the REFIO pin and populate the resistor R62 shown in Figure 20.
- External reference with disabled internal buffer. For this configuration, connect the external reference to the REFBUF pin and populate the resistor R46 shown in Figure 20 , and also connect the REFIO test point to ground.

## EVALUATION BOARD SOFTWARE

### SOFTWARE INSTALLATION PROCEDURE

Download the ACE evaluation software from the EVAL-AD4858FMCZ evaluation kit page. Install the software on a PC before using the EVAL-AD4858FMCZ kit. Download the AD4858 ACE plug-in from the EVAL-AD4858FMCZ page or from the plug-in manager in ACE.

Perform the following steps to complete the installation process:

1. Install the ACE evaluation software.
2. Install the AD4858 plug-in. The ACE Quickstart page shows the plug-in installation guide.

#### Warning

Install the ACE software before connecting the EVAL-AD4858FMCZ and ZedBoard to the PC's USB port to ensure that the evaluation system is properly recognized when it is connected.

#### Installing the ACE Evaluation Software

To install the ACE evaluation software, take the following steps:

1. Download the ACE software to a Windows-based PC.
2. Double click the **ACEInstall.exe** file to begin the installation. By default, the ACE software is saved to the following location: **C:\Program Files (x86)\Analog Devices\ACE**.
3. A dialog box opens asking for permission to allow the program to make changes to the PC. Click **Yes** to start the installation process.
4. In the **ACE Setup** window, click **Next >** to continue the installation.

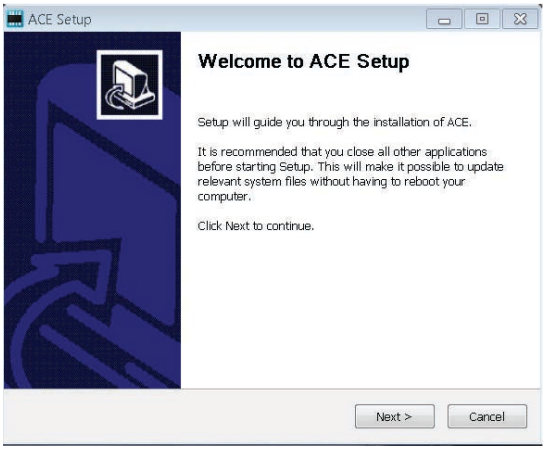


*Figure 5. Evaluation Software Install Confirmation*

5. Read the software license agreement and click **I Agree**.


*Figure 6. License Agreement*

6. Click **Browse...** to choose the installation location and then click **Next >** .

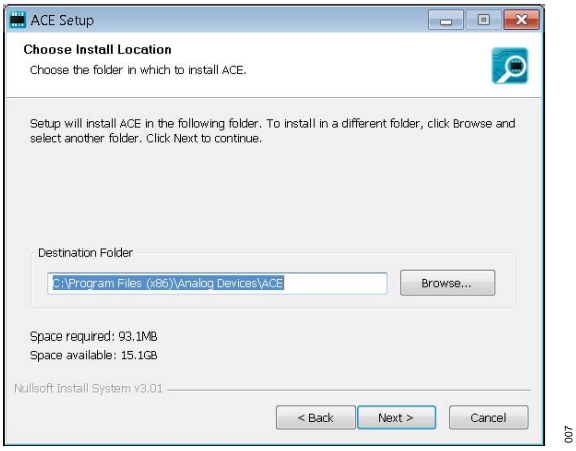


*Figure 7. Choose Install Location Window*

7. The ACE software components to install are preselected. Click **Install** .

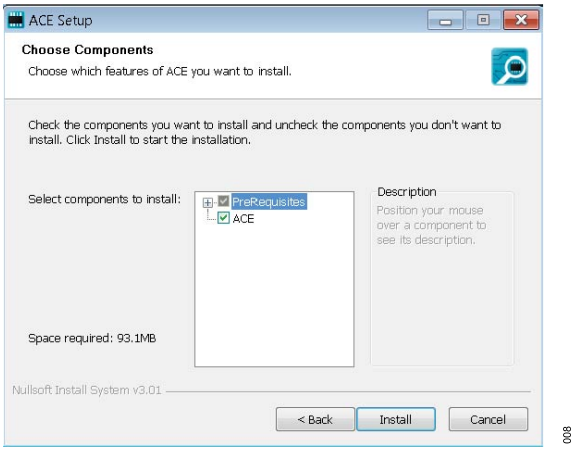


*Figure 8. Choose Components*

8. The **Windows Security** window opens . Click **Install**. No action is required.

## EVALUATION BOARD SOFTWARE


*Figure 9. Windows Security Window*

**9.** The installation is in progress. No action required.

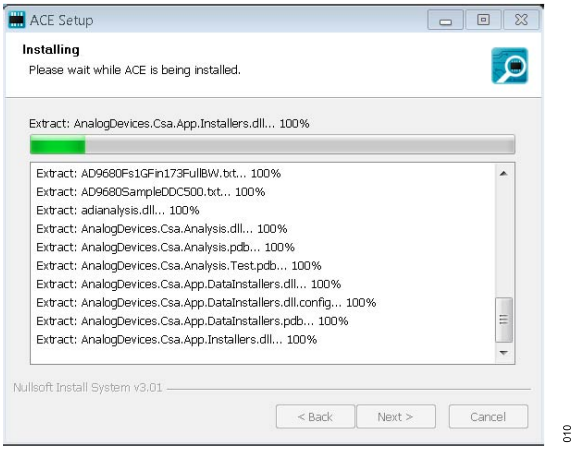


*Figure 10. Installation in Progress*

**10.** When the installation completes, click **Next >** , and then click **Finish**.

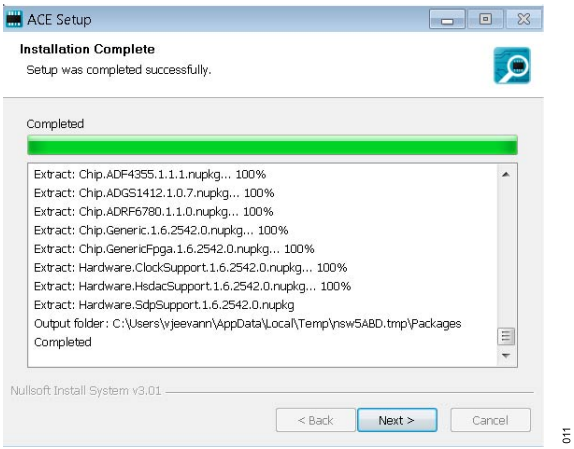


*Figure 11. Installation complete*

### Disconnecting the EVAL-AD4858FMCZ

Always disconnect power from the ZedBoard, through the SW8/ POWER switch, before disconnecting the EVAL-AD4858FMCZ from the FMC connector.

## ACE SOFTWARE OPERATION

### LAUNCHING THE SOFTWARE

To start the ACE evaluation software, open the Windows **Start** menu and click **Analog Devices > ACE**. The software window continues loading until the software recognizes the AD4858 evaluation board. When the software recognizes the board, double-click on the icon in the **Start** view to open the main window seen in Figure 12. For more detailed information about ACE, refer to the ACE user guide (Analysis | Control | Evaluation - ACE Software).

Note the **Power** yellow LED (LD13) and the **Done** blue LED (LD12) are turned on.

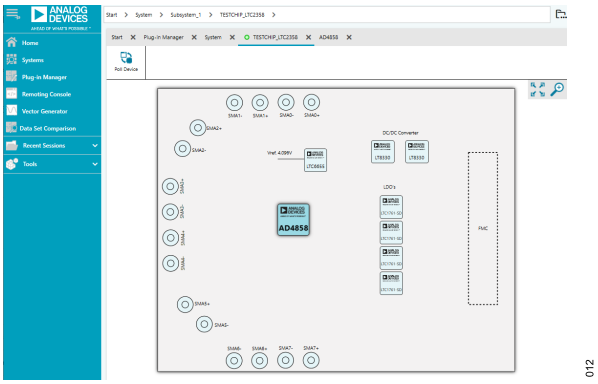


*Figure 12. Board View*

### Chip View

Hover over the AD4858 symbol in the **Board View** and double click to enter the **Chip View** (Figure 13).

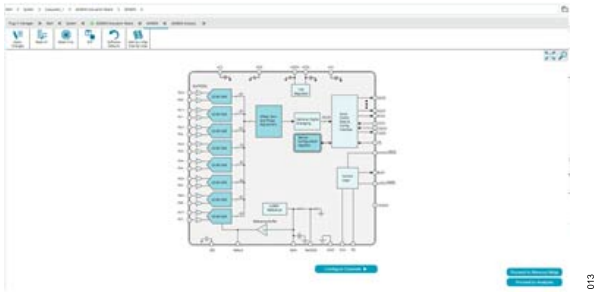


*Figure 13. Chip View*

In this view, you can configure the AD4858 per channel SoftSpan , offset, gain, and phase values by left or right clicking the dark blue symbols (see Figure 14 and Figure 15) by choosing the appropriate field from a drop-down window.

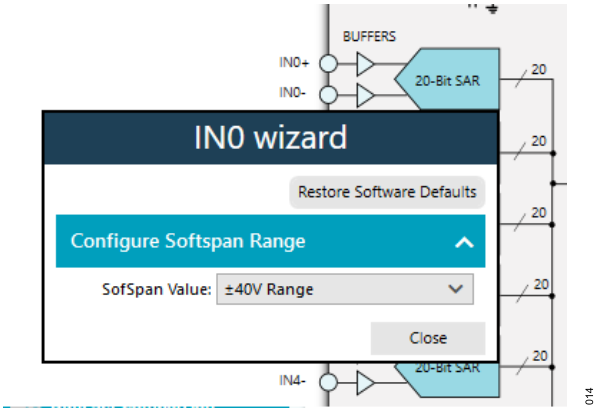


*Figure 14. Setting the Per Channel SoftSpan Range*

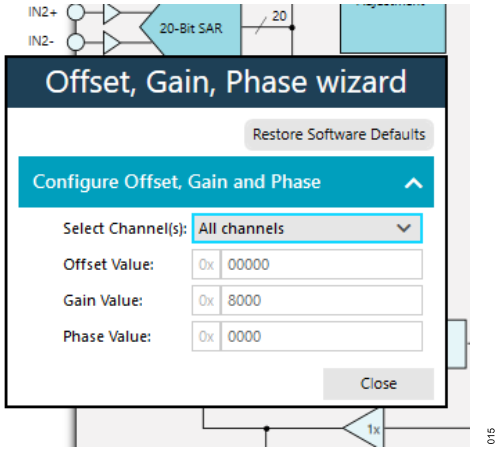


*Figure 15. Setting the Per Channel Offset, Gain and Phase*

Selecting the **Configure Channels** button allows for a global configuration of the channel settings while the **Proceed to Memory Map** radio button allows direct access and programing of the AD4858 memory registers. Note that the **Apply Changes** button must be selected each time a setting is changed to take effect.

### ANALYSIS VIEW

Click **Proceed to Analysis** to navigate to the **AD4858 Analysis** window. From here, choose the type of analysis to be performed by selecting the **Waveform** tab, the **FFT** tab, or the **Histogram** tab. Select options for **Run Once** or **Run Continuous** to begin capturing data which will appear in the **Results** section and **Waveform** plot window. Select channel results to be displayed in **Displayed Channels** section (default is display all).

### Waveform Tab

The **Waveform** tab displays data in the form of time vs. discrete data values with the results, as shown in Waveform Tab.

## ACE SOFTWARE OPERATION

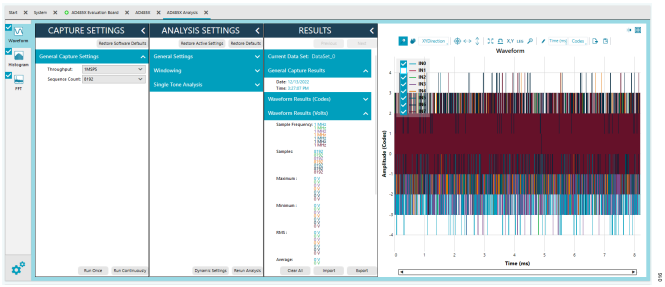


*Figure 16. Waveform Tab*

The **Waveform** graph shows each successive sample of the AD4858 output. The user can zoom in on and pan over the **Waveform** graph using the embedded waveform tool bar located above the graph. Select the channels to display in the **Display Channels** section.

Under the **Display Units** pull-down menu, select **Codes** above the **Waveform** graph to select whether the **Waveform** graph displays in units of **Codes**, **Hex**, or **Volts**. The axis controls are dynamic.

### FFT tab

The **FFT** tab displays fast Fourier transform (FFT) information for the last batch of samples gathered (see Figure 17).

When performing an FFT analysis, the **RESULTS** pane shows the noise and distortion performance of the AD4858. The signal-to-noise ratio (**SNR**) and other noise performance measurements, such as the signal-to-noise-and-distortion (**SINAD**), **Dynamic Range**, noise density (**Noise/Hz**), and peak harmonic or spurious noise (**SFDR**), are shown in the **Results** section. The total harmonic disturbance (**THD**) measurements, as well as the major harmonics contributing to the THD performance, are shown as well.

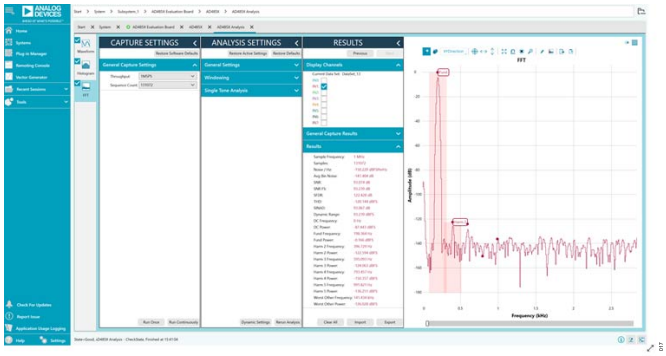


*Figure 17. FFT Analysis of a 200 Hz Sine Wave at 1 MSPS*

### Histogram Tab

The **Histogram** tab contains the histogram graph and the **RESULTS** pane, as shown in Figure 18.

The **RESULTS** pane displays the information related to the DC performance.

The **Histogram** graph displays the number of hits per code within the sampled data. Use this graph for DC analysis as it indicates the noise performance of the device.

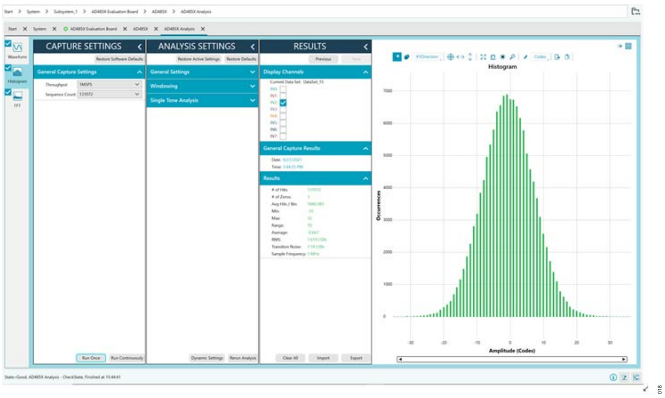


*Figure 18. Histogram Tab*

## EVALUATION BOARD SCHEMATIC AND ARTWORK

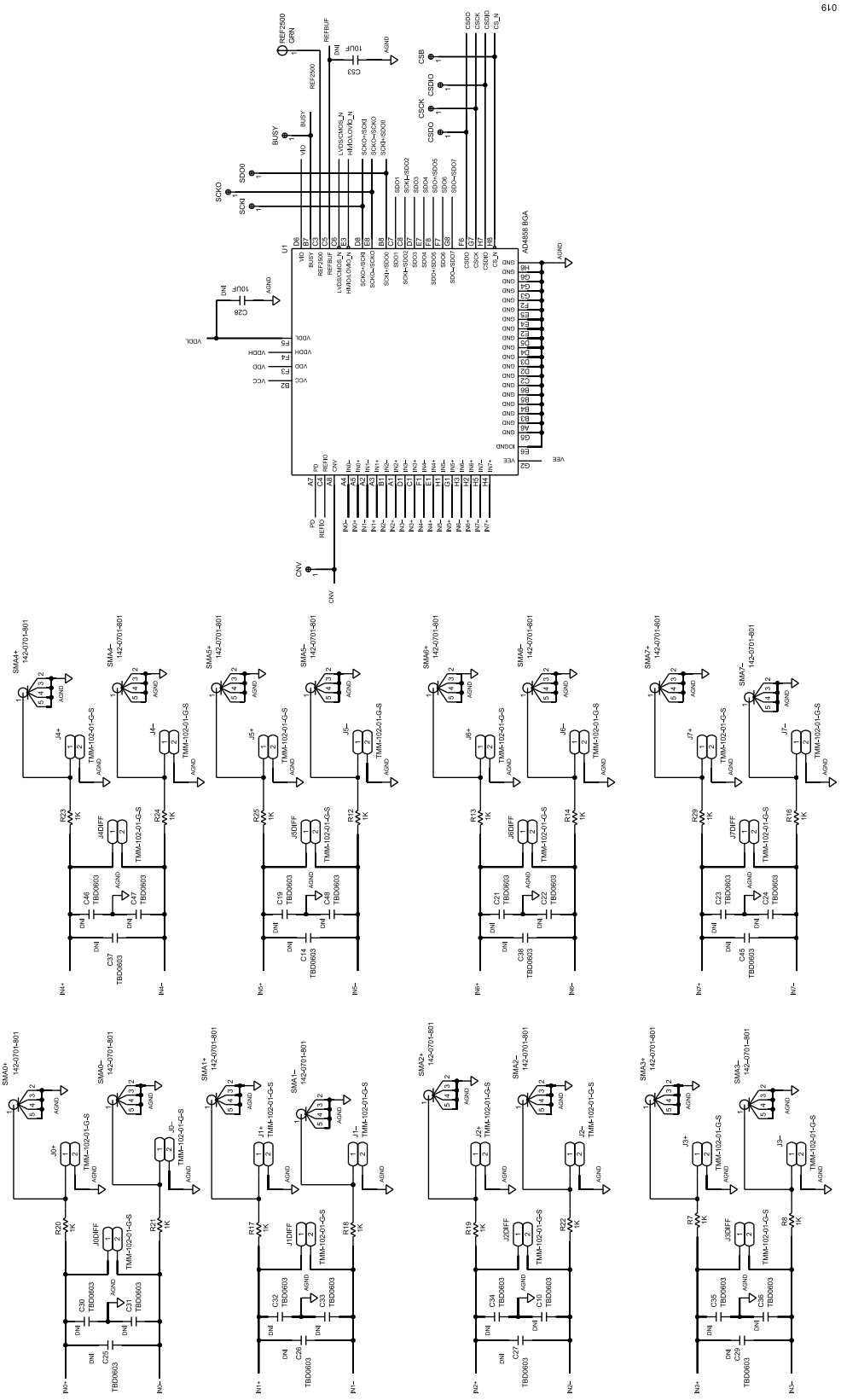

*Figure 19. Analog Inputs Schematic*

## EVALUATION BOARD SCHEMATIC AND ARTWORK

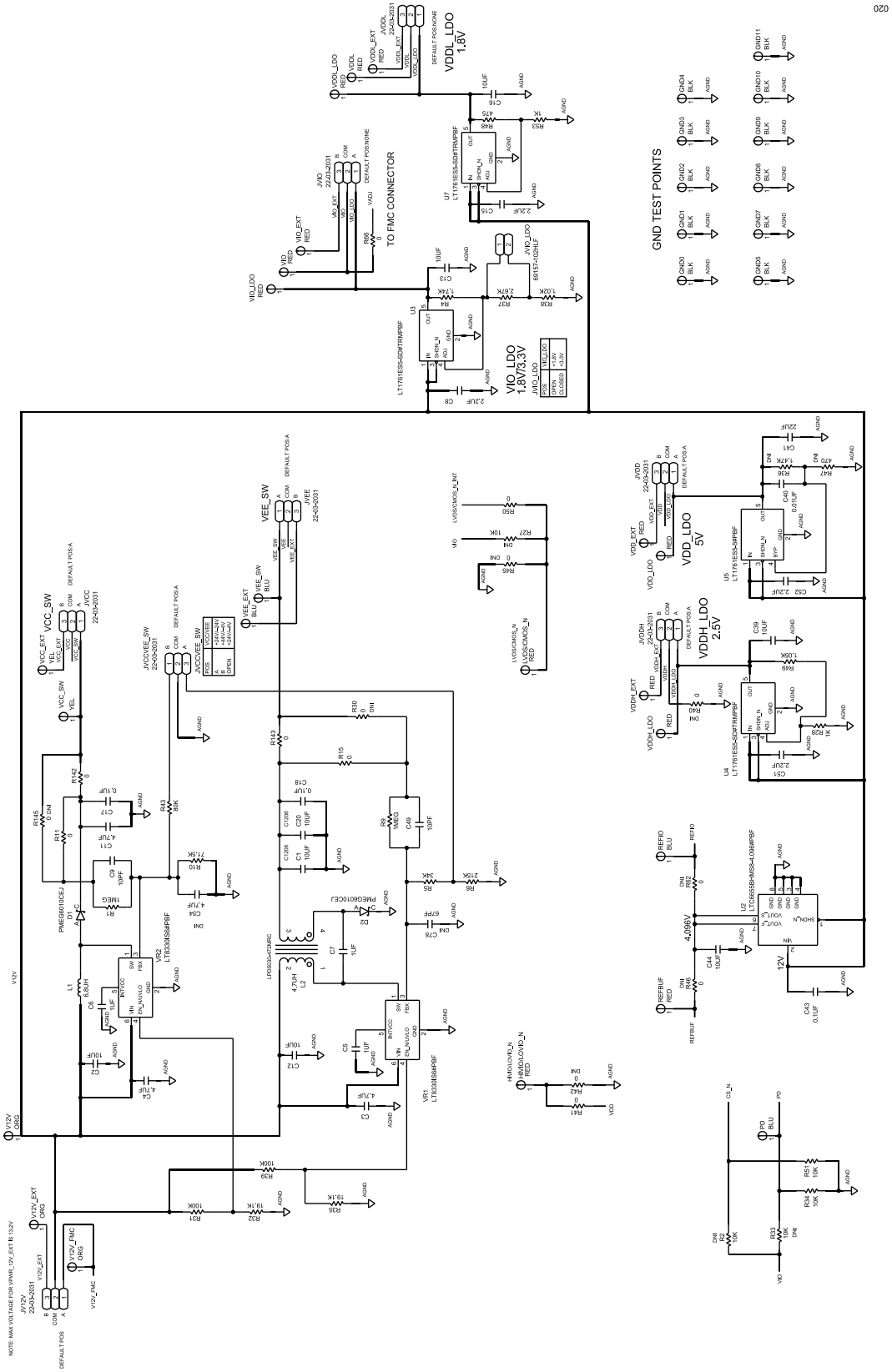


*Figure 20. Power Solution Schematic*

## EVALUATION BOARD SCHEMATIC AND ARTWORK

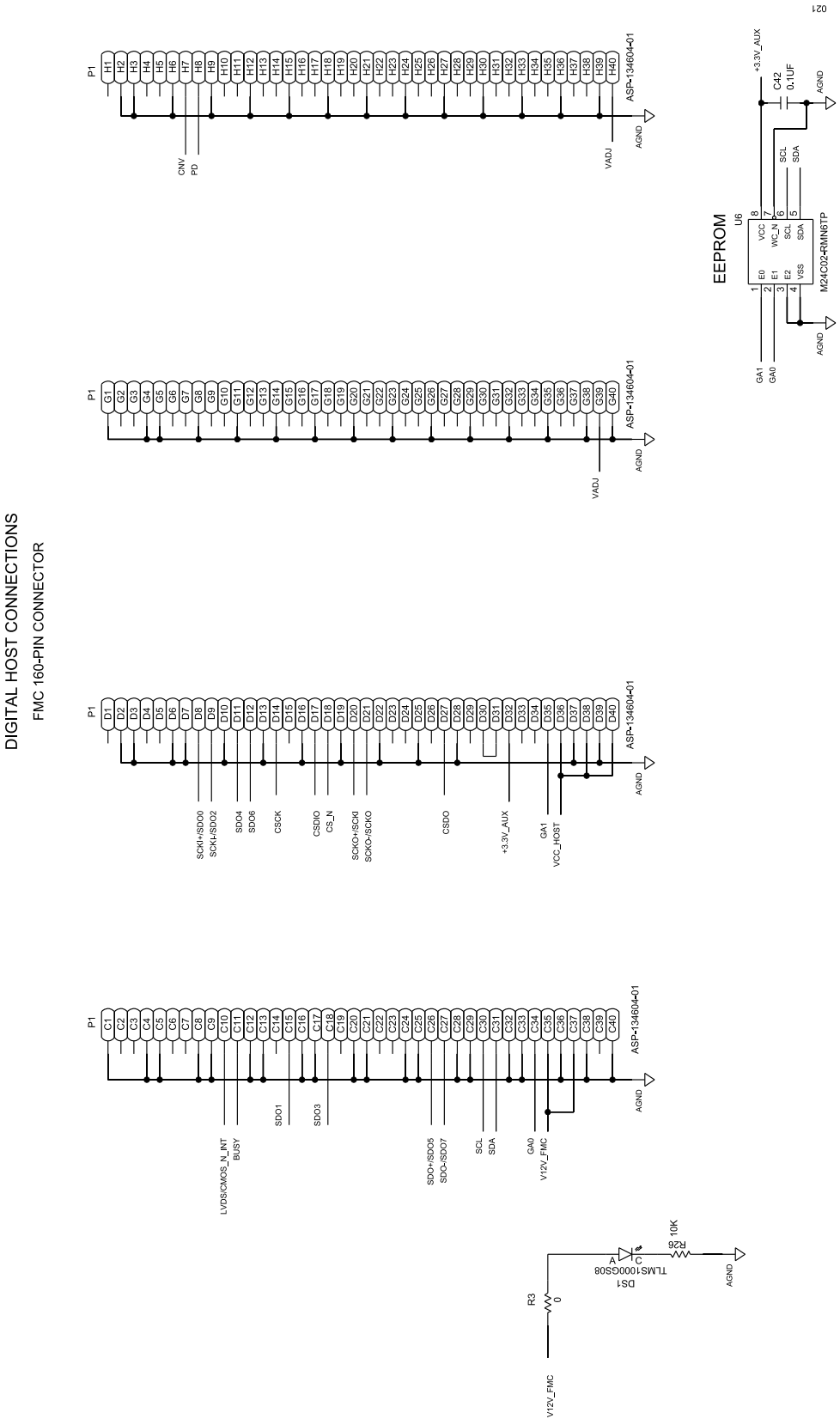


*Figure 21. FMC Connection Schematic*

## NOTES

**ESD Caution**
**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.