Evaluating the ADGM1121 0 Hz/DC to 16 GHz, 2 x DPDT, MEMS Switch

FEATURES

- Single-supply voltage: 3.3 V
- Wide frequency range: DC to 16 GHz
- 2.92 mm connectors for RF signals
- Parallel interface and SPI
- On-board calibration thru transmission line for analyzer calibration

EVALUATION KIT CONTENTS

- EVAL-ADGM1121SDZ evaluation board
- 2m USB 2.0 (Male) to USB Mini (Male) cable

ADDITIONAL EQUIPMENT NEEDED

- 3.3 V DC power supply or USB port
- Vector network analyzer (VNA)
- EVAL-SDP-CB1Z (SDP-B) controller board
- Analysis | Control | Evaluation (ACE) Software with EVAL-ADGM1121SDZ plugin

GENERAL DESCRIPTION

This user guide describes the EVAL-ADGM1121SDZ for the ADGM1121, a dual-chip, RF switching solution containing a double-pole, double-throw (DPDT), microelectromechanical systems (MEMS) switch, and a control chip co-packaged in a compact, 5.00 mm × 4.00 mm × 1.00 mm, LGA package.

The DPDT switch uses Analog Devices' MEMS switch technology, providing optimum performance in terms of bandwidth, power handling capability, and linearity for RF applications. The control chip generates the high-voltage signals needed for the MEMS switch and allows the user to control its operation through a simple and flexible complementary metal-oxide semiconductor (CMOS)/low voltage transistor to transistor logic (LVTTL)-compliant parallel-interface as well as through a serial-peripheral interface (SPI). It is possible to daisy-chain multiple ADGM1121 devices together to enable the configuration of multiple devices with a minimal number of digital lines.

For SPI, the EVAL-ADGM1121SDZ connects to the USB port of a PC through the system demonstration platform (SDP) board. The EVAL-SDP-CB1Z board (SDP-B controller board) is available to order at the Analog Devices website.

The EVAL-ADGM1121SDZ comes fitted with connectors for RF and control signals as well as links to control the operation of the switch and evaluate its performance.

For full details on the ADGM1121, see the ADGM1121 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADGM1121SDZ.

EVAL-ADGM1121SDZ PHOTOGRAPH

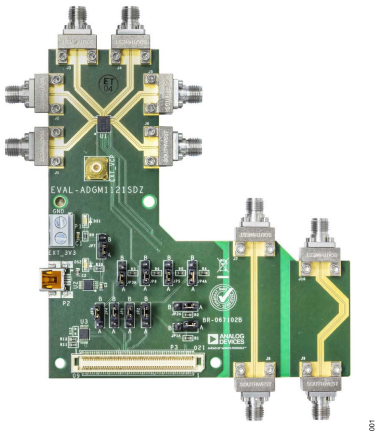

Figure 1. EVAL-ADGM1121SDZ Photograph

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EVALUATION BOARD HARDWARE

The EVAL-ADGM1121SDZ evaluation kit contains a fully fitted printed circuit board (PCB).

The EVAL-ADGM1121SDZ allows the user to connect RF signals to the MEMS switch. The user controls the switch operation using the on-board links or by applying the correct control signals to the appropriate connectors.

The EVAL-ADGM1121SDZ provides an additional transmission line to facilitate the calibration of the network analyzer to minimize the effects of the PCB tracks that connect the RF signals to the MEMS switch. See the Network Analyzer Calibration Procedure section for more information on the calibration process.

POWER SUPPLY

To operate the EVAL-ADGM1121SDZ, the user must provide an external power supply either through a Mini-USB connector (USB_PWR) or through the power block (EXT_3V3). When JP7 is in the USB_PWR position, the EVAL-ADGM1121SDZ is powered by the Mini-USB connector, and when JP7 is in the EXT_3V3 position, the EVAL-ADGM1121SDZ is powered by the external 3.3 V power supply through the power block (see Table 1). The power-supply voltage required for the EVAL-ADGM1121SDZ is 3.3 V, and it must be positive with respect to the ground of the EVAL-ADGM1121SDZ. The ground of the EVAL-ADGM1121SDZ is marked with GND on the silkscreen (see Figure 24).

Table 1. JP7 Link Position

Position	Power Supply Selection
USB_PWR	EVAL-ADGM1121SDZ powered by the Mini-USB
EXT_3V3	EVAL-ADGM1121SDZ powered by the external 3.3 V power supply

RF CONNECTORS

The 2.92 mm end launch connectors on the EVAL-ADGM1121SDZ (RF1A, RF2A, RF1B, RF2B, RFCA, and RFCB) connect to each switch in the ADGM1121 for performance evaluation. The J7 and J8 connectors connect to a transmission line to estimate the loss associated with the PCB (see the Measuring Switch Performance section). Table 2 describes the RF connectors to the ADGM1121.

Table 2. Connecting the RF Connectors to the ADGM1121

Connector	Description
RF1A	Port RF1A of the ADGM1121
RF1B	Port RF1B of the ADGM1121
RF2A	Port RF2A of the ADGM1121
RF2B	Port RF2B of the ADGM1121
RFCA	Common RFCA port of the ADGM1121
RFCB	Common RFCB port of the ADGM1121
J7, J8	Calibration thru transmission lines used for calibration

SWITCH CONTROL CONNECTORS

The ADGM1121 can either be controlled through SPI or parallel-interface. When the PIN_N/SPI link is set to the B position, the SPI is enabled. When the PIN_N/SPI link is set to the A position, the parallel-interface is enabled (see Table 3).

Table 3. PIN_N/SPI Link Position

Position	Reference Clock Setting
A (Default)	Parallel-interface enabled
B	SPI enabled, parallel-interface disabled

The ADGM1121 comes with a standard LVTTL parallel-interface consisting of four input pins (IN1, IN2, IN3, and IN4) controlled by the IN1, IN2, IN3, and IN4 links. See Table 6 for more details on the logic control when using the parallel-interface. JP1 to JP4 links should be moved to the B position (see Table 4)

The ADGM1121 also has an SPI that can be controlled by connecting to the USB port of a PC through the SDP board connected to the SDP connector (P3). JP1 to JP4 links should be moved to position A (see Table 4).

Table 4. JP1 to JP4 Link Position

Position	Control Interface Setting
A	SPI control through SDP Connector (P3)
B (Default)	Parallel-interface through IN1 to IN4

The control IC packaged with the MEMS switch internally generates the voltage required to drive the switch. The internal control IC contains a reference clock signal at a nominal 10 MHz. In normal operation, set the EXTD_EN link to A position, enabling the built-in 10 MHz oscillator to enable the internal driver IC voltage boost circuitry (see Table 5). Set the EXTD_EN link to B position to disable the internal 10 MHz oscillator and drive the VCP pin with 80 V DC from the external voltage supply. The VCP pin is connected to the EXT_VCP Subminiature Version B (SMB) connector on the EVAL-ADGM1121SDZ, which can be used for applying 80 V DC to the external voltage supply. Disabling the internal oscillator eliminates the associated 10 MHz noise feedthrough into the switch. With the oscillator disabled, the logic interface pins (IN1 to IN4) still control the switch.

Table 5. EXTD_EN Link Position

Position	Reference Clock Setting
A (Default)	Built-in 10 MHz oscillator enable
B	Disables the internal oscillator

EVALUATION BOARD HARDWARE

Table 6. Link Settings (Per PCB Label) for Parallel-Interface Use

Link Name	Link Position	RF Switch Status
IN1	OFF (default)	RF1A to RFCA = OFF
	ON	RF1A to RFCA = ON
IN2	OFF (default)	RF2A to RFCA = OFF
	ON	RF2A to RFCA = ON
IN3	OFF (default)	RF2B to RFCB = OFF
	ON	RF2B to RFCB = ON
IN4	OFF (default)	RF1B to RFCB = OFF
	ON	RF1B to RFCB = ON

EVALUATION BOARD SOFTWARE FOR THE SPI

INSTALLING THE SOFTWARE

The EVAL-ADGM1121SDZ uses the Analog Devices ACE software. ACE is a desktop software application that allows the evaluation and control of multiple evaluation systems.

The ACE software installer installs the necessary SDP drivers and .NET Framework 4 by default. Install the ACE software before connecting the SDP driver. The Analog Devices website provides the ACE software and access to full instructions on how to install and use it.

After the installation completes, the EVAL-ADGM1121SDZ plugins appear when opening the ACE software.

INITIAL SETUP

Complete the following steps to set up the EVAL-ADGM1121SDZ:

1. Change the PIN_N/SPI link position from A to B and keep the EXTD_EN link position at A position (see Table 3 and Table 5).
2. Change the position of the JP1 through the JP4 links to the A position (see Table 4), respectively.
3. Connect the EVAL-ADGM1121SDZ to the SDP board and connect the SDP board to the computer through a USB cable.
4. Power the EVAL-ADGM1121SDZ, as described in the Power Supply section.
5. Run the ACE software. The EVAL-ADGM1121SDZ plugins appear in the **Attached Hardware** window of the **Start** tab (see Figure 2).
6. Double-click the EVAL-ADGM1121SDZ plugins to open the evaluation board view in Figure 3.
7. The chip block diagram can be accessed by double-clicking the **ADGM1121** chip (see Figure 3). The view after clicking the **ADGM1121** chip provides a basic representation of the functionality of the EVAL-ADGM1121SDZ. The main functions are labeled in Figure 4.

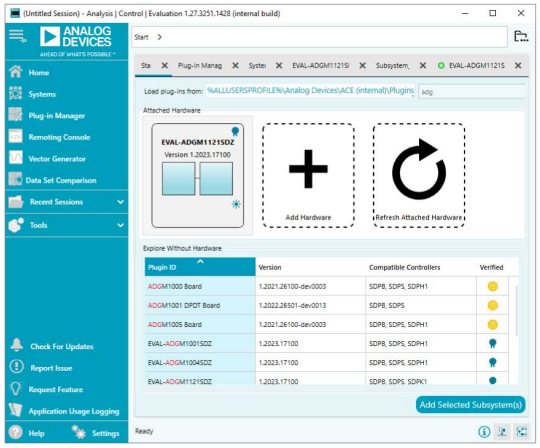

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Figure 2. EVAL-ADGM1121SDZ Plugin Start-Up Window

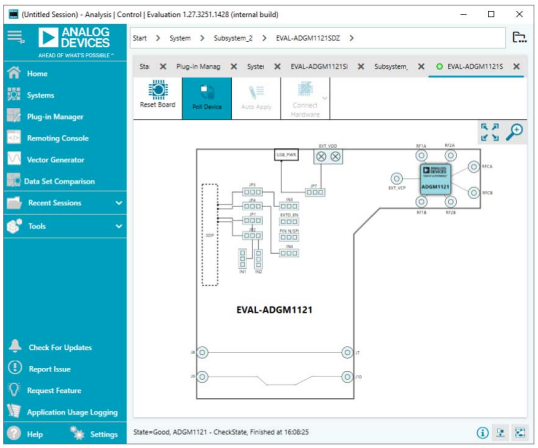

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Figure 3. Evaluation Board View of the EVAL-ADGM1121SDZ

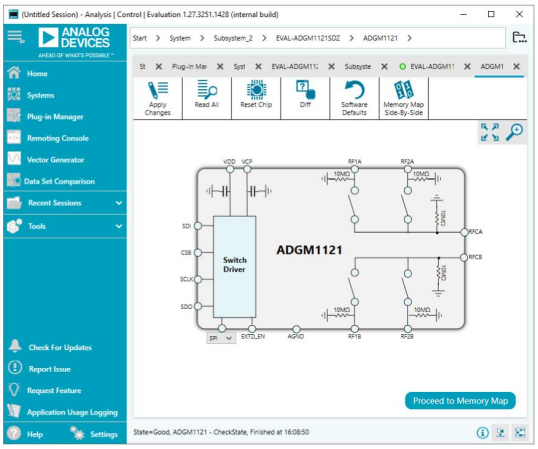

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Figure 4. Chip Block Diagram View for the ADGM1121

EVAL-ADGM1121SDZ BLOCK DIAGRAM AND DESCRIPTIONS

The EVAL-ADGM1121SDZ software is organized so that it appears similar to the functional block diagram shown in the ADGM1121 data sheet. A full description of each block and register, as well as their respective settings, are given in the ADGM1121 data sheet.

Some of the blocks and their functions are described in Table 7 because these blocks pertain to the EVAL-ADGM1121SDZ. The full screen block diagram, shown in Figure 5, describes the functionality of each block.

All changes to the blocks correspond to the block diagram in the software. For example, if the internal register bit is enabled, it displays as enabled on the block diagram. If any bits or registers have modified values not transferred to the EVAL-ADGM1121SDZ, they appear in bold in Figure 5. After clicking **Apply Changes**, the data is transferred to the EVAL-ADGM1121SDZ.

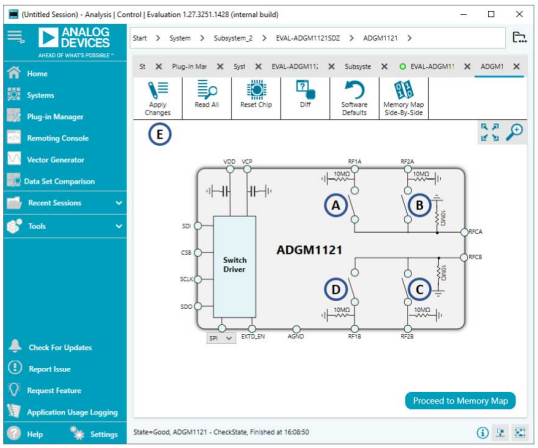

Figure 5. EVAL-ADGM1121SDZ Block Diagram with Labels

Table 7. EVAL-ADGM1121SDZ Block Diagram Function Descriptions (See Figure 5)

Label	Function Description
A	Click the switch symbol to open and close the RF1A to RFCA switch.
B	Click the switch symbol to open and close the RF2A to RFCA switch.
C	Click the switch symbol to open and close the RF2B to RFCB switch.
D	Click the switch symbol to open and close the RF1B to RFCB switch.
E	Click **Apply Changes** to apply all the modified values to the devices.

EVAL-ADGM1121SDZ BLOCK DIAGRAM AND DESCRIPTIONS

MEMORY MAP

Click **Proceed to Memory Map** for full accessibility to all the registers (see Figure 5). This access allows registers to be edited at a bit level (see Figure 6). The bits shaded in dark gray in Figure 6 are read only bits and cannot be accessed from ACE, and all other bits are toggled. Clicking **Apply Changes** transfers data to the ADGM1121.

All changes made in the memory map correspond to the block diagram. For example, if the internal register bit is enabled, the bit displays as enabled in the block diagram. Any bits or registers that are bold in Figure 6 are modified values not transferred to the EVAL-ADGM1121SDZ. Click **Apply Changes** to transfer data to the EVAL-ADGM1121SDZ.

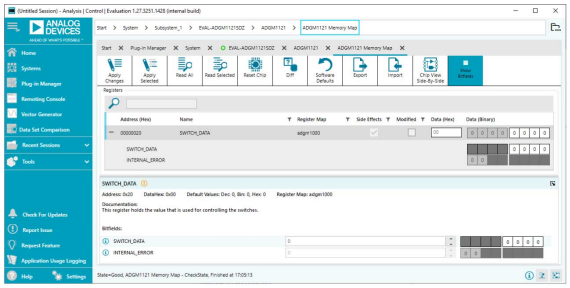

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Figure 6. ADGM1121 Memory Map

MEASURING SWITCH PERFORMANCE

Figure 7 shows the connection diagram of the EVAL-ADGM1121SDZ in parallel-interface. Apply a V_{DD} supply to the EVAL-ADGM1121SDZ to measure the performance of the switch. The links are set according to the switch under test (see Table 6). After selecting the desired channel and its state, the switch performance data can be collected using a network analyzer. Terminate the RFx edge connectors of the unused switch channels into 50 Ω loads to achieve the full performance of the channel under test.

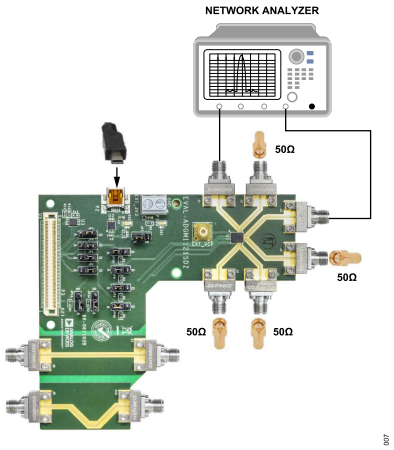

Figure 7. EVAL-ADGM1121SDZ Connection Diagram for Parallel-Interface

The EVAL-ADGM1121SDZ, shown in Figure 7, comes with a calibration transmission line, calibration thru, on the PCB. This calibration line removes the insertion loss and phase offset of the PCB transmission lines connecting to the switch from the measurement. Figure 8 shows the calibration transmission line and Figure 9 shows its insertion loss and return loss up to 20 GHz. The calibration line is exactly the same length as the distance from any one RFxA/RFxB connector to the RFCA/RFCB pin of the ADGM1121 plus the distance from the RFCA/RFCB connector to the RFCA/RFCB pin of the ADGM1121.

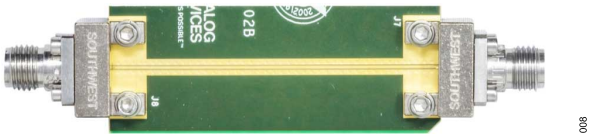

Figure 8. EVAL-ADGM1121SDZ Calibration Transmission Line Used for PCB Insertion Loss and Phase Offset Correction

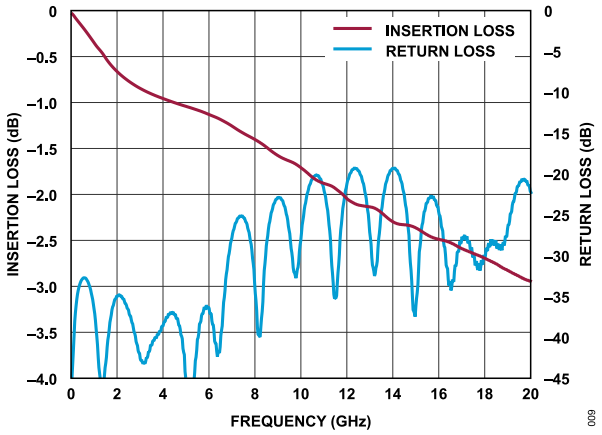

Figure 9. Calibration Transmission Line Insertion Loss and Return Loss

Figure 10 shows the calibration line length. All RF traces connecting to the ADGM1121 are of equal length.

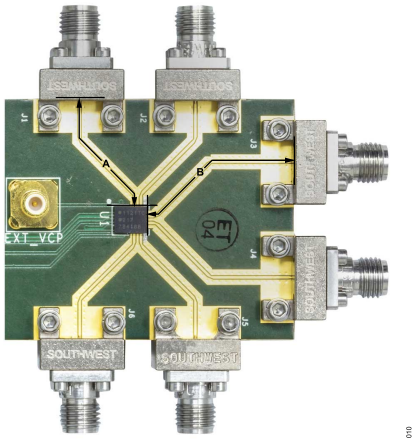

Figure 10. Calibration Transmission Line Length Equal to the A + B Length

To de-embed the PCB transmission line insertion loss from the entire switch insertion loss board measurement (the RF1A to RFCA path), divide the S(2,1) insertion loss of the measured data by the |S(2,1)| of the calibration thru line. Perform this de-embedding using the network analyzer at the time of the measurement or after the measurement using individual measurement data files. See the Network Analyzer Calibration Procedure section for more information.

Use the network analyzer port extension function to de-embed any phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delays into the port extension menu on the network analyzer corresponding to any phase offset introduced from an RF edge connector to the switch pin. Figure 10 shows an example of these phase offsets on a typical switch measurement, labeled as A and B. Both A and B are identical in length and can be calculated by measuring the time delay of the calibration line and dividing it by two.

MEASURING SWITCH PERFORMANCE

Figure 11 shows the ADGM1121 switch insertion loss measurement results of all four channels that are de-embedded with respect to the PCB transmission line losses.

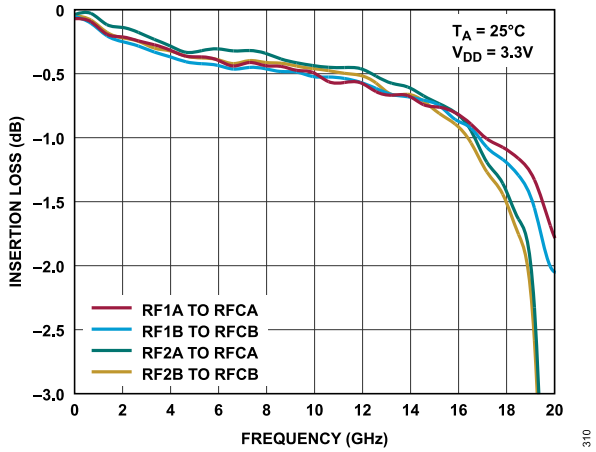

Figure 11. PCB De-Embedded ADGM1121 Insertion Loss Performance

Figure 12 shows the ADGM1121 switch return loss performance measurement results for all four channels.

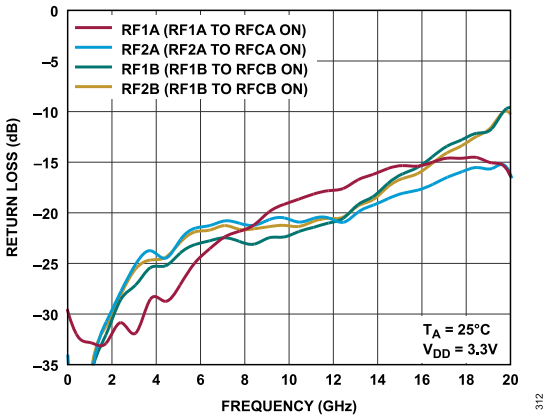

Figure 12. ADGM1121 Return Loss Performance

Figure 13 shows the ADGM1121 switch off isolation performance measurement results for all four channels.

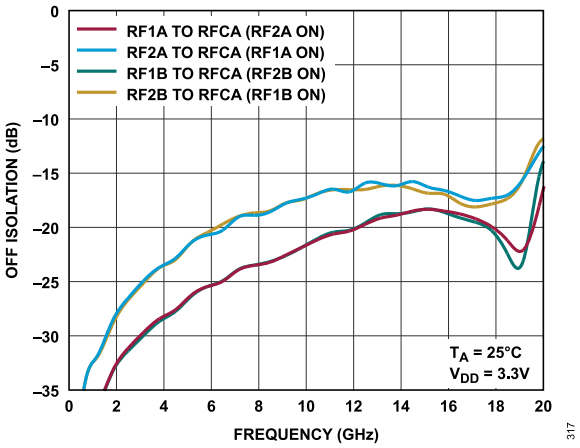

Figure 13. ADGM1121 Off-Isolation Performance

NETWORK ANALYZER CALIBRATION PROCEDURE

Use the following procedure in conjunction with the EVAL-ADGM1121SDZ for two-port measurements, assuming there is a set of manual calibration standards or an electric calibration type unit to perform a short load open through (SLOT) calibration of the network analyzer. The maximum value for the network analyzer frequency sweep for the EVAL-ADGM1121SDZ PCB can be up to 20 GHz. Perform the following steps for the two-port measurements:

1. Perform a full, two-port standard SLOT calibration of the network analyzer.
2. Connect the calibration thru calibration line (Connector J7 and Connector J8) to the analyzer and measure its insertion loss, S(2,1).
3. Save the measured data to the network analyzer memory for later use.
4. Configure the EVAL-ADGM1121SDZ links and power up the EVAL-ADGM1121SDZ, as described in the Power Supply section.
5. Connect the network analyzer to the desired MEMS switch RF connectors and apply the external control signals, if needed.
6. Measure the complete insertion loss of the EVAL-ADGM1121SDZ. Include the insertion loss of the MEMS switch and test fixture (PCB transmission lines and RF connectors).
7. De-embed the PCB losses from the complete evaluation board measurement using the data saved at step 3 and the measured data at step 6. Because the extraction method is dependent on the network analyzer, consult the network analyzer user manual before performing the extraction. Typically, the divide **Data/Memory** math function divides the complete S(2,1) insertion loss measurement data by the calibration thru line S(2,1) insertion loss data stored in memory.
8. Use the network analyzer port extension function to de-embed the phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delay values into the port extension menu on the network analyzer for each RF edged connector to switch the pin path equal to the electrical length of the calibration line divided by two.

HANDLING GUIDELINES

Adhere to the following handling guidelines for the EVAL-ADGM1121SDZ:

- Always treat the ADGM1121 as a static sensitive device and observe normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps, or other electrostatic discharge (ESD) control devices.
- Take care when connecting signals. Hold the EVAL-ADGM1121SDZ from the edges to avoid any damage to the device under test (DUT).
- Avoid connecting live signal sources. Ensure that outputs are switched off (preferably grounded) before connecting to the DUT. In addition, ensure all instrumentation shares a common chassis ground.
- Avoid running measurement instruments (for example, digital multimeters (DMMs) in autorange modes). Some instruments can generate large transient compliance voltages when switching ranges.
- Use the highest practical range (that is, lowest resolution) setting for resistance measurements to minimize compliance voltages.

LAYOUT RECOMMENDATIONS

The EVAL-ADGM1121SDZ is a 4-layer board. The EVAL-ADGM1121SDZ uses 8 mil Roger RO4003C dielectric. The outer copper layers have 2.2 mil finish thickness with electroless nickel immersion gold (ENIG) finish. The RF transmission lines were designed using a coplanar waveguide model with a width of 14 mil and ground spacing of 7 mil to have a characteristic impedance of 50 Ω (see Figure 14 and Figure 15). It is recommended to use plenty of vias under the ADGM1121 and along the RF traces to provide good grounding and to avoid any resonance at high frequencies. To achieve optimum RF performance, Southwest Microwave end launch edge mount jack connectors (1092-04A-12) are used.

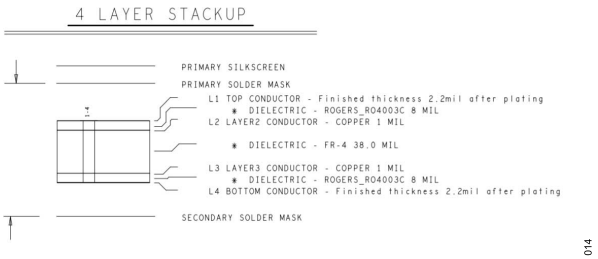

Figure 14. EVAL-ADGM1121SDZ Board Stackup

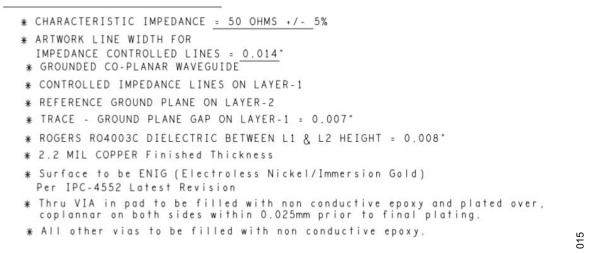

Figure 15. EVAL-ADGM1121SDZ Additional Board Manufacturing Information

SOLDERING RECOMMENDATIONS

To avoid solder voids under the ADGM1121, it is recommended to use a 0.0767 mm (3 mil) thick solder stencil with nano coating. The aperture size for the solder stencil must be 1:1, and divide the paste mask with multiple pads, as shown in Figure 16. Poor soldering may impact the RF performance of the ADGM1121.

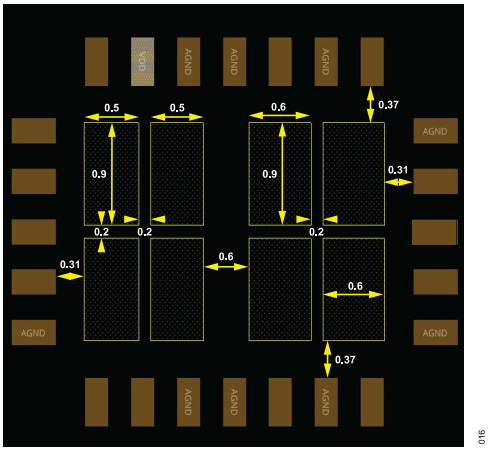

Figure 16. Solder Stencil Recommendations in Millimeters

EVALUATION BOARD SCHEMATICS AND ARTWORK

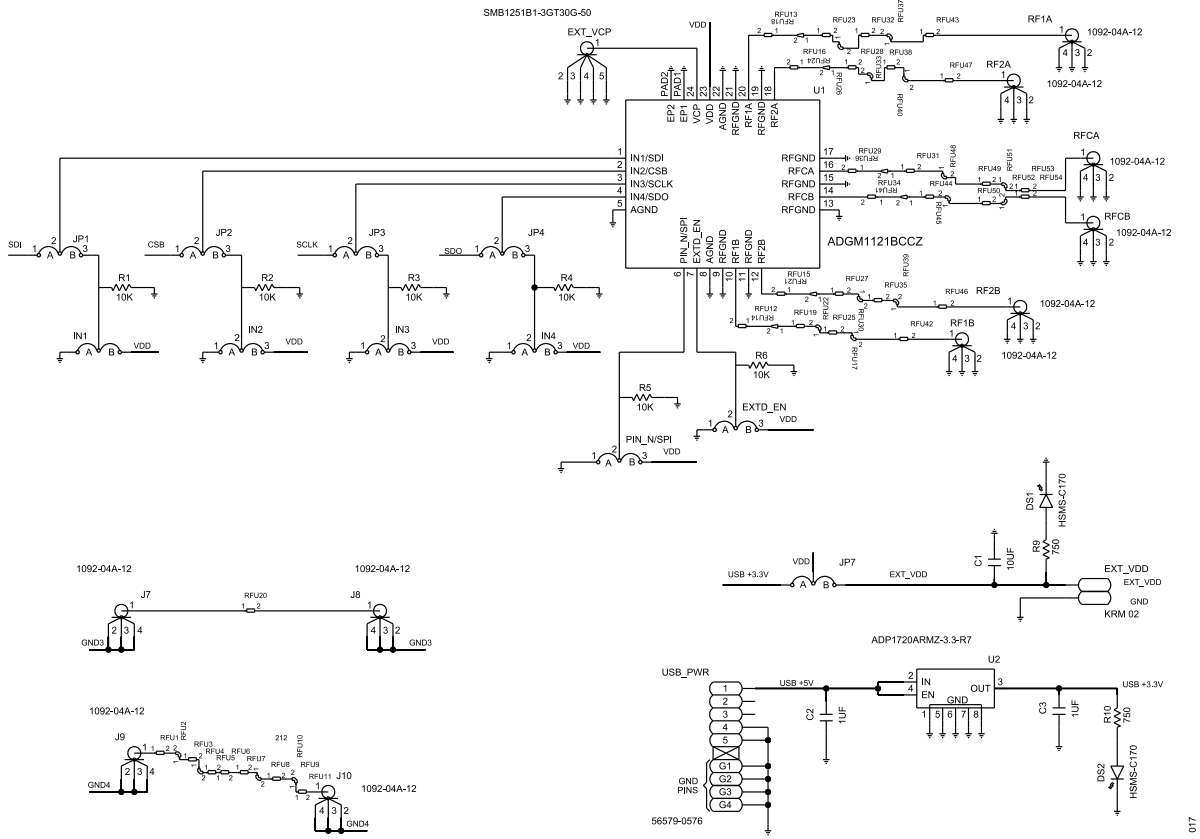

Figure 17. Schematic of the EVAL-ADGM1121SDZ

EVALUATION BOARD SCHEMATICS AND ARTWORK

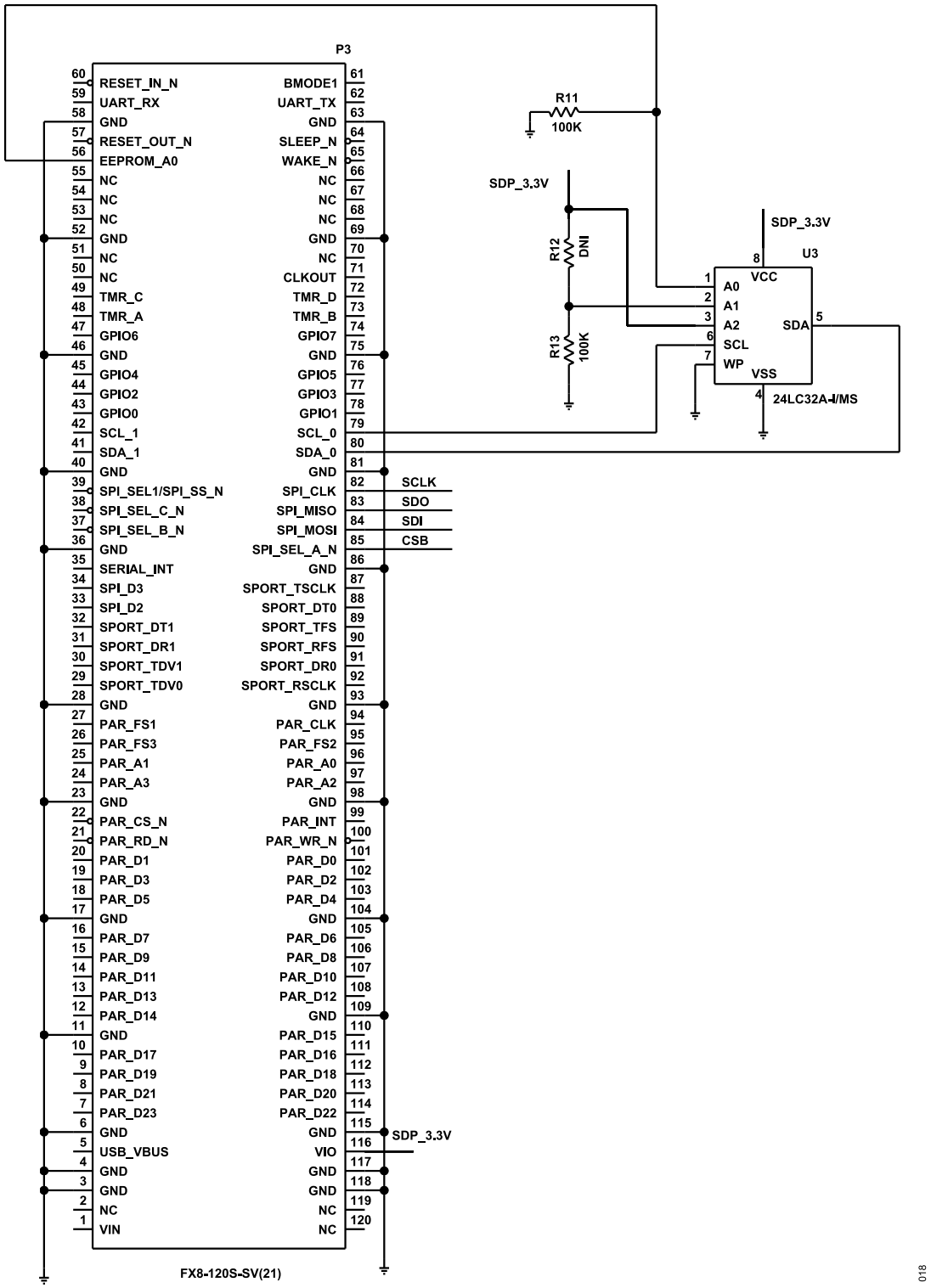

Figure 18. Schematic of the EVAL-ADGM1121SDZ with an SDP Connector

EVALUATION BOARD SCHEMATICS AND ARTWORK

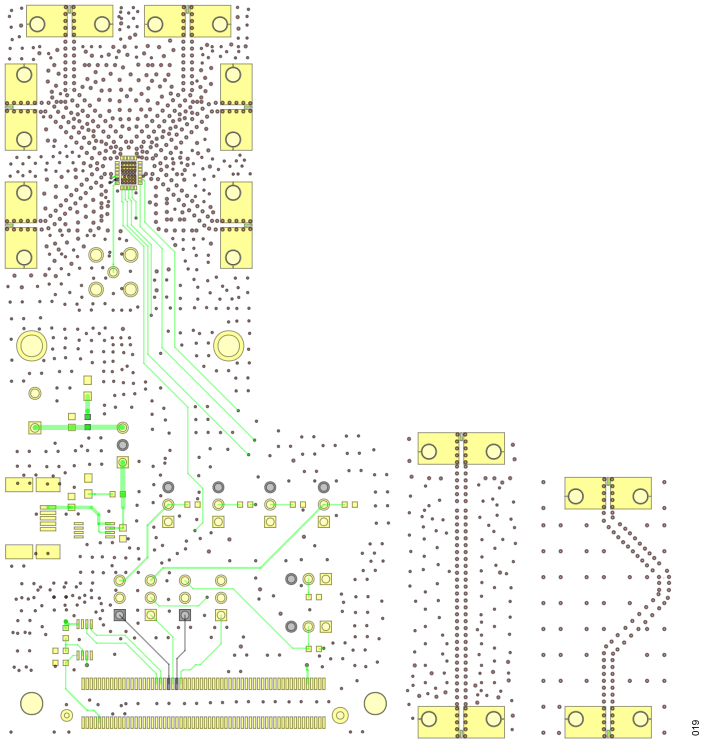

Figure 19. EVAL-ADGM1121SDZ Component Side PCB Drawing (Layer 1)

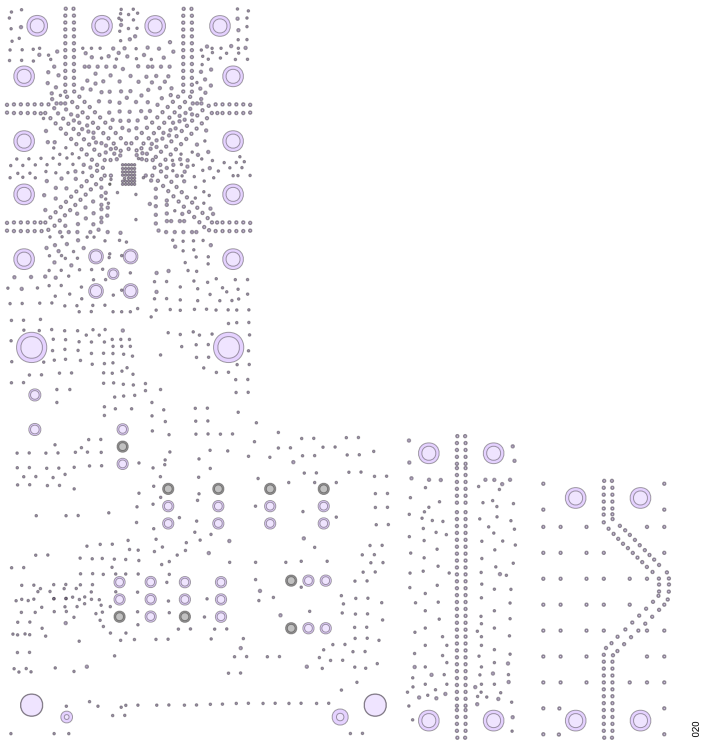

Figure 20. EVAL- ADGM1121SDZ Component Side Ground Plane PCB Drawing (Layer 2)

EVALUATION BOARD SCHEMATICS AND ARTWORK

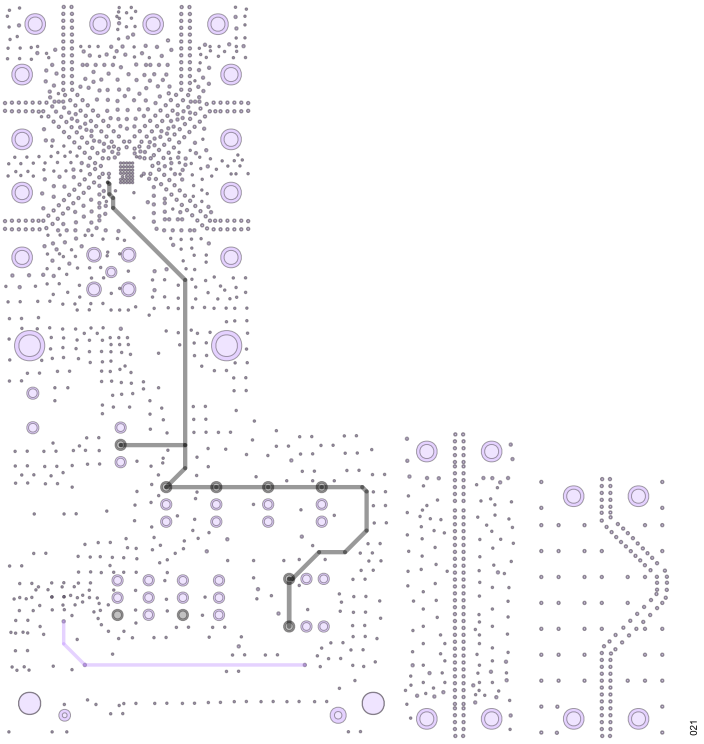

Figure 21. EVAL- ADGM1121SDZ Component Side Ground Plane PCB Drawing (Layer 3)

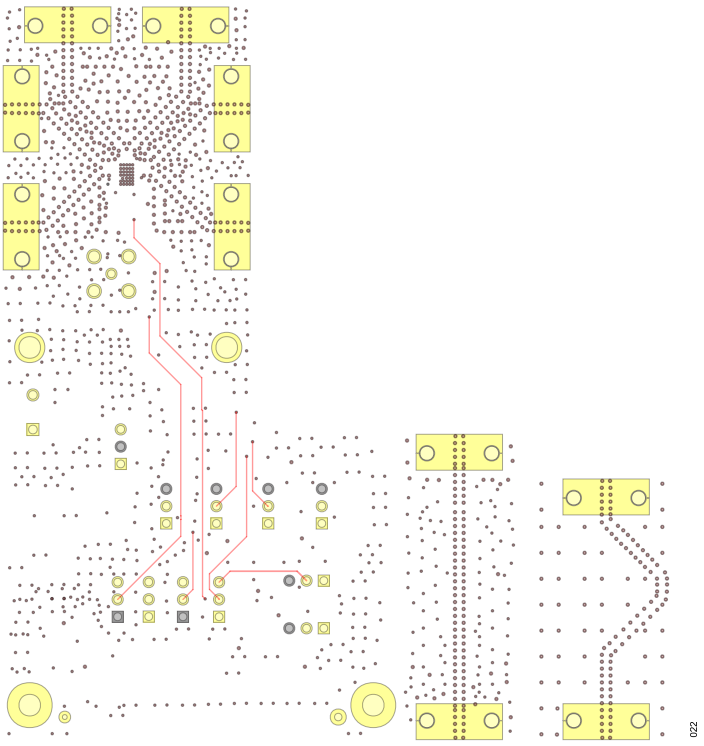

Figure 22. EVAL- ADGM1121SDZ Component Side, Bottom Side PCB Drawing (Layer 4)

EVALUATION BOARD SCHEMATICS AND ARTWORK

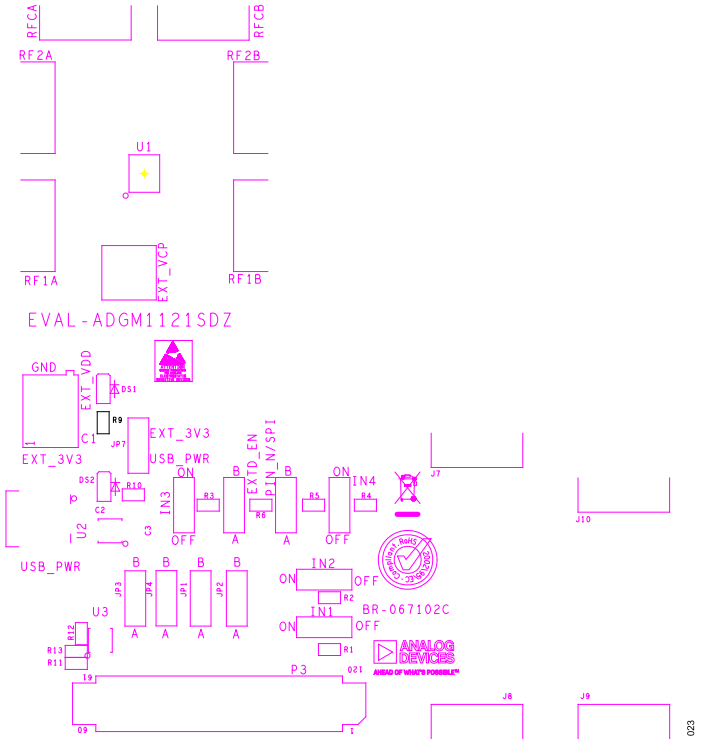

Figure 23. EVAL-ADGM1121SDZ Component Side Silkscreen PCB Drawing (Top)

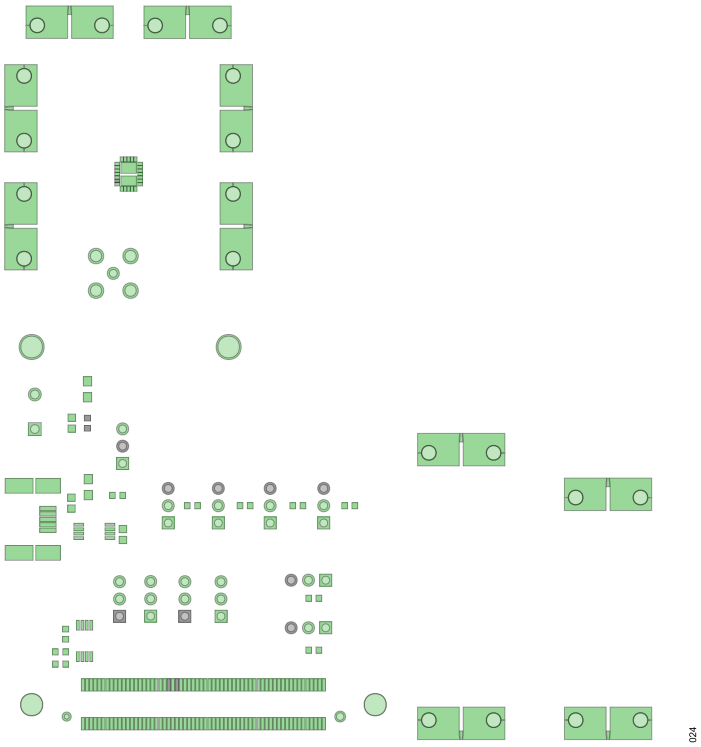

Figure 24. EVAL-ADGM1121SDZ Soldermask Top

EVALUATION BOARD SCHEMATICS AND ARTWORK

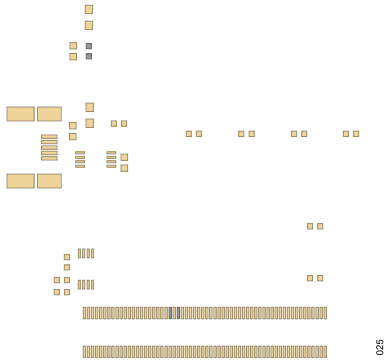

Figure 25. EVAL-ADGM1121SDZ Paste Top

ORDERING INFORMATION

BILL OF MATERIALS

Table 8. Bill of Materials

Reference Designator	Description	Manufacturer	Manufacturer Number
C1	10 µF ceramic capacitor, 10 V, 20%, X5R, 0603, low effective series resistance (ESR)	TDK	C1608X5R1A106M080AC
C2, C3	1 µF ceramic capacitors, 16 V, 10%, X7R, 0603	AVX	0603YC105KAT2A
DS1, DS2	630 nm light emitting diode (LED), surface-mount device (SMD), red	Broadcom Limited	HSMS-C170
EXTD_EN, IN1 to IN4, JP1 to JP4, JP7, PIN_N/SPI	PCB connectors, 3-position, male header, unshrouded single row, 2.54 mm pitch, 3 mm solder tail	Harwin	M20-9990345
EXT_VCP	PCB connectors, Subminiature Version B (SMB), coaxial straight jack	Amphenol	SMB1251B1-3GT30G-50
EXT_VDD	2-pin terminal block (5 mm pitch)	Lumberg	KRM 02
J7 to J10, RF1A, RF1B, RF2A, RF2B, RFCA, RFCB	Coaxial connectors, edge launch edge mount, 2.92 mm jack	Southwest Microwave	1092-04A-12
P3	120-way, 0.6 mm pitch, 2 row straight PCB connector	HRS	FX8-120S-SV(21)
R1 to R6	10 kΩ resistors, SMD, 0.01%, 1/16 W, 0603	Multicomp (SPC)	MCTF0603TTX1002
R9, R10	750 Ω resistor, SMD, 1%, 1/10 W, 0603, AEC-Q200	Vishay	CRCW0603750RFKEA
R11, R13	100 kΩ resistors, SMD, 1%, 1/10 W, 0603	Yageo	RC0603JR-07100KL
R12	100 kΩ resistor, SMD, 1%, 1/10 W, 0603, do not insert (DNI)	Yageo	RC0603JR-07100KL
U1	IC, 0 Hz to 16 GHz, SPDT MEMS switch	Analog Devices	ADGM1121BCCZ
U2	IC, 32 kb serial EEPROM	Microchip Technology	24LC32A-I/MS
U3	IC, 50 mA, high voltage, micropower linear regulator	Analog Devices	ADP1720ARMZ-3.3-R7
USB_PWR	CONN-PCB USB MINI-AB SERIES	Molex	56579-0576
Not applicable[1]	Wideband 50 Ω termination SMA loads	Pasternack	PE6081

[1] Screwed on at measurement time (see Figure 7).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.