NSF040120L3A0

1200 V, 40 mΩ, N-channel SiC MOSFET

6 October 2023 **Objective data sheet**

1. General description

The NSF040120L3A0 is a Silicon Carbide based 1200V power MOSFET in a well-established 3-pin TO-247-3 plastic package for through hole PCB mounting technology. The excellent R_{DSon} temperature stability combined with its fast switching speed makes it a product of choice in high power and high voltage industrial applications like E-vehicle charging infrastructure, photovoltaic inverters and motor drives.

2. Features and benefits

- Very low switching losses
- Fast reverse recovery
- Fast switching speed
- Temperature independent turn-off switching losses
- Very fast and robust intrinsic body diode

3. Applications

- E-vehicle charging infrastructure
- Photovoltaic inverters
- Switch mode power supply
- Uninterruptable power supply
- Motor drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage			-	-	1200	V
V_{GS}	gate-source voltage		[1]	-10	-	22	V
I_D	drain current	T_c = 25 °C	[2]	-	-	66	A
		T_c = 100 °C	[2]	-	-	48	A
I_{DM}	peak drain current	pulsed; t_p limited by T_j (max)	[3]	-	-	160	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 15 V; I_D = 40 A; T_j = 25 °C		-	40	60	mΩ

[1] Recommended turn off gate voltage is -5 V. Recommended turn on gate voltage is 15 V. Do not use with V_{GSon} < 13 V.
[2] Limited by $T_{j(max)}$ and $R_{th(j-c)max}$.
[3] Designed value (not tested).

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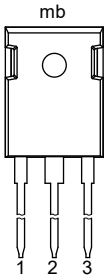
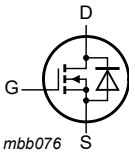
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 TO-247-3L (SOT429-2)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NSF040120L3A0	TO-247-3L	Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247-3L	SOT429-2

7. Marking

Table 4. Marking codes

Type number	Marking code
NSF040120L3A0	NSF0412A0

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	1200	V
V_{GS}	gate-source voltage		[1]	-10	22	V
I_D	drain current	T_c = 25 °C	[2]	-	66	A
		T_c = 100 °C	[2]	-	48	A
I_{DM}	peak drain current	pulsed; t_p limited by T_j (max)	[3]	-	160	A
P_{tot}	total power dissipation	T_c = 25 °C	[2]	-	319	W
T_j	junction temperature			-55	175	°C
T_{stg}	storage temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_c = 25 °C	[2]	-	59	A
I_{SM}	peak source current	pulsed; limited by T_j (max)	[3]	-	120	A

[1] Recommended turn off gate voltage is -5 V. Recommended turn on gate voltage is 15 V. Do not use with V_{GSon} < 13 V.
[2] Limited by $T_{j(max)}$ and $R_{th(j-c)max}$.
[3] Designed value (not tested).

9. Thermal characteristics

Table 6. Thermal characteristics

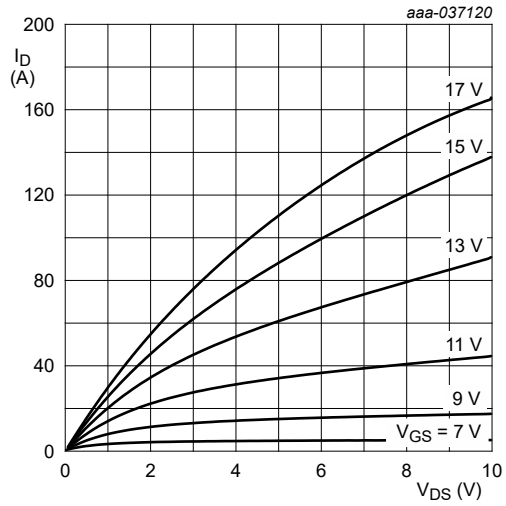
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case			-	0.37	0.47	K/W

10. Characteristics

Table 7. Characteristics

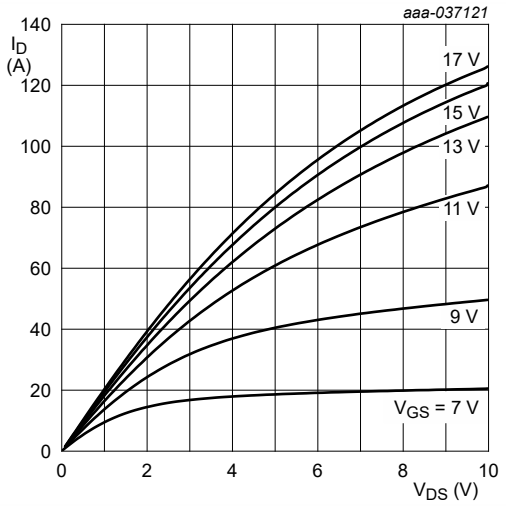
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0 V; T_j = 25 °C		1200	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 4 mA; V_{DS} = V_{GS}; T_j = 25 °C	[1]	1.7	2.3	2.9	V
I_{DSS}	drain leakage current	V_{DS} = 1200 V; V_{GS} = 0 V; T_j = 25 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 22 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 15 V; I_D = 40 A; T_j = 25 °C		-	40	60	mΩ
		V_{GS} = 15 V; I_D = 40 A; T_j = 100 °C		-	42	-	mΩ
		V_{GS} = 15 V; I_D = 40 A; T_j = 175 °C		-	53	-	mΩ
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 40 A; T_j = 25 °C		-	18	-	S
R_G	gate resistance	f = 0.5 MHz; T_j = 25 °C		-	2.8	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DD} = 800 V; I_D = 40 A; V_{GS} = -5/+15 V; T_j = 25 °C		-	84	-	nC
Q_{GS}	gate-source charge			-	34	-	nC
Q_{GD}	gate-drain charge			-	26	-	nC
C_{iss}	input capacitance	V_{DD} = 800 V; f = 0.5 MHz; V_{GS} = 0 V; T_j = 25 °C		-	2600	-	pF
C_{oss}	output capacitance			-	136	-	pF
C_{rss}	reverse transfer capacitance			-	6	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 800 V; I_D = 40 A; $R_{G(ext)}$ = 2.2 Ω; V_{GS} = -5/+15 V; L = 82 µH; T_j = 25 °C		-	57	-	ns
t_r	rise time			-	20	-	ns
$t_{d(off)}$	turn-off delay time			-	22	-	ns
t_f	fall time			-	9	-	ns
E_{on}	turn-on switching loss			-	1413	-	µJ
E_{off}	turn-off switching loss			-	160	-	µJ
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 40 A; V_{GS} = -5 V; T_j = 25 °C		-	4.5	-	V
t_{rr}	reverse recovery time	V_{DD} = 800 V; I_S = 40 A; dI_S/dt = 1649 A/µs; T_j = 25 °C		-	31	-	ns
Q_r	recovered charge			-	217	-	nC

[1] Measured according to JEP183.



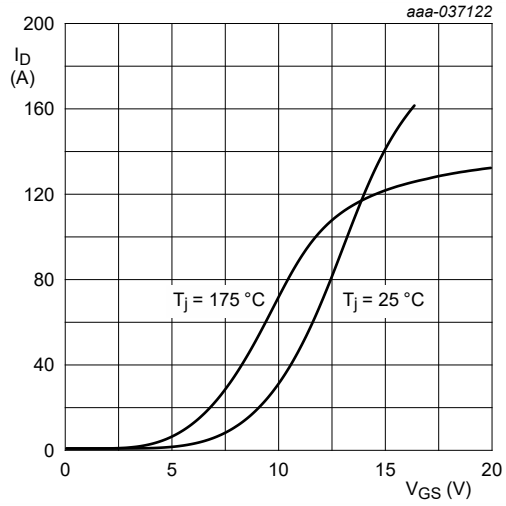
T_j = 25 °C

Fig. 1. Output characteristics: drain current as a function of drain-source voltage; typical values



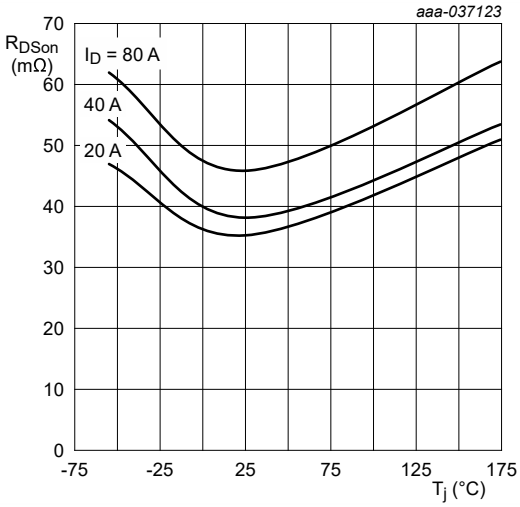
T_j = 175 °C

Fig. 2. Output characteristics: drain current as a function of drain-source voltage; typical values



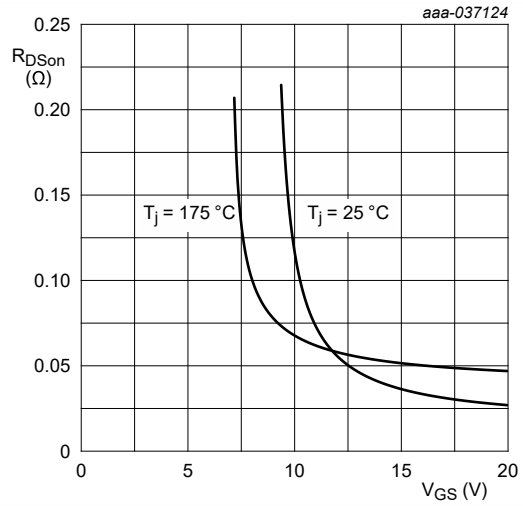
V_{DS} = 10 V; t_p < 300 µs

Fig. 3. Transfer characteristics: drain current as a function of gate-source voltage; typical values



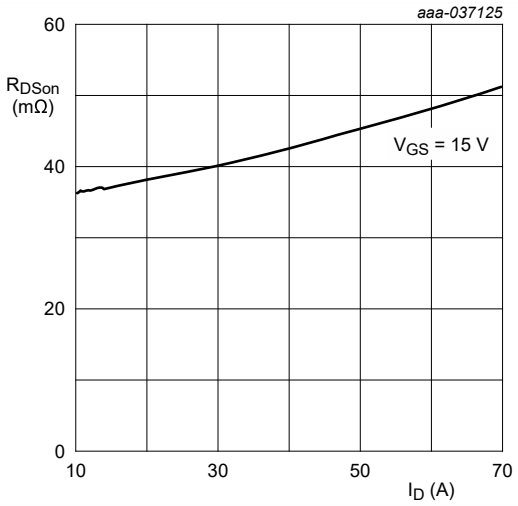
V_{GS} = 15 V; t_p < 300 µs

Fig. 4. Normalized drain-source on-state resistance as a function of junction temperature; typical values



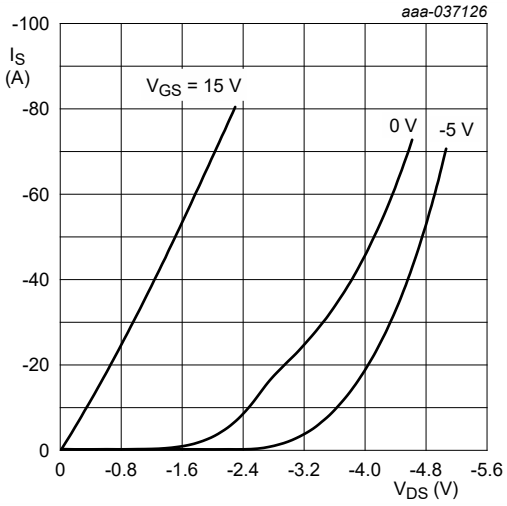
I_D = 20 A

Fig. 5. Drain-source on-state resistance as a function of threshold voltage



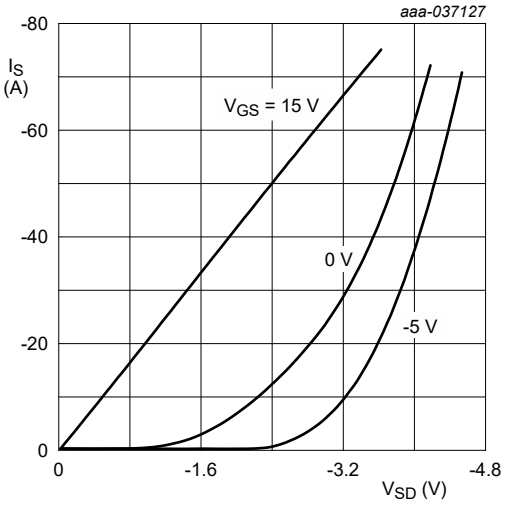
T_j = 25 °C

Fig. 6. Drain-source on-state resistance as a function of drain current; typical values



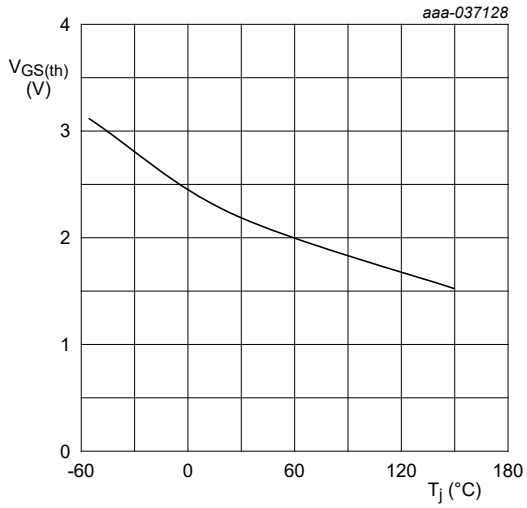
t_p < 300 µs; T_j = 25 °C

Fig. 7. Source current as a function of source-drain voltage; typical values



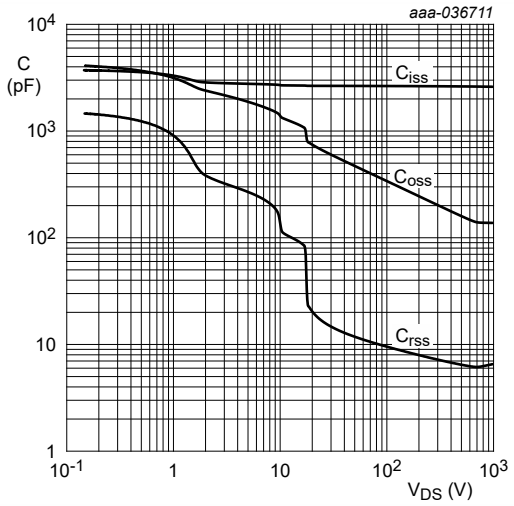
t_p < 300 µs; T_j = 175 °C

Fig. 8. Source current as a function of source-drain voltage; typical values



I_D = 4 mA

Fig. 9. Gate-source threshold voltage as a function of junction temperature; typical values



f = 0.5 MHz; V_{GS} = 0 V; T_j = 25 °C

Fig. 10. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

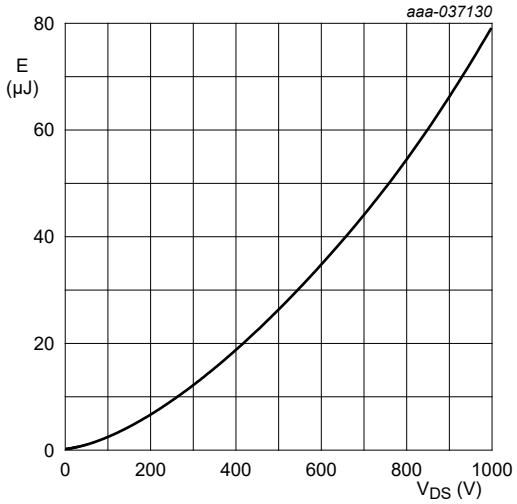
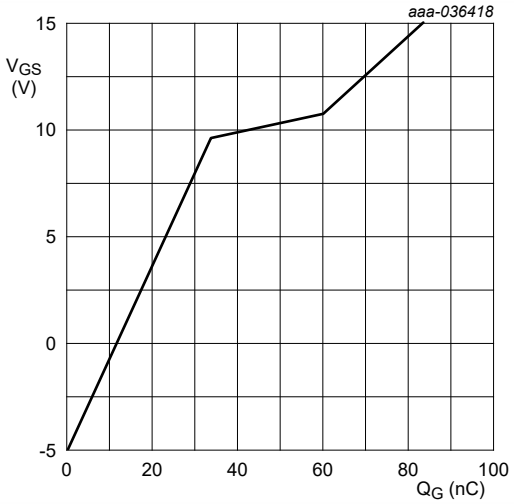
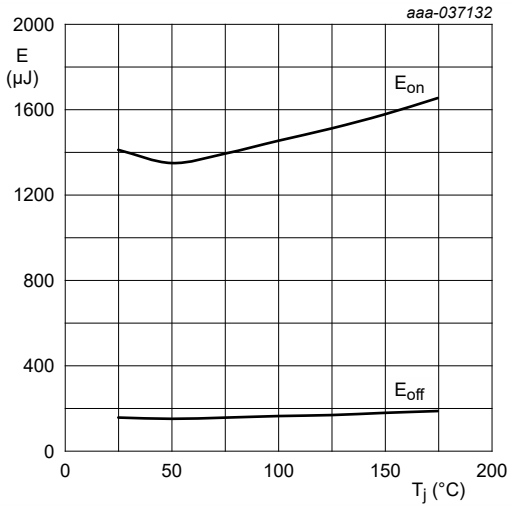


Fig. 11. C_{oss} stored energy as a function of drain-souce voltage; typical values



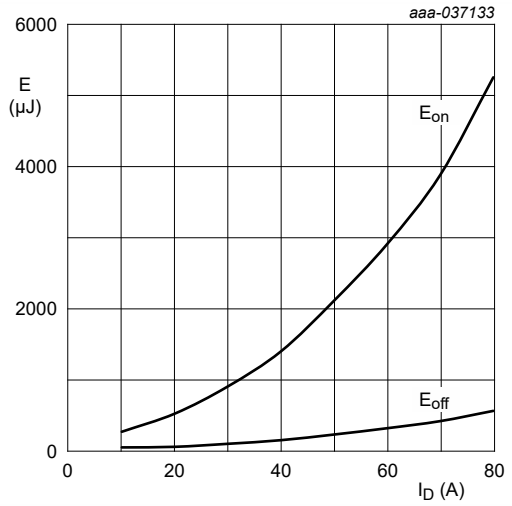
V_{DD} = 800 V; I_D = 40 A; T_{amb} = 25 °C

Fig. 12. Gate-source voltage as a function of gate charge; typical values



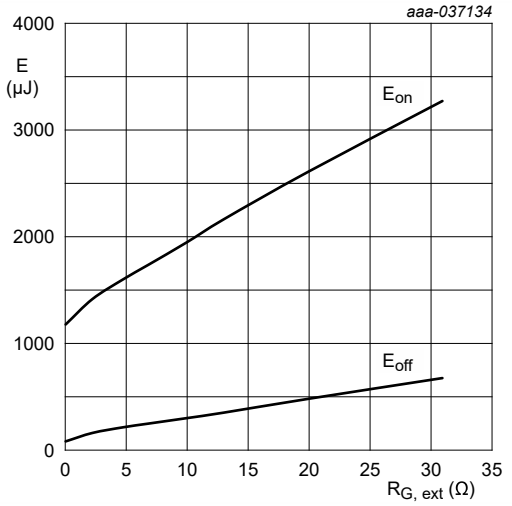
V_{DD} = 800 V; I_D = 40 A; V_{GS} = -5/15 V; $R_{G,\,ext}$ = 2.2 Ω; L = 82 µH

Fig. 13. Switching loss as a function of junction temperature; typical values



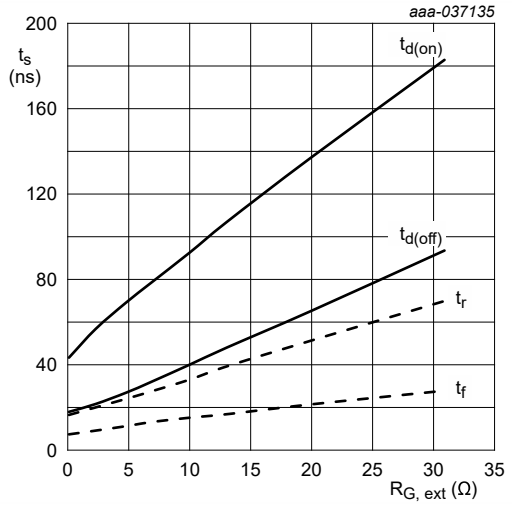
V_{DD} = 800 V; V_{GS} = -5/15 V; $R_{G,\,ext}$ = 2.2 Ω; T_j = 25 °C

Fig. 14. Switching loss as a function of drain current; typical values



V_{DD} = 800 V; I_D = 40 A; V_{GS} = -5/15 V; T_j = 25 °C

Fig. 15. Switching loss as a function of external gate resistance; typical values



V_{DD} = 800 V; I_D = 40 A; V_{GS} = -5/15 V; T_j = 25 °C

Fig. 16. Switching times as a function of external gate resistance; typical values

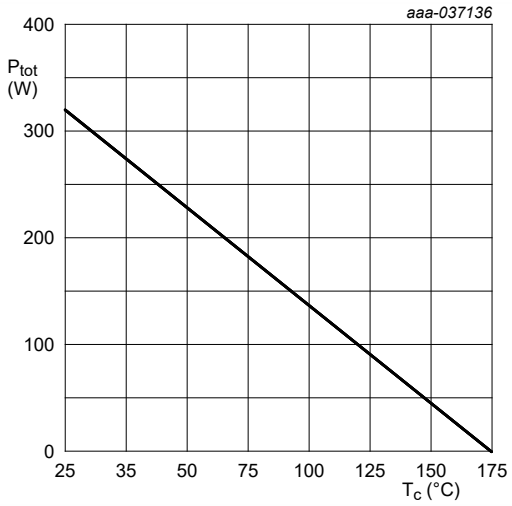


Fig. 17. Power dissipation derating as a function of case temperature; maximum values

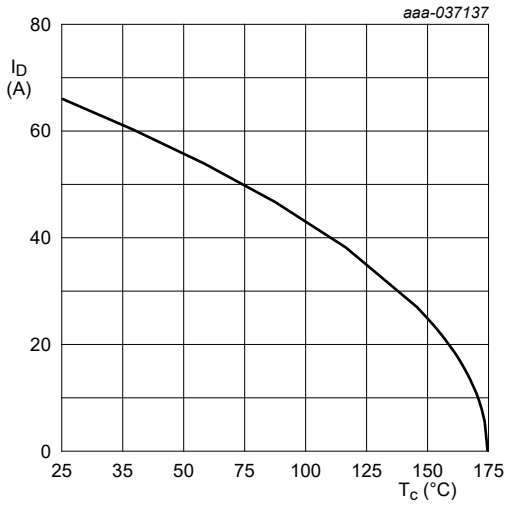


Fig. 18. Continuous drain current as a function of case temperature; maximum values

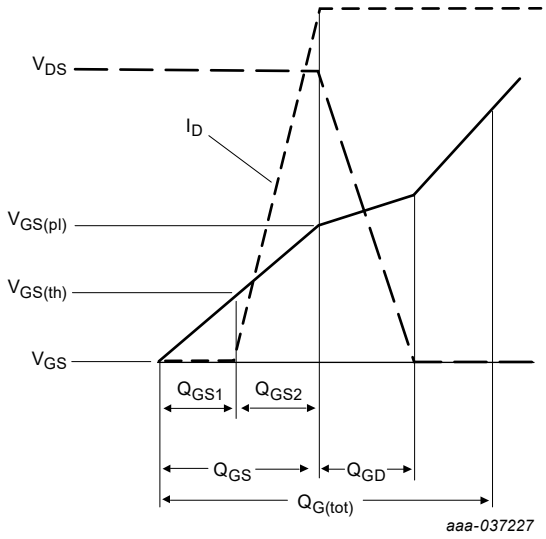


Fig. 19. Gate charge waveform definitions

11. Test information

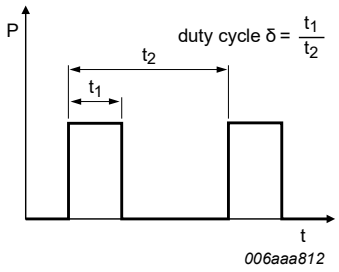
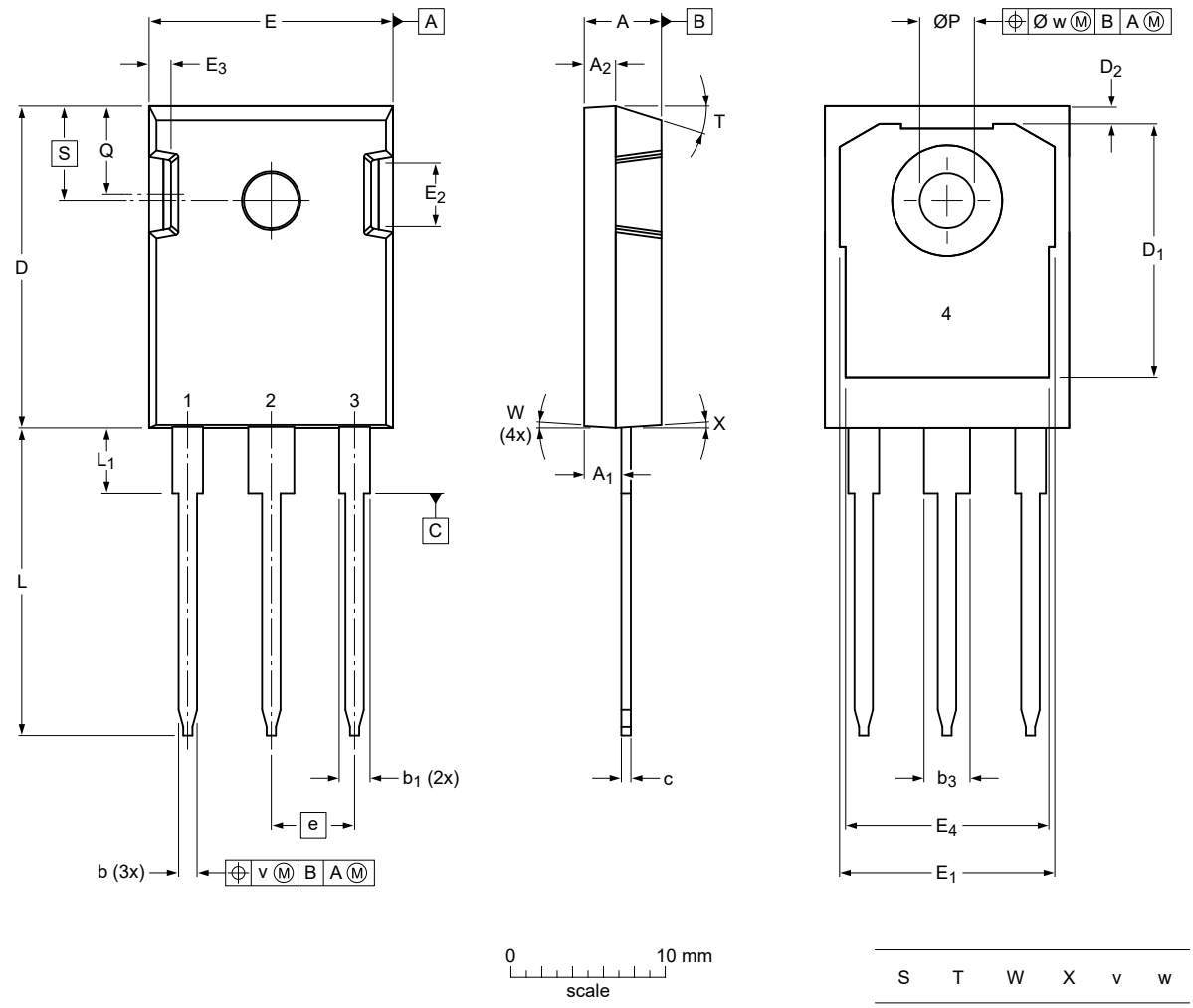


Fig. 20. Duty cycle definition

12. Package outline

Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247-3L **SOT429-2**



S	T	W	X	v	w
6.17 BSC	17.5° REF	3.5° REF	4° REF	0.25	0.64

Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	b_1	b_3	c	D	D_1	D_2	E	E_1	E_2	E_3	E_4	e	L	L_1	P	Q
mm	max	5.21	2.54	2.16	1.33	2.41	3.38	0.68	21.1	17.65	1.25	16.13	14.15	5.1	1.9	13.43	5.44 BSC	20.32	4.4	3.65	6.0
	nom																				
	min	4.83	2.29	1.91	1.07	1.91	2.87	0.55	20.8	16.25	0.95	15.75	13.1	3.68	1.0	12.38		19.81	4.1	3.51	5.49

Note:
All metal surfaces are tin plated except trimmed area

sot429-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT429-2		TO-247-3L				~~22-02-09~~ 22-03-23

Fig. 21. Package outline TO-247-3L (SOT429-2)

13. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NSF040120L3A0 v.3	20231006	Objective data sheet	-	NSF040120L3A0 v.2
Modifications:	• Thermal characteristics: R_{th} values updated.			
NSF040120L3A0 v.2	20230929	Objective data sheet	-	NSF040120L3A0 v.1
Modifications:	• Limiting values: Footnotes adapted and conditions at IDM ISM specified • Characteristics: Conditions adapted at trr and Qrr • Characteristics: Values adapted at "gate resistance", switching times, "reverse recovery time","recovery charge" • Characteristics: Values added for E_{on} and E_{off} • Characteristics: Figures added			
NSF040120L3A0 v.1	202300502	Objective data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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