Evaluating the LTC9101-3/LTC9103 16-Port, IEEE 802.3at PSE Controller with Power Management and LED Control

FEATURES

- 16 Port IEEE 802.3at-compliant PSE
- Autonomous Power Management with flash configuration
- Serial LED driver for Port LEDs

EVALUATION KIT CONTENTS

- EVAL-LTC9101-3-AZ Daughter Card
- EVAL-LTC9101-3-MB-AZ Motherboard

DOCUMENTS NEEDED

LTC9101-3/LTC9103 Datasheet

ADDITIONAL HARDWARE NEEDED

- DC Power Supply
- IEEE 802.3af/at Powered Device(s)

SOFTWARE NEEDED

Contact Analog Devices Applications for information regarding Custom Configurations.

GENERAL DESCRIPTION

The EVAL-LTC9101-3 is a 16-channel IEEE 802.3at compliant power sourcing equipment (PSE) with autonomous power management and serial LED driver for port LEDs. The EVAL-LTC9101-3 includes the EVAL-LTC9101-3-AZ daughter card, the EVAL-LTC9101-3-MB-AZ motherboard, and features the LTC9101-3 and LTC9103 PSE platform chipset.

In the EVAL-LTC9101-3, a single LTC9101-3 digital controller interfaces with up to two LTC9103, 8-channel, analog controllers for 16 power channels total. Up to sixteen IEEE 802.3af/at/bt powered devices (PDs) can be connected to the EVAL-LTC9101-3 and powered from this system using a single power supply.

The LTC9101-3 and LTC9103 use a proprietary isolated data interface allowing the LTC9101-3 to share the same logic supply as the host controller and eliminate the need for an additional isolated 3.3 V supply. The EVAL-LTC9101-3 operates completely autonomously without a host controller, including flash configuration for power management and port LEDs. Port Status and Fault LEDs quickly show PoE status for up to sixteen ports, including fault codes, driven by the LTC9101-3 using a serial LED driver. A Supply Overload LED warns if system power usage is near the power budget and indicates if port power is denied or revoked.

Robust surge protection is provided by design and on-board surge protection devices. An optional on-board buck regulator provides 3.3 V from the VEE supply for the digital circuits. This demonstration manual provides a quick start procedure and an EVAL-LTC9101-3 overview.

Design files for this circuit board are available at https://www.analog.com/EVAL-LTC9101-3

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REVISION HISTORY

7/2023—Revision 0: Initial Version

EVAL-LTC9101-3 EVALUATION BOARD PHOTO

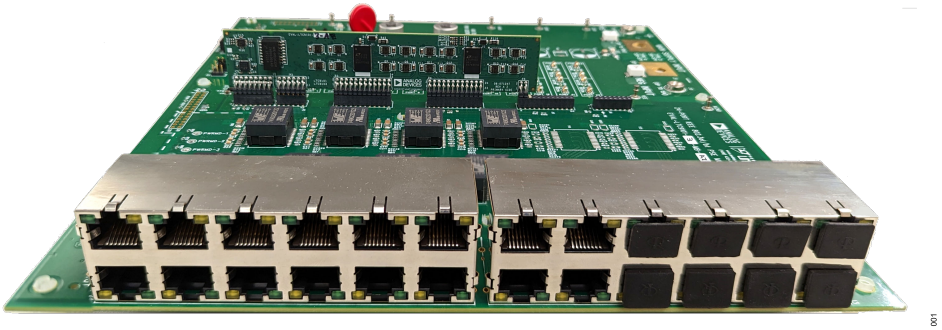

Figure 1. EVAL-LTC9101-3 Evaluation Board Photo

QUICK START PROCEDURE

EVAL-LTC9101-3 Operation

The EVAL-LTC9101-3 includes the EVAL-LTC9101-3-AZ daughter card and EVAL-LTC9101-3-MB-AZ motherboard. This kit allows for evaluating the LTC9101-3/LTC9103 chipset configured as either an 8-port or 16-port, 802.3at PSE endpoint.

Follow the procedure below and refer to Figure 2 through Figure 4, and Table 1 for proper equipment setup and default configuration. This default setup automatically powers all valid PDs.

1. On the EVAL-LTC9101-3-MB-AZ motherboard, set $\overline{\text{LEGACY}}$ jumper JP14 to HI to only power IEEE 802.3 compliant PDs that present a valid detection signature.
2. On the EVAL-LTC9101-3-MB-AZ motherboard, set the CFG1 (JP21) jumper to HI to enable all ports. For CFG1 options see Table 1 .

Table 1. EVAL-LTC9101-3 CFG1 Jumper Settings

Jumper		
CFG1 (JP21)	# of LTC9103s	Max # of Ports
LO	1	8
HI	2	16

3. Align pin 1 of the 16-pin male connector P1 on the EVAL-LTC9101-3-AZ daughter card with pin 1 of the 16-pin female connector J11 on the EVAL-LTC9101-3-MB-AZ motherboard as shown in Figure 2. The five male connectors and five female sockets should match. Keyed pins in J12 assist with the alignment shown in Figure 3. Carefully push the daughter card straight down until the male and female connectors are flush with each other.
4. Connect a supply to the EVAL-LTC9101-3-MB-AZ motherboard with the positive rail to POS INPUT (+) and negative rail to NEG INPUT (-) as shown in Figure 3. Use a power supply capable of sourcing the system power budget, refer to Table 1. Ramp the supply up to within 51 V and 57 V.

   NOTE: At start up, the Supply Overload LED ($\overline{\text{OVR}}$), Status LEDs (Green LEDs on J3 and J4), and Fault LEDs (Yellow LEDs on J3 and J4) go through a default self test pattern. The power on self test pattern will be repeated on a LTC9101-3 reset. This does not affect PoE operation and the LEDs will be valid once the test pattern is complete.
5. Connect up to sixteen IEEE 802.3af/at/bt PDs to the motherboard's RJ45 connectors J3 and J4, as shown in Figure 4.

   NOTE: RJ45 ports 17, 18, 19, 20, 21, 22, 23 and 24 on J3 are blocked on the EVAL-LTC9101-3-MB-AZ motherboard in the EVAL-LTC9101-3. See the section on Port Output for more information.

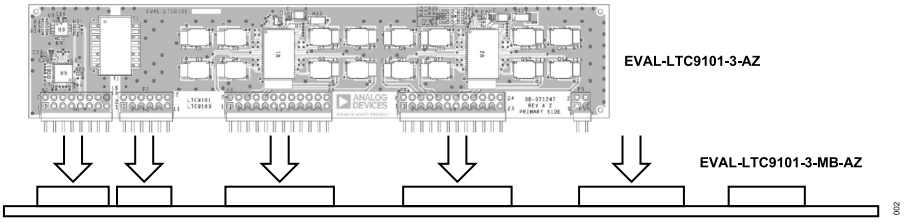

Figure 2. Inserting the EVAL-LTC9101-3-AZ Daughter Card into J1 through J5 of the EVAL-LTC9101-3-MB-AZ Motherboard

QUICK START PROCEDURE

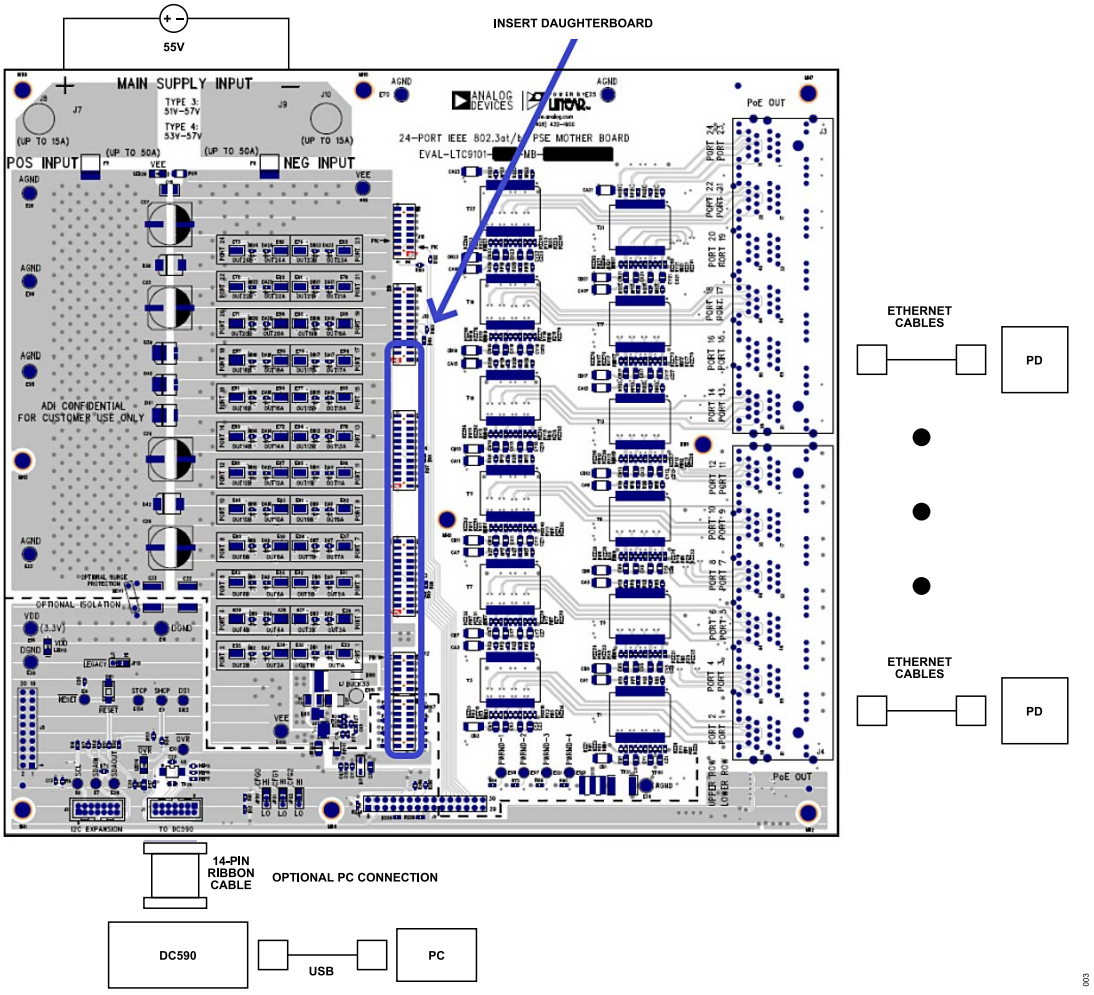

Figure 3. EVAL-LTC9101-3 Connections

LTC9101-3 EVALUATION KIT

EVAL-LTC9101-3 includes the EVAL-LTC9101-3-MB-AZ, 16-Port, 2-pair IEEE 802.3at PoE PSE motherboard for a PSE endpoint. This motherboard accepts an EVAL-LTC9101-3-AZ daughter card with sixteen power channels. It contains two, 2×6, RJ45 connectors and sixteen 1000BASE-T Ethernet transformers rated for PoE operation. The EVAL-LTC9101-3-MB-AZ motherboard also has switches, jumpers, and pushbuttons for configuring the PSE, with port LEDs and test points.

PORT OUTPUT

The PDs are connected using an Ethernet cable (Cat5, Cat5e or better cabling as specified by IEEE 802.3) to any of the valid ports at the two, 2×6, RJ45 connectors J3 and J4 on the EVAL-LTC9101-3-MB-AZ motherboard. The LTC9101-3/LTC9103 delivers power over one power channel. The term “channel” refers to the PSE circuitry assigned to a corresponding pairset. Each port is connected as a 2-pair port driven by a single power channel connected to Alternative A (pairs 1, 2 and 3, 6). Alternative B (pairs 4, 5 and 7, 8) is unpowered. Each port has a test point OUTnA which connects to Alternative A, pair 1, 2 for port n.

An IEEE 802.3at PSE uses a single power channel per port, connected to either Alternative A or Alternative B. EVAL-LTC9101-3-MB-AZ layout supports up to twenty four 4-pair ports with options for connecting Alternative A and Alternative B.

The EVAL-LTC9101-3 supports sixteen, 2-pair ports. Refer to See-Figure 4 for the port output map of the EVAL-LTC9101-3.

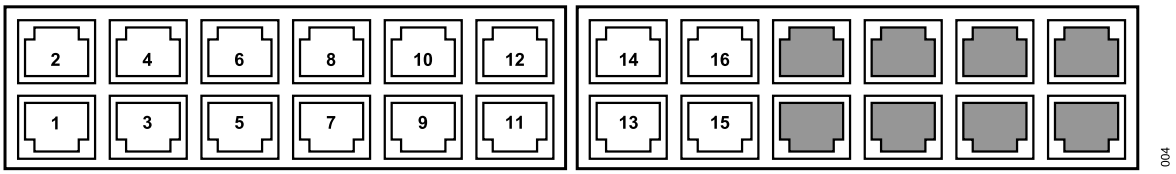

Figure 4. EVAL-LTC9101-3 Port Output Map

LTC9101-3 EVALUATION KIT

DAUGHTER CARD INSERTION PRECAUTIONS

When inserting or removing the daughter card into the EVAL-LTC9101-3-MB-AZ motherboard, verify all supplies and LEDs are off. Push the card straight down for insertion or pull straight up for removal to avoid bending the connector pins. Follow the instructions in the Quick Start Procedure for alignment and see Figure 2.

MAIN VEE POE SUPPLY

The VEE supply is the main PoE supply connected to the EVAL-LTC9101-3-MB-AZ motherboard. For proper connection and appropriate supply voltage ranges see Quick Start Procedure.

Choose a power supply with a limit set higher than the maximum system power budget. The banana jacks (J8 and J10) are sufficient for up to 15 A.

ISOLATION

The IEEE 802.3 Ethernet specifications require network segments (including the analog PoE circuitry) to be electrically isolated from the chassis ground. The EVAL-LTC9101-3-MB-AZ motherboard and EVAL-LTC9101-3-AZ daughter card layouts and high voltage capacitors provide an isolation barrier between Analog and Digital domains. Transformers provide a galvanic barrier between DGND and AGND on the EVAL-LTC9101-3-AZ daughter card. By default, this isolation barrier is bridged by resistors on the motherboard to allow for evaluation using a single power supply. Remove RISO1 and RISO2, then provide an external 3.3 V supply between V_{DD} and DGND to evaluate this board as an isolated system.

All RJ45 shields and terminations are connected to the chassis ground. AGND and V_{EE} each connect to the chassis ground with two pairs of 1 nF, 2 kV capacitors (C6-C9). AGND and V_{EE} also connect to DGND each with 10 nF, 2 kV capacitors (C32-C33). An optional 0 Ω resistor can be installed at RISO3 to tie the chassis ground to DGND. Two series 1206, 5.1 MΩ resistors connect between AGND and DGND for high voltage capacitance discharge. See Figure 5 for diagram of connections between Analog and Digital domains, as well as chassis ground on the EVAL-LTC9101-3-MB-AZ motherboard.

The EVAL-LTC9101-3-AZ daughter card is laid out with isolation.

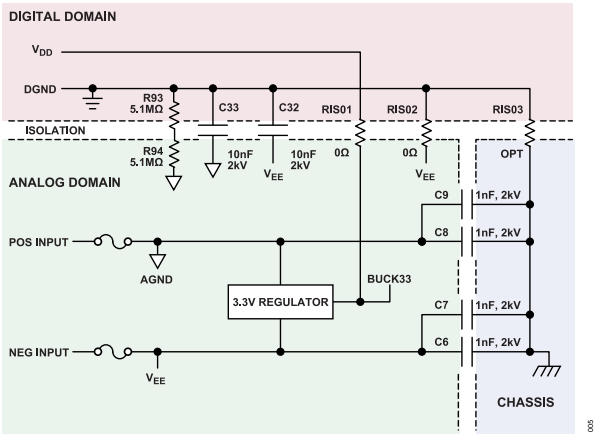

Figure 5. Motherboard Power Supply Connections and Isolation Barriers

LED INDICATORS

The V_{EE} LED (D29) and V_{DD} LED (LED13) indicate if a voltage is present at the respective supplies. Verify these LEDs are off before inserting or removing the daughter card.

Each port has respective Status and Fault LEDs to indicate different states. Status is connected to a green LED while Fault is connected to a yellow LED. For default Port LED behavior see Table 2. The Supply Overload LED ($\overline{OVR}$, LED14) indicates if power has been denied, revoked, or if the system is near the power budget. Status, Fault, and Supply Overload LED functions can be modified with a custom configuration package.

LTC9101-3 EVALUATION KIT

Table 2. Default PoE Operation vs. port LEDs

	LED	
Condition	**Port Status**	**Port Fault**
Detect Open	Off	Off
Port Powered	On	Off
Detect Invalid	Off	Blink
Class Invalid	Off	Blink
Inrush Fault	Off	Blink
P_{CUT}, I_{CUT} and I_{LIM}	Off	Blink
DC Disconnect	Off	Blink
Power Denied	Blink	Off
Power Revoked	Blink	Off

NOTE: Blink rate is 800ms on and 800ms off.

DEVICE CONFIGURATION

The CFG1 pin state during reset configures the number of analog controllers in the system. The CFG1 pin connects to a jumper that pulls either HI for a logical 1, or LO for logical 0. See Table 1 for the numbers of ports and LTC9103s set by CFG1 pin. CFG1 pin also sets the default system power budget and near-limit warning thresholds. See Power Management section for more information. The CFG0 and CFG2 jumpers must be set LO, to set the CFG0 and CFG2 pins to a logical 0.

CUSTOM CONFIGURATIONS

An LTC9101-3/LTC9103 system may be configured in a variety of ways by storing a custom configuration package in a dedicated flash partition. If a stored configuration is utilized, CFG1 is still required to inform the LTC9101-3 how many analog controllers are in the system. Refer to the data sheet for more information and contact ADI Applications for assistance with generating custom configuration packages.

DIGITAL CONNECTIONS

The DC590 USB to I^2C controller board is connected to the EVAL-LTC9101-3-MB-AZ motherboard at J1 through a 14-pin ribbon cable. The LTC9101-3's I^2C base address is 0x20. SDAOUT and SDAIN can be tied together through a shunt resistor, R73. Turrets on the EVAL-LTC9101-3-MB-AZ motherboard provide test points for SCL, SDAIN, SDAOUT, V_{DD}, DGND, and $\overline{\text{RESET}}$.

$\overline{\text{RESET}}$ PUSHBUTTON

Pushbutton switch SW1, when pressed, pulls the $\overline{\text{RESET}}$ pin of the daughter card logic low. The PSE controller is then held inactive with all ports off. When SW1 is released, $\overline{\text{RESET}}$ is pulled high, and the PSE returns to autonomous operation while $\overline{\text{OVR}}$, Status, and Fault LEDs run through the LED power on self test.

ONBOARD 3.3 V SUPPLY

The EVAL-LTC9101-3-MB-AZ motherboard has an onboard (non-isolated) 3.3 V/1 A buck regulator that provides a local 3.3 V, with the net named BUCK33. This onboard logic supply is for demonstration purposes only and allows for use of a single supply while evaluating the EVAL-LTC9101-3.

SURGE TESTING

The EVAL-LTC9101-3 can be configured with either the Digital domain connected to reference ground plane, or with the Digital domain floating with the Analog domain for different surge test setups. The default EVAL-LTC9101-3 configuration has DGND connected to V_{EE} and floating from chassis ground.

LEGACY MODE

Legacy Mode operation is enabled with the $\overline{\text{LEGACY}}$ pin, which is controlled by the $\overline{\text{LEGACY}}$ jumper (JP15). If the $\overline{\text{LEGACY}}$ jumper is LO, Legacy mode is enabled and legacy PDs with large common-mode capacitance (>10 µF) will be powered. If the $\overline{\text{LEGACY}}$ jumper is HI or floating, legacy mode is disabled and only valid IEEE 802.3 PDs will be powered. The $\overline{\text{LEGACY}}$ pin state is continuously monitored.

LTC9101-3 EVALUATION KIT

POWER MANAGEMENT

The LTC9101-3 manages a user-defined system-level power budget across all ports. Port power is automatically assigned based on system power availability, initial physical classification and after power-up, port dynamic power consumption. The default system power budget is based off the maximum number of ports in the system, which is set by the CFG1 pin. See Table 3 for the default power management settings. The Supply Overload ($\overline{OVR}$) LED turns on if it is near the power budget and blink if power is denied or revoked. The LTC9101-3 prioritizes port power by port number, sequentially (port 1 is highest priority). Refer to the data sheet for more information on the Power Management algorithm. The system power budget, warning levels, and port priority can be modified with a custom configuration package.

Table 3. Default System Power Budget and Near-Limit Warning Thresholds

CFG1	Total Number of Ports	System Power Budget	Set Power Warning ($\overline{OVR}$ LED Turns On)	Power Warning Reset ($\overline{OVR}$ LED Turns Off)
LO	8	64 W	49 W	45 W
HI	16	128 W	113 W	109 W

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.