Revision History

For 2Gbit /4Gbit/8Gbit LPDDR4X SDRAM 200ball FBGA Package

Revision	Details	Date
Rev 1.0	Initial Release	Mar 2021
Rev 1.1	Add 2Gb,4Gb LPDDR4X	Apr 2023

1 Overview

The Alliance LPDDR4X SDRAM is organized as 1 or 2 channels per device, and individual channel is 8-banks and 16-bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 16n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 16n bits prefetched to achieve very high bandwidth.

1.1 Features

The 2Gbit /4Gbit/8Gbit LPDDR4X SDRAM offers the following key features:

- Configuration:
  - x32 for 2-channels per device (AS4C256M32MD4V)
  - x16 for 1-channel per device (AS4C128M16MD4V/AS4C256M16MD4V)
  - 8 internal banks per each channel
- On-Chip ECC:
  - Single-bit error correction (per 64-bits), which will maximize reliability
  - Optional ERR output signal per channel, which indicates ECC event occurrence
  - ECC Register, which controls ECC function
- Low-voltage Core and I/O Power Supplies:
  - V_{DD2} = 1.06-1.17V, V_{DDQ} = 0.57-0.65V, V_{DD1} = 1.70-1.95V
- LVSTL(Low Voltage Swing Terminated Logic) I/O Interface
- Internal VREF and VREF Training
- Dynamic ODT :
  - DQ ODT :VSSQ Termination
  - CA ODT :VSS Termination
- Selectable output drive strength (DS)
- Max. Clock Frequency : 1.6GHz (3.2Gbps for one channel)
- 16-bit Pre-fetch DDR data bus
- Single data rate (multiple cycles) command/address bus
- Bidirectional/differential data strobe per byte of data (DQS, $\overline{DQS}$)
- DMI pin support for write data masking and DBI functionality
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL =16, 32)
- Support non-targert DRAM ODT control
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- ZQ Calibration
- Operation Temperature:
  - Automotive A2 (TC = -40°C to 105°C)
- On-chip temperature sensor to control self refresh rate
- On-chip temperature sensor whose status can be read from MR4
- 200-ball x16/x32 Discrete Package (0.80mm x 0.65mm)
- RoHS-compliant, “green” packaging

Table 1. Speed Grade Information

Speed Grade	Clock Frequency	Data Rate (Mb/s)	Read Latency (RL)	tCK (ns)
LPDDR4X-3200	1600MHz	3200	28	0.625

*Other clock frequencies/data rates supported; please refer to AC timing tables.

1.2 Product List

Table 2 shows all possible products within the 2Gbit/4Gbit/8Gbit LPDDR4X SDRAM component generation. Availability depends on application needs.

Table 2 - Ordering Information for 2Gbit/4Gbit/8Gbit LPDDR4X Components

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C128M16MD4V-062BAN	128M x 16	Automotive -40°C to 105°C	1600	200-ball FBGA
AS4C256M16MD4V-062BAN	256M x 16	Automotive -40°C to 105°C	1600	200-ball FBGA
AS4C256M32MD4V-062BAN	256M x 32	Automotive -40°C to 105°C	1600	200-ball FBGA

1.3 Addressing

Table 3 - 2Gbit/4Gbit/8Gbit LPDDR4X SDRAM Addressing

Memory Density		**2Gb**	**4Gb**	**8Gb**
Organization		x16	x16	x32
Number of Channels		1	1	2
Density per channel		2Gb	4Gb	4Gb
Configuration		16Mb x 16DQ x 8 banks x 1 channel	32Mb x 16DQ x 8 banks x 1 channel	32Mb x 16DQ x 8 banks x 2 channels
Number of Banks (per Channel)		8	8	8
Array Pre-Fetch (Bits, per channel)		256	256	256
Number of Rows (per channel)		16,384	32,768	32,768
Number of Columns (fetch boundaries)		64	64	64
Page Size (Bytes)		2,048	2,048	2048
Bank Address		BA0-BA2	BA0-BA2	BA0-BA2
X16	Row Addresses	R0-R13	R0-R14	R0-R14
	Column Addresses	C0-C9	C0-C9	C0-C9
Burst Starting Address Boundary		64-bit	64-bit	64-bit

NOTE 1 The lower two column addresses (C0 - C1) are assumed to be “zero” and are not transmitted on the CA bus.
NOTE 2 Row and Column address values on the CA bus that are not used for a particular density be at valid logic levels.
NOTE 3 For non - binary memory densities,only half of the row address space is valid. When the MSB address bit is “HIGH”, then the MSB - 1 address bit must be “LOW”.
NOTE 4 The row address input which violates restriction described in note 3 may result in undefined or vendor specific behavior. Consult memory vendor for more information.

1.4 Package Block Diagram

Figure 1 – Dual Channel Package Block Diagram

Part number: AS4C256M32MD4V

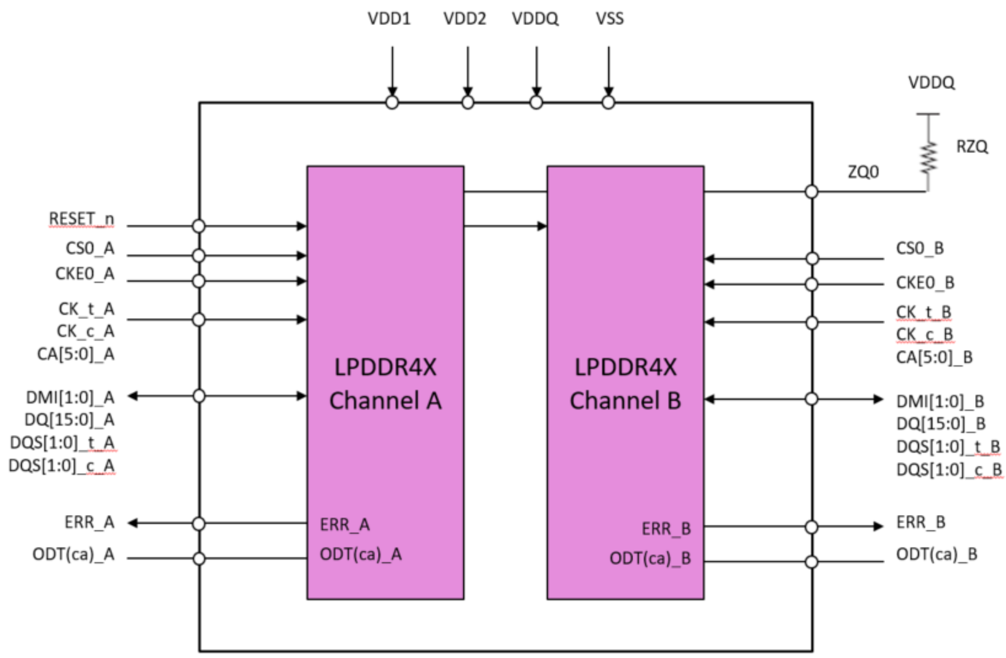
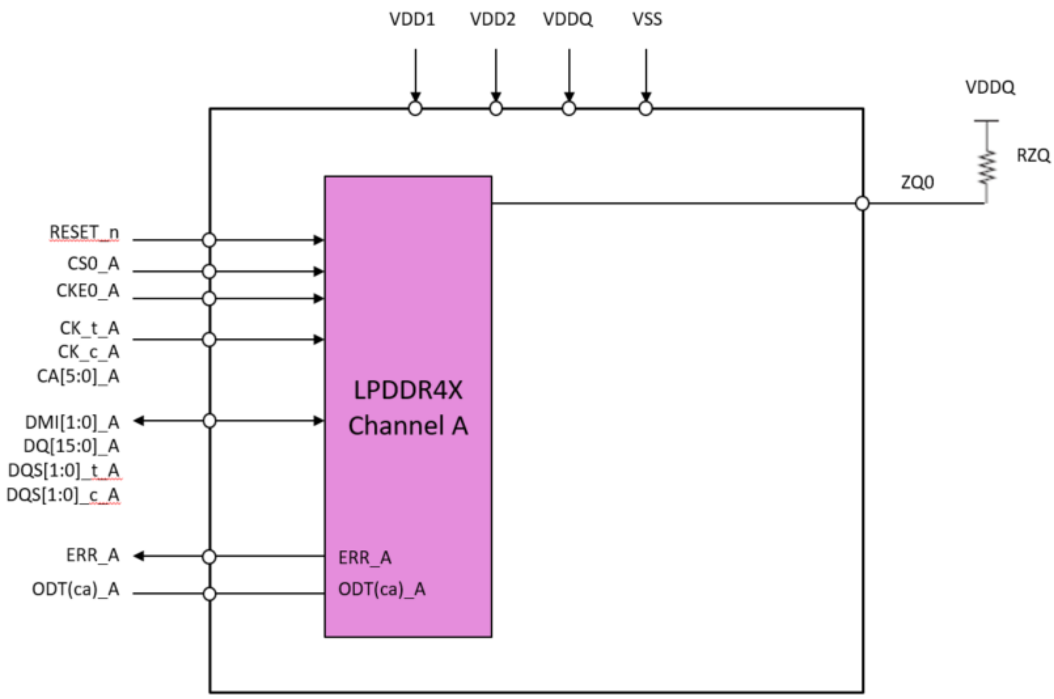


Figure 2 – Single Channel Package Block Diagram

Part number: AS4C128M16MD4V / AS4C256M16MD4V



1.5 Package Ballout

Figure 3 - 200-ball x32 Discrete Package, 0.80mm x 0.65mm using MO-311

0.80mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	VSS	VDD2	ZQ0			NC	VDD2	VSS	ERR_A	NC
B	NC	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	NC
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_T_A	VSS	VDDQ			VDDQ	VSS	DQS1_T_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_C_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_C_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT_CA_A	VSS	VDD1	VSS			VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_A	NC	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	NC			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	NC			CK_t_B	CK_c_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	NC	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_CA_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_C_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_C_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_T_B	VSS	VDDQ			VDDQ	VSS	DQS1_T_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	NC	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	NC
AB	NC	NC	VSS	VDD2	VSS			VSS	VDD2	VSS	ERR_B	NC

NOTE 1 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.
NOTE 2 Top View, A1 in top left corner.
NOTE 3 ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT_CA_[x] pads for other ranks (if present) are disabled in the package.
NOTE 4 Die pad VSS and VSSQ signals are combined to VSS package balls.
NOTE 5 11A and 11AB are optional ERR signals.

Figure 4 - 200-ball x16 Discrete Package, 0.80mm x 0.65mm using MO-311

0.80mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	VSS	VDD2	ZQ0			NC	VDD2	VSS	ERR_A	NC
B	NC	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	NC
C	VSS	DQ1 _A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1 _A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_T_A	VSS	VDDQ			VDDQ	VSS	DQS1_T_A	VSS	VDDQ
E	VSS	DQ2 _A	DQS0_C_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_C_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11 _A	VDD1
G	VSS	ODT_CA_A	VSS	VDD1	VSS			VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_ A	NC	CS0_A	VDD2			VDD2	CA2 _A	CA3 _A	CA4 _A	VDD2
J	VSS	CA1 _ A	VSS	CKE0_A	NC			CK_t_A	CK_ c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
P	VSS	NC	VSS	NC	NC			NC	NC	VSS	NC	VSS
R	VDD2	NC	NC	NC	VDD2			VDD2	NC	NC	NC	VDD2
T	VSS	NC	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	NC	VDDQ	NC	VDD2			VDD2	NC	VDDQ	NC	VDD1
V	VSS	NC	NC	NC	VSS			VSS	NC	NC	NC	VSS
W	VDDQ	VSS	NC	VSS	VDDQ			VDDQ	VSS	NC	VSS	VDDQ
Y	VSS	NC	NC	NC	VSS			VSS	NC	NC	NC	VSS
AA	NC	NC	VDDQ	NC	VDDQ			VDDQ	NC	VDDQ	NC	NC
AB	NC	NC	VSS	VDD2	VSS			VSS	VDD2	VSS	NC	NC

NOTE 1 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.
NOTE 2 Top View, A1 in top left corner.
NOTE 3 ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT_CA_[x] pads for other ranks (if present) are disabled in the package.
NOTE 4 Die pad VSS and VSSQ signals are combined to VSS package balls.
NOTE 5 11A is optional ERR signal.

1.6 Pin Functional Description

Table 4 - Pin Functional Description

Symbol	Type	Function
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A CKE_B	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A CS_B	Input	**Chip Select:** CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A CA[5:0]_B	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is ignored by LPDDR4X devices. ODT-CS/CA/CK function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either V_{DD2} or V_{SS}.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data Input/Output:** Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	**Data Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to V_{DDQ} through a 240Ω ± 1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2}	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	**Ground Reference:** Power supply ground reference.
RESET_n	Input	**RESET:** When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.

NOTE 1 "_A" and "_B" indicate DRAM channel "_A" pads are present in all devices. "_B" pads are present in dual channel SDRAM devices only.

1.7 Command truth table

Command Truth Table

	SDR Command Pins	SDR CA Pins (6)							
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
Deselect (DES)	L	X						R1	1,2
Multi-Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,9,13
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Precharge (PRE) (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Refresh (REF) (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Self Refresh Entry (SRE)	H	L	L	L	H	H	V	R1	1,2
	L	V						R2	
Write -1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9,13
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write -1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5,6,9,13
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9,13
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2, Mask Write -2, Read-2, MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
CAS-2 Non-target ODT	L	L	H	L	L	H	V	R1	1,2,3,14
	L	V						R2	
RFU	H	L	H	L	H	L	V	R1	1,2
	L	V						R2	
RFU	H	L	H	L	H	H	V	R1	1,2
	L	V						R2	
Mode Register Write -1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12,13
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
RFU	H	L	H	H	H	H	V	R1	1,2
	L	V						R2	
Activate -1 (ACT-1)	H	H	L	R12	R13	R14	R15	R1	1,2,3,10
	L	BA0	BA1	BA2	R16	R10	R11	R2	
Activate -2 (ACT-2)	H	H	H	R6	R7	R8	R9	R1	1,10
	L	R0	R1	R2	R3	R4	R5	R2	

NOTE1 All LPDDR4 commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
NOTE2 "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CA[5:0] can be floated.
NOTE3 Bank addresses BA[2:0] determine which bank is to be operated upon.
NOTE4 AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.
NOTE5 Mask Write-1 command supports only BL 16. For Mark Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).
NOTE6 AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an Auto-Precharge will occur to the bank associated with the Write, Mask Write or Read command.
NOTE7 If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-Fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
NOTE8 For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
NOTE9 Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.

NOTE10 Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
NOTE11 MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
NOTE12 MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.
NOTE13 The Non-Target DRAM function is supported for Write-1, Mask Write-1, Read-1, Mode Register Read-1, MPC (only Write FIFO, Read FIFO and Read DQ calibration) command. And CAS-2 is not needed for Non-Target DRAM and CAS-2 Non-target ODT is used instead. The Non-Target DRAM function as optional feature. Refer to vendor specific datasheets.
NOTE14 Write-1, Mask Write-1, Read-1, Mode Register Read-1, MPC (only Write FIFO, Read FIFO and Read DQ calibration) command must be immediately followed by CAS-2 Non-target ODT command consecutively without any other command in between. Write-1, Mask Write-1, Read-1, Mode Register Read-1, MPC (only Write FIFO, Read FIFO and Read DQ calibration) command must be issued first before issuing CAS-2 Non-target ODT command.

1.8 Power-up, Initialization and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as **Table 5.**

Table 5 - MRS defaults settings

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00_B	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0_B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000_B	WL = 4
RL	MR2 OP[2:0]	000_B	RL = 6, nRTP=8
nWR	MR1 OP[6:4]	000_B	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00_B	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000_B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000_B	DQ ODT is disabled
V_{REF}(CA) Setting	MR12 OP[6]	1_B	V_{REF}(CA) Range[1] enabled
V_{REF}(CA) Value	MR12 OP[5:0]	011101_B	Range1: 50.3% of V_{DDQ}
V_{REF}(DQ) Setting	MR14 OP[6]	1_B	V_{REF}(DQ) Range[1] enabled
V_{REF}(DQ) Value	MR14 OP[5:0]	011101_B	Range1: 50.3% of V_{DDQ}

1.8.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4X device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW ($\leq$0.2 x V_{DD2}) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in **Table 6**. V_{DD1} must ramp at the same time or earlier than V_{DD2}. V_{DD2} must ramp at the same time or earlier than V_{DDQ}.

Table 6 - Voltage Ramp Conditions

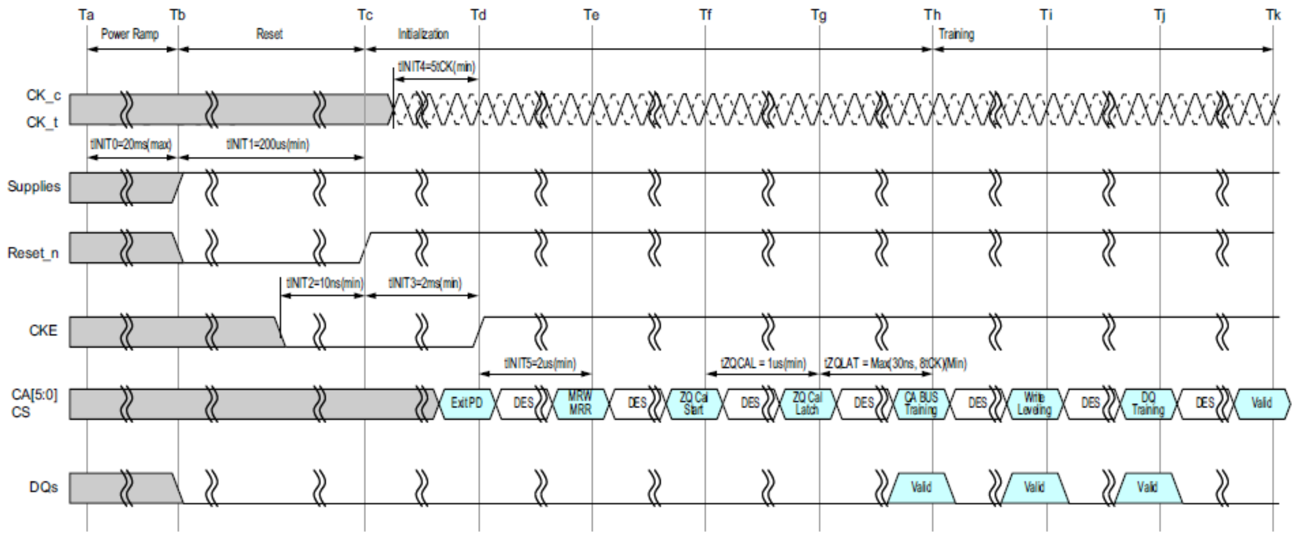
After	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200 mV

NOTE 1 Ta is the point when any power supply first reaches 300 mV.
NOTE 2 Voltage ramp conditions in Table 8 apply between Ta and power-off (controlled or uncontrolled).
NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.
NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
NOTE 5 The voltage difference between any of V_{SS} and V_{SSQ} pins must not excess 100 mV.

2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch- up. CKE, CK_t, CK_c, CS_n and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be deasserted to HIGH(Tc). At least 10ns before RESET_n de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".

1.8.1 Voltage Ramp and Device Initialization (cont'd)



NOTES : 1. Training is optional and may be done at the system architects discretion. The training sequence after ZQ_CAL Latch(Th, Sequence7~9) in Figure 5 is simplified recommendation and actual training sequence may vary depending on systems.

Figure 5 - Power Ramp and Initialization Sequence

4. After RESET_n is de-asserted(Tc), wait at least tINIT3 before activating CKE. Clock(CK_t,CK_c) is required to be started and stabilized for tINIT4 before CKE goes active(Td). CS is required to be maintained LOW when controller activates CKE.

5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands(Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory(Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4X DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4X device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

7. After tZQLAT is satisfied (Th) the command bus (internal V_{REF}(CA), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal V_{REF} and align CS/CA with CK for high-speed operation. The LPDDR4X device will power-up with receivers configured for low-speed operations, and V_{REF}(CA) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

   NOTE The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See 4.29, (item 1.), MRW for information on how to enter/exit the training mode.

8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high (Ti). See 4.31, Mode Register Write-WR Leveling Mode, for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS_t/_c timing to the point where the LPDDR4X device recognizes the start of write DQ data burst with desired write latency.

9. After write leveling, the DQ Bus (internal V_{REF}(DQ), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust V_{REF}(DQ)(Tj). The LPDDR4X device will power-up with receivers configured for low-speed operations and V_{REF}(DQ) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train

DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.

10. At Tk the LPDDR4X device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

Table 7 - Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	-	20	ms	Maximum voltage-ramp time
tINIT1	200	-	us	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	-	ns	Minimum CKE low time before RESET_n high
tINIT3	2	-	ms	Minimum CKE low time after RESET_n high
tINIT4	5	-	tCK	Minimum stable clock before first CKE high
tINIT5	2	-	us	Minimum idle time before first MRW/MRR command
tZQCAL	1	-	us	ZQ calibration time
tZQLAT	Max(30ns, 8tCK)	-	ns	ZQCAL latch quiet time.
tCKb	Note *1,2	Note *1,2	ns	Clock cycle time during boot

NOTE 1 Min tCKb guaranteed by DRAM test is 18 ns.
NOTE 2 The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

1.8.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 x V_{DD2} anytime when reset is needed. RESET_n needs to be maintained for minimum tPW_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET_n.
2. Repeat steps 4 to 10 in1.6.1.

Table 8 - Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RESET	100	-	ns	Minimum RESET_n low Time for Reset Initialization with stable power

1.8.3 Power-off Sequence

The following procedure is required to power off the device.
While powering off, CKE must be held LOW (0.2 X V_{DD2}) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. RESET_n, CK_t, CK_c, CS and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Table 9 - Power Supply Conditions

After	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200 mV

The voltage difference between any of V_{SS}, V_{SSQ} pins must not exceed 100 mV.

1.8.4 Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/μs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 10 - Timing Parameters Power Off

Symbol	Value		Unit	Comment
	Min	Max		
tPOFF	-	2	s	Maximum Power-off ramp item

1.9 Mode Register Definition

Table 11 shows the mode registers for LPDDR4X SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table 11 - Mode Register Assignment in LPDDR4X SDRAM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	Reserved	RFU	RFU	RZQI		RFU	RFU	Refresh mode
1	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	WR Lev	WLS	WL			RL		
3	DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL
4	TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		
5	LPDDR4X Manufacturer ID							
6	Revision ID-1							
7	Revision ID-2							
8	IO Width		Density				Type	
9	Vendor Specific Test Register							
10	RFU							ZQ-Reset
11	RFU	CA ODT			RFU	DQ ODT		
12	CBT Mode	VR-CA	V_{REF}(CA)					
13	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	RFU	VR(dq)	V_{REF}(DQ)					
15	Lower-Byte Invert Register for DQ Calibration							
16	PASR Bank Mask							
17	PASR Segment Mask							
18	DQS Oscillator Count - LSB							
19	DQS Oscillator Count - MSB							
20	Upper-Byte Invert Register for DQ Calibration							
21	RFU							
22	ODT for x8_2ch(Byte) mode		ODTD-CA	ODTE-CS	ODTE-CK	CODT		
23	DQS interval timer run time setting							
24	TRR Mode	TRR Mode BAn			Unlimited MAC	MAC Value		
25	PPR Resource							
26	RFU							
27	RFU							
28	RFU							
29	RFU							
30	Reserved for testing - SDRAM will ignore							
31	RFU							
32	DQ Calibration Pattern “A” (default = 5AH)							
33	ECC control							
34	ECC error count							
35	RFU							
36	RFU							
37	RFU							
38	RFU							
39	Reserved for testing - SDRAM will ignore							
40	DQ Calibration Pattern “B” (default = 3CH)							

MR0 Register Information (MA[5:0] = 00_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved	RFU	RFU	RZQI		RFU	Latency Mode	Refresh mode

Function	Register Type	Operand	Data	Notes
Refresh mode	Read-only	OP[0]	0_B : Both legacy & modified refresh mode supported 1_B : Only modified refresh mode supported	
Latency Mode		OP[1]	0_B : Device supports normal latency 1_B : Device supports byte mode latency	5,6
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	00_B: RZQ Self-Test Not Supported 01_B: ZQ pin may connect to V_{SSQ} or float 10_B: ZQ-pin may short to V_{DDQ} 11_B: ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to V_{SSQ} or float, nor short to V_{DDQ})	1,2,3,4

NOTE 1: RZQI MR value, if supported, will be valid after the following sequence:
a. Completion of MPC ZQCAL Start command to either channel.
b. Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied.
RZQI value will be lost after Reset.

NOTE 2: If the ZQ-pin is connected to V_{SSQ} to set default calibration, OP[4:3] shall be set to 01_B. If the ZQ-pin is not connected to V_{SSQ}, either OP[4:3] = 01_B or OP[4:3] = 10_B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 3: In the case of possible assembly error, the LPDDR4X-SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.

NOTE 4: If ZQ Self-Test returns OP[4:3] = 11_B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240Ω ± 1%).

NOTE 5: See byte mode addendum spec for byte mode latency details.

NOTE 6: Byte mode latency for 2Ch. x16 device is only allowed when it is stacked in a same package with byte mode device.

MR1 Register Information (MA[5:0] = 01_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	

Function	Register Type	Operand	Data	Notes
BL (Burst Length)	Write-only	OP[1:0]	00_B: BL=16 Sequential (default) 01_B: BL=32 Sequential 10_B: BL=16 or 32 Sequential (on-the-fly) All Others: Reserved	1,7
WR-PRE (WR Pre-amble Length)		OP[2]	0_B: Reserved 1_B: WR Pre-amble = 2*tCK	5,6
RD-PRE (RD Pre-amble Type)		OP[3]	0_B: RD Pre-amble = Static (default) 1_B: RD Pre-amble = Toggle	3,5,6
nWR (Write-Recovery for Auto-Precharge commands)		OP[6:4]	000_B: nWR = 6 (default) 001_B: nWR = 10 010_B: nWR = 16 011_B: nWR = 20 100_B: nWR = 24 101_B: nWR = 30 110_B: nWR = 34 111_B: nWR = 40	2,5,6
RPST (RD Post-Amble Length)		OP[7]	0_B: RD Post-amble = 0.5*tCK (default) 1_B: RD Post-amble = 1.5*tCK	4,5,6

NOTE 1: Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the “BL” bit in the command operands. See the Command Truth Table.

NOTE 2: The programmed value of nWR is the number of clock cycles the LPDDR4X-SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto-precharge) enabled.

NOTE 3: For Read operations this bit must be set to select between a "toggling" pre-amble and a "Non-toggling" Pre-amble. See 4.5, Read Preamble and Postamble, for a drawing of each type of pre-amble.

NOTE 4: OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.

NOTE 5: There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 6: There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 7: Supporting the two physical registers for Burst Length: MR1 OP[1:0] as optional feature. Applications requiring support of both vendor options shall assure that both FSP-OP[0] and FSP-OP[1] are set to the same code. Refer to vendor datasheets for detail.

Table 12 - Burst Sequence for READ

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
		V	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
		V	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
		V	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	0	1	0	0	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1	1	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	1	0	0	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

NOTE 1: C0-C1 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2: The starting burst address is on 64-bit (4n) boundaries.

Table 13 - Burst Sequence for Write

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

NOTE 1: C0-C1 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2: The starting address is on 256-bit (16n) boundaries for Burst length 16.
NOTE 3: The starting address is on 512-bit (32n) boundaries for Burst length 32.
NOTE 4: C2-C3 shall be set to '0' for all Write operations.

MR2 Register Information (MA[5:0] = 02_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WR Lev	WLS	WL			RL		

Function	Register Type	Operand	Data	Notes
RL (Read latency)	Write-only	OP[2:0]	RL & nRTP for DBI-RD Disabled (MR3 OP[6]=0_B) 000_B: RL=6, nRTP = 8 (Default) 001_B: RL=10, nRTP = 8 010_B: RL=14, nRTP = 8 011_B: RL=20, nRTP = 8 100_B: RL=24, nRTP = 10 101_B: RL=28, nRTP = 12 110_B: RL=32, nRTP = 14 111_B: RL=36, nRTP = 16 RL & nRTP for DBI-RD Enabled (MR3 OP[6]=1_B) 000_B: RL=6, nRTP = 8 001_B: RL=12, nRTP = 8 010_B: RL=16, nRTP = 8 011_B: RL=22, nRTP = 8 100_B: RL=28, nRTP = 10 101_B: RL=32, nRTP = 12 110_B: RL=36, nRTP = 14 111_B: RL=40, nRTP = 16	1,3,4
WL (Write latency)		OP[5:3]	WL Set "A" (MR2 OP[6]=0_B) 000_B: WL=4 (Default) 001_B: WL=6 010_B: WL=8 011_B: WL=10 100_B: WL=12 101_B: WL=14 110_B: WL=16 111_B: WL=18 WL Set "B" (MR2 OP[6]=1_B) 000_B: WL=4 001_B: WL=8 010_B: WL=12 011_B: WL=18 100_B: WL=22 101_B: WL=26 110_B: WL=30 111_B: WL=34	1,3,4
WLS (Write Latency Set)		OP[6]	0_B: WL Set "A" (default) 1_B: WL Set "B"	1,3,4
WR LEV (Write Leveling)		OP[7]	0_B: Disabled (default) 1_B: Enabled	2

Notes:

1. See Table 25 Read and Write Latencies for detail.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the LPDDR4X-SDRAM device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR3 Register Information (MA[5:0] = 03_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL

Function	Register Type	Operand	Data	Notes
PU-Cal (Pull-up Calibration Point)	Write-only	OP[0]	0_B: V_{DDQ}*0.6 1_B: V_{DDQ}*0.5 (default)	1,4
WR PST(WR Post-Amble Length)		OP[1]	0_B: WR Post-amble = 0.5*tCK (default) 1_B: WR Post-amble = 1.5*tCK(Vendor specific function)	2,3,5
Post Package Repair Protection		OP[2]	0_B: PPR protection disabled (default) 1_B: PPR protection enabled	6
PDDS (Pull-Down Drive Strength)		OP[5:3]	000_B: RFU 001_B: RZQ/1 010_B: RZQ/2 011_B: RZQ/3 100_B: RZQ/4 101_B: RZQ/5 110_B: RZQ/6 (default) 111_B: Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	0_B: Disabled (default) 1_B: Enabled	2,3
DBI-WR (DBI-Write Enable)		OP[7]	0_B: Disabled (default) 1_B: Enabled	2,3

Notes:

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.
5. Refer to the supplier data sheet for vender specific function. 1.5*tCK apply > 1.6GHz clock.
6. If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset.
   MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

MR4 Register Information (MA[5:0] = 04_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		

Function	Register Type	Operand	Data	Notes
Refresh Rate	Read	OP[2:0]	000_B: SDRAM Low temperature operating limit exceeded 001_B: 4x refresh 010_B: 2x refresh 011_B: 1x refresh (default) 100_B: 0.5x refresh 101_B: 0.25x refresh, no de-rating 110_B: 0.25x refresh, with de-rating 111_B: SDRAM High temperature operating limit exceeded	1,2,3,4, 7,8,9
SR Abort (Self Refresh Abort)	Write	OP[3]	0_B: Disable (default) 1_B: Enable	9,11
PPRE (Post-package repair entry/exit)	Write	OP[4]	0_B: Exit PPR mode (default) 1_B: Enter PPR mode	5,9
Thermal Offset (Vender Specific Function)	Write	OP[6:5]	00_B: No offset, 0~5 C gradient (default) 01_B: 5°C offset, 5~10°C gradient 10_B: 10°C offset, 10~15°C gradient 11_B: Reserved	10
TUF (Temperature Update Flag)	Read	OP[7]	0_B: No change in OP[2:0] since last MR4 read (default) 1_B: Change in OP[2:0] since last MR4 read	6,7,8

Notes:

1. The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. OP[2:0]=011_B corresponds to a device temperature of 85 °C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1_B, the device temperature is greater than 85 °C.
2. At higher temperatures (>85 °C), AC timing derating may be required. If derating is required the LPDDR4X-SDRAM will set OP[2:0]=110_B.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when OP[2:0]=000_B or 111_B.
5. Post-package repair can be entered or exited by writing to OP[4].
6. When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
7. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence(Te).
8. See the section on “temperature Sensor” for information on the recommended frequency of reading MR4.
9. OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.
10. Refer to the supplier data sheet for vender specific function.
11. Self Refresh abort feature is available for higher density devices starting with 12Gb device.

MR5 Register Information (MA[5:0] = 05_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LPDDR4X Manufacturer ID							

Function	Register Type	Operand	Data	Function
Manufacturer ID	Read-Only	OP[7:0]	0101 0010B: Alliance Memory All Others: Reserved	Manufacturer ID

MR6 Register Information (MA[7:0] = 06_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-1							

Function	Register Type	Operand	Data	Notes
LPDDR4X Revision ID-1	Read-only	OP[7:0]	00000000_B: A-version 00000001_B: B-version	1

NOTE 1 MR6 is vendor specific.

MR7 Register Information (MA[7:0] = 07_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-2							

Function	Register Type	Operand	Data	Notes
LPDDR4X Revision ID-2	Read-only	OP[7:0]	00000000_B: A-version 00000001_B: B-version	1

NOTE 1 MR7 is vendor specific.

MR8 Register Information (MA[5:0] = 08_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
IO Width		Density				Type	

Function	Register Type	Operand	Data	Notes
Type	Read-only	OP[1:0]	00_B: S16 SDRAM (16n pre-fetch) All Others: Reserved	
Density		OP[5:2]	0000_B: 4Gb dual channel die / 2Gb single channel die 0001_B: 6Gb dual channel die / 3Gb single channel die 0010_B: 8Gb dual channel die / 4Gb single channel die 0011_B: 12Gb dual channel die / 6Gb single channel die 0100_B: 16Gb dual channel die / 8Gb single channel die 0101_B: 24Gb dual channel die / 12Gb single channel die 0110_B: 32Gb dual channel die / 16Gb single channel die All Others: Reserved	
IO Width		OP[7:6]	00_B: x16 (per channel) All Others: Reserved	

MR9 Register Information (MA[7:0] = 09_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specific Test Register							

NOTE 1 Only 00_H should be written to this register.

MR10 Register Information (MA[7:0] = $0A_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							**ZQ-Reset**

Function	Register Type	Operand	Data	Notes
ZQ-Reset	Write-only	OP[0]	0_B: Normal Operation (Default) 1_B: ZQ Reset	1,2

NOTE 1 ZQCal Timing Parameters for calibration latency and timing.
NOTE 2 If the ZQ-pin is connected to V_{DDQ} through R_{ZQ}, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to V_{SS}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

MR11 Register Information (MA[5:0] = $0B_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ ODTnt	CA ODT			DQ ODTnt	DQ ODT		

Function	Register Type	Operand	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)	Write-only	OP[2:0]	000_B: Disable (Default) 001_B: RZQ/1 010_B: RZQ/2 011_B: RZQ/3 100_B: RZQ/4 101_B: RZQ/5 110_B: RZQ/6 111_B: RFU	1,2,3
DQ ODTnt (DQ Bus Receiver On-Die Termination for non-target DRAM)		OP[7,3]	00_B: Disable (Default) 01_B: RZQ/3 10_B: RZQ/5 11_B: RZQ/6	1,2,3,4
CA ODT (CA Bus Receiver On-Die-Termination)		OP[6:4]	000_B: Disable (Default) 001_B: RZQ/1 010_B: RZQ/2 011_B: RZQ/3 100_B: RZQ/4 101_B: RZQ/5 110_B: RZQ/6 111_B: RFU	1,2,3

NOTE 1: All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2: There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3: There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4: ODT for non-target DRAM is optional.

MR12 Register Information (MA[5:0] = $0C_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CBT Mode	VR-CA	V_{REF}(CA)					

Function	Register Type	Operand	Data	Notes
V_{REF}(CA) (V_{REF}(CA) Setting)	Read/ Write	OP[5:0]	000000_B: -- Thru -- 110010_B: See table below All Others: Reserved	1,2,3, 5,6
VR-CA (V_{REF}(CA) Range)		OP[6]	0_B: V_{REF}(CA) Range[0] enabled 1_B: V_{REF}(CA) Range[1] enabled (default)	1,2,4, 5,6
CBT Mode	Write	OP[7]	0_B: Mode1 (Default) 1_B: Mode2	7

NOTE 1: This register controls the V_{REF}(CA) levels. Refer to **Table 14** - VREF Settings for Range[0] and Range[1] for actual voltage of V_{REF}(CA).

NOTE 2: A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.

NOTE 3: A write to OP[5:0] sets the internal V_{REF}(CA) level for FSP[0] when MR13 OP[6]=0_B, or sets FSP[1] when MR13 OP[6]=1_B. The time required for V_{REF}(CA) to reach the set level depends on the step size from the current level to the new level. See the section on V_{REF}(CA) training for more information.

NOTE 4: A write to OP[6] switches the LPDDR4X-SDRAM between two internal V_{REF}(CA) ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF}(CA) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.

NOTE 5: There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 6: There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 7: This field can be activated in only Byte Mode: x8. Device.

Table 14 - V_{REF} Settings for Range[0] and Range[1]

Step: 0.6% (1/167)

Function	Operand	Range[0] Values (% of V_{DDQ})		Range[1] Values (% of V_{DDQ})		Notes
V_{REF} Settings for MR12	OP[5:0]	000000_B: 15.0%	011010_B: 30.5 %	000000B: 32.9%	011010_B: 48.5%	1,2,3
		000001_B: 15.6%	011011_B: 31.1%	000001B: 33.5%	011011_B: 49.1%	
		000010_B: 16.2%	011100_B: 31.7%	000010_B: 34.1%	011100_B: 49.7%	
		000011_B: 16.8%	011101_B: 32.3%	000011_B: 34.7%	011101_B: 50.3% (default)	
		000100_B: 17.4%	011110_B: 32.9%	000100_B: 35.3%	011110_B: 50.9%	
		000101_B: 18.0%	011111_B: 33.5%	000101_B: 35.9%	011111_B: 51.5%	
		000110_B: 18.6%	100000_B: 34.1%	000110_B: 36.5%	100000_B: 52.1%	
		000111_B: 19.2%	100001_B: 34.7%	000111_B: 37.1%	100001_B: 52.7%	
		001000_B: 19.8%	100010_B: 35.3%	001000_B: 37.7%	100010_B: 53.3%	
		001001_B: 20.4%	100011_B: 35.9%	001001_B: 38.3%	100011_B: 53.9%	
		001010_B: 21.0%	100100_B: 36.5%	001010_B: 38.9%	100100_B: 54.5%	
		001011_B: 21.6%	100101_B: 37.1%	001011_B: 39.5%	100101_B: 55.1%	
		001100B: 22.2%	100110B: 37.7%	001100B: 40.1%	100110B: 55.7%	
		001101_B: 22.8%	100111_B: 38.3%	001101_B: 40.7%	100111_B: 56.3%	
		001110_B: 23.4%	101000_B: 38.9%	001110_B: 41.3%	101000_B: 56.9%	
		001111_B: 24.0%	101001_B: 39.5%	001111_B: 41.9%	101001_B: 57.5%	
		010000_B: 24.6%	101010_B: 40.1%	010000_B: 42.5%	101010_B: 58.1%	
		010001_B: 25.1%	101011_B: 40.7%	010001_B: 43.1%	101011_B: 58.7%	
		010010_B: 25.7%	101100_B: 41.3%	010010_B: 43.7%	101100_B: 59.3%	
		010011_B: 26.3%	101101_B: 41.9%	010011_B: 44.3%	101101_B: 59.9%	
		010100_B: 26.9%	101110_B: 42.5%	010100_B: 44.9%	101110_B: 60.5%	
		010101_B: 27.5%	101111_B: 43.1%	010101_B: 45.5%	101111_B: 61.1%	
		010110_B: 28.1%	110000_B: 43.7%	010110_B: 46.1%	110000_B: 61.7%	
		010111_B: 28.7%	110001_B: 44.3%	010111_B: 46.7%	110001_B: 62.3%	
		011000_B: 29.3%	110010_B: 44.9%	011000_B: 47.3%	110010_B: 62.9%	
		011001_B: 29.9%	All Others: Reserved	011001_B: 47.9%	All Others: Reserved	

NOTE 1 These values may be used for MR12 OP[5:0] to set the V_{REF}(CA) levels in the LPDDR4X-SDRAM.

NOTE 2 The range may be selected in the MR12 register by setting OP[6] appropriately.

NOTE 3 The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency setting which may use different terminations values.

MR13 Register Information (MA[5:0] = $0D_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT

Function	Register Type	Operand	Data	Notes
CBT (Command Bus Training)	Write-only	OP[0]	0_B: Normal Operation (default) 1_B: Command Bus Training Mode Enabled	1
RPT (Read Preamble Training Mode)		OP[1]	0_B : Disable (default) 1_B : Enable	
VRO (V_{REF} Output)		OP[2]	0_B: Normal operation (default) 1_B: Output the V_{REF}(CA) and V_{REF}(DQ) values on DQ bits	2
VRCG (V_{REF} Current Generator)		OP[3]	0_B: Normal Operation (default) 1_B: V_{REF} Fast Response (high current) mode	3
RRO Refresh rate option		OP[4]	0_B: Disable codes 001 and 010 in MR4 OP[2:0] 1_B: Enable all codes in MR4 OP[2:0]	4, 5
DMD (Data Mask Disable)		OP[5]	0_B: Data Mask Operation Enabled (default) 1_B: Data Mask Operation Disabled	6
FSP-WR (Frequency Set Point Write/Read)		OP[6]	0_B: Frequency-Set-Point[0] (default) 1_B: Frequency-Set-Point [1]	7
FSP-OP (Frequency Set Point Operation Mode)		OP[7]	0_B: Frequency-Set-Point[0] (default) 1_B: Frequency-Set-Point [1]	8

Notes:

1. A write to set OP[0]=1 causes the LPDDR4X-SDRAM to enter the Command Bus Training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See the Command Bus Training section for more information.
2. When set, the LPDDR4X-SDRAM will output the V_{REF}(CA) and V_{REF}(DQ) voltages on DQ pins. Only the “active” frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V_{REF} levels. The DQ pins used for V_{REF} output are vendor specific.
3. When OP[3]=1, the V_{REF} circuit uses a high-current mode to improve V_{REF} settling time.
4. MR13 OP4 RRO bit is valid only when MR0 OP0 = 1. For LPDDR4X devices with MR0 OP0 = 0, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4X devices must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0B) data masking is enabled for the device. When disabled (OP[5]=1B), masked write command is illegal. See 4.16, LPDDR4X Data Mask (DM) and Data Bus Inversion (DBIdc) Function.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as V_{REF}(CA) Setting, V_{REF}(CA) Range, V_{REF}(DQ) Setting, V_{REF}(DQ) Range. For more information, refer to 4.30, Frequency Set Point.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as V_{REF}(CA) Setting, V_{REF}(CA) Range, V_{REF}(DQ) Setting, V_{REF}(DQ) Range. For more information, refer to 4.30 Frequency Set Point section.

MR14 Register Information (MA[5:0] = $0E_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR(DQ)	V_{REF}(DQ)					

Function	Register Type	Operand	Data	Notes
V_{REF}(DQ) (V_{REF}(DQ) Setting)	Read/ Write	OP[5:0]	000000_B: -- Thru -- 110010_B: See table below All Others: Reserved	1,2,3, 5,6
VR(dq) (V_{REF}(DQ) Range)		OP[6]	0_B: V_{REF}(DQ) Range[0] enabled 1_B: V_{REF}(DQ) Range[1] enabled (default)	1,2,4, 5,6

Notes:

1. This register controls the V_{REF}(DQ) levels for Frequency-Set-Point[1:0]. Values from either VR(DQ)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to'0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal V_{REF}(DQ) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for V_{REF}(DQ) to reach the set level depends on the step size from the current level to the new level. See the section on V_{REF}(DQ) training for more information.
4. A write to OP[6] switches the LPDDR4X-SDRAM between two internal V_{REF}(DQ) ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF}(DQ) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 15 - V_{REF} Settings for Range[0] and Range[1]

Step: 0.6% (1/167)

Function	Operand	Range[0] Values (% of V_{DDQ})		Range[1] Values (% of V_{DDQ})		Notes
V_{REF} Settings for MR14	OP[5:0]	000000$_B$: 15.0%	011010$_B$: 30.5 %	000000B: 32.9%	011010$_B$: 48.5%	1,2,3
		000001$_B$: 15.6%	011011$_B$: 31.1%	000001B: 33.5%	011011$_B$: 49.1%	
		000010$_B$: 16.2%	011100$_B$: 31.7%	000010$_B$: 34.1%	011100$_B$: 49.7%	
		000011$_B$: 16.8%	011101$_B$: 32.3%	000011$_B$: 34.7%	011101$_B$: 50.3%	
		000100$_B$: 17.4%	011110$_B$: 32.9%	000100$_B$: 35.3%	011110$_B$: 50.9%	
		000101$_B$: 18.0%	011111$_B$: 33.5%	000101$_B$: 35.9%	011111$_B$: 51.5%	
		000110$_B$: 18.6%	100000$_B$: 34.1%	000110$_B$: 36.5%	100000$_B$: 52.1%	
		000111$_B$: 19.2%	100001$_B$: 34.7%	000111$_B$: 37.1%	100001$_B$: 52.7%	
		001000$_B$: 19.8%	100010$_B$: 35.3%	001000$_B$: 37.7%	100010$_B$: 53.3%	
		001001$_B$: 20.4%	100011$_B$: 35.9%	001001$_B$: 38.3%	100011$_B$: 53.9%	
		001010$_B$: 21.0%	100100$_B$: 36.5%	001010$_B$: 38.9%	100100$_B$: 54.5%	
		001011$_B$: 21.6%	100101$_B$: 37.1%	001011$_B$: 39.5%	100101$_B$: 55.1%	
		001100B: 22.2%	100110B: 37.7%	001100B: 40.1%	100110B: 55.7%	
		001101$_B$: 22.8%	100111$_B$: 38.3%	**001101**$_B$: 40.7% **(default)**	100111$_B$: 56.3%	
		001110$_B$: 23.4%	101000$_B$: 38.9%	001110$_B$: 41.3%	101000$_B$: 56.9%	
		001111$_B$: 24.0%	101001$_B$: 39.5%	001111$_B$: 41.9%	101001$_B$: 57.5%	
		010000$_B$: 24.6%	101010$_B$: 40.1%	010000$_B$: 42.5%	101010$_B$: 58.1%	
		010001$_B$: 25.1%	101011$_B$: 40.7%	010001$_B$: 43.1%	101011$_B$: 58.7%	
		010010$_B$: 25.7%	101100$_B$: 41.3%	010010$_B$: 43.7%	101100$_B$: 59.3%	
		010011$_B$: 26.3%	101101$_B$: 41.9%	010011$_B$: 44.3%	101101$_B$: 59.9%	
		010100$_B$: 26.9%	101110$_B$: 42.5%	010100$_B$: 44.9%	101110$_B$: 60.5%	
		010101$_B$: 27.5%	101111$_B$: 43.1%	010101$_B$: 45.5%	101111$_B$: 61.1%	
		010110$_B$: 28.1%	110000$_B$: 43.7%	010110$_B$: 46.1%	110000$_B$: 61.7%	
		010111$_B$: 28.7%	110001$_B$: 44.3%	010111$_B$: 46.7%	110001$_B$: 62.3%	
		011000$_B$: 29.3%	110010$_B$: 44.9%	011000$_B$: 47.3%	110010$_B$: 62.9%	
		011001$_B$: 29.9%	All Others: Reserved	011001$_B$: 47.9%	All Others: Reserved	

Notes:
1. These values may be used for MR14 OP[5:0] to set the VREF(DQ) levels in the LPDDR4X-SDRAM.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency setting which may use different terminations values.

MR15 Register Information (MA[5:0] = $0F_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Lower-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0_B: Do not invert 1_B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55_H	1,2,3

Notes:
1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DMI[0] is not inverted, and always transmits the “true” data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table 16 - MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR16 Register Information (MA[5:0] = 10_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Bank Mask							

Function	Register Type	Operand	Data	Notes
Bank[7:0] Mask	Write-only	OP[7:0]	0_B: Bank Refresh enabled (default) : Unmasked 1_B: Bank Refresh disabled : Masked	1

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

Notes:
1. When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2. PASR bank-masking is on a per-channel basis. The two channels on the die may have different bank masking in dual channel devices.

MR17 Register Information (MA[5:0] = 11_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Segment Mask							

Function	Register Type	Operand	Data	Notes
PASR Segment Mask	**Write-only**	**OP[7:0]**	**0_B: Segment Refresh enabled (default)** **1_B: Segment Refresh disabled**	

Segment	OP[n]	Segment Mask	2Gb per channel R13:R11	3Gb per channel R14:R12	4Gb per channel R14:R12	6Gb per channel R15:R13	8Gb per channel R15:R13	12Gb per channel R16:R14	16Gb per channel R16:R14
0	0	xxxxxxx1	000_B						
1	1	xxxxxx1x	001_B						
2	2	xxxxx1xx	010_B						
3	3	xxxx1xxx	011_B						
4	4	xxx1xxxx	100_B						
5	5	xx1xxxxx	101_B						
6	6	x1xxxxxx	110_B	Not Allowed	110_B	Not Allowed	110_B	Not Allowed	110_B
7	7	1xxxxxxx	111_B		111_B		111_B		111_B

Notes:

1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual channel devices.
   For 3Gb, 6Gb, and 12Gb per channel densities, OP[7:6] must always be LOW (=00_B).

MR18 Register Information (MA[5:0] = 12_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0 - 255 LSB DRAM DQS Oscillator Count	1,2,3

Notes:

1. MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR19 Register Information (MA[5:0] = 13_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0-255 MSB DRAM DQS Oscillator Count	1,2,3

Notes:
1. MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR20 Register Information (MA[5:0] = 14_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Upper-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Upper-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0_B: Do not invert 1_B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55_H	1,2

Notes:

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
2. DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table 17 - MR20 Invert Register Pin Mapping

PIN	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR22 Register Information (MA[5:0] = 16_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ODTD for x8_2ch(Byte) mode		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write-only	OP[2:0]	000_B: Disable (Default) 001_B: RZQ/1 (illegal if MR3 OP[0] = 0B) 010_B: RZQ/2 011_B: RZQ/3 (illegal if MR3 OP[0] = 0B) 100_B: RZQ/4 101_B: RZQ/5 (illegal if MR3 OP[0] = 0B) 110_B: RZQ/6 (illegal if MR3 OP[0] = 0B) 111_B: RFU	1,2,3
ODTE-CK (CK ODT enabled for non-terminating rank)		OP[3]	ODT bond PAD is ignored 0B: ODT-CK Enable (Default) 1B: ODT-CK Disable	2,3,4
ODTE-CS (CS ODT enable for non-terminating rank)		OP[4]	ODT bond PAD is ignored 0B: ODT-CS Enable (Default) 1B: ODT-CS Disable	2,3,4
ODTD-CA (CA ODT termination disable)		OP[5]	ODT bond PAD is ignored 0B: ODT-CA Enable (Default) 1B: ODT-CA Disable	2,3,4
X8ODTD[7:0] (CA/CLK ODT termination disable, [7:0] Byte select)		OP[6]	Byte mode device x8 2ch only, upper [15:8] Byte selected Device 0B: ODT-CS/CA/CLK follows MR11 OP[6:4] and MR22 OP[5:3] (default) 1B: ODT-CS/CA/CLK Disabled	4
X8ODTD[7:0] (CA/CLK ODT termination disable, [15:8] Byte select)		OP[7]	Byte mode device x8 2ch only, upper [15:8] Byte selected Device 0B: ODT-CS/CA/CLK follows MR11 OP[6:4] and MR22 OP[5:3] (default) 1B: ODT-CS/CA/CLK Disabled	4

Notes:
1. All values are "typical". Depend on SOC setting, value at disable grade may cause weak driver, user can set to other value if necessary..
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. The ODT_CA pin is ignored by LPDDR4X devices. The ODT_CA pin shall be connected to either VDD2 or VSS. CA/ CS/ CK ODT is fully controlled through MR11 and MR22. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed.

MR23 Register Information (MA[5:0] = 17_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS interval timer run time setting							

Function	Register Type	Operand	Data	Notes
DQS interval timer run time	Write-only	OP[7:0]	00000000_B: DQS interval timer stop via MPC Command (Default) 00000001_B: DQS timer stops automatically at 16^{th} clocks after timer start 00000010_B: DQS timer stops automatically at 32^{nd} clocks after timer start 00000011_B: DQS timer stops automatically at 48^{th} clocks after timer start 00000100_B: DQS timer stops automatically at 64^{th} clocks after timer start -------------- Thru -------------- 00111111_B: DQS timer stops automatically at $(63X16)^{th}$ clocks after timer start $01XXXXXX_B$: DQS timer stops automatically at 2048^{th} clocks after timer start $10XXXXXX_B$: DQS timer stops automatically at 4096^{th} clocks after timer start $11XXXXXX_B$: DQS timer stops automatically at 8192^{nd} clocks after timer start	1, 2

Notes:

1. MPC command with OP[6:0]=1001101_B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000_B.
2. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

MR24 Register Information (MA[5:0] = 18_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TRR Mode	TRR Mode BAn			Unlimited	MAC Value		

Function	Register Type	Operand	Data	Notes
MAC Value	Read-only	OP[2:0]	000_B: Unknown when bit OP3=0 (Note 1) Unlimited when bit OP3=1 (Note 2) 001_B: 700K 010_B: 600K 011_B: 500K 100_B: 400K 101_B: 300K 110_B: 200K 111_B: Reserved	
Unlimited MAC		OP[3]	0_B: OP[2:0] define MAC value 1_B: Unlimited MAC value (Note 2, Note 3)	
TRR Mode BAn	Write-only	OP[6:4]	000_B: Bank 0 001_B: Bank 1 010_B: Bank 2 011_B: Bank 3 100_B: Bank 4 101_B: Bank 5 110_B: Bank 6 111_B: Bank 7	
TRR Mode		OP[7]	0_B: Disabled (default) 1_B: Enabled	

Notes:
1. Unknown means that the device is not tested for tMAC and pass/fail value in unknown.
2. There is no restriction to number of activates.
3. MR24 OP [2:0] is set to zero.

MR25 Register Information (MA[5:0] = 19_H)

Mode Register 25 contains one bit of readout per bank indicating that at least one resource is available for Post Package Repair programming.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Bank7	Bank6	Bank5	Bank4	Bank3	Bank2	Bank1	Bank0

Function	Register Type	Operand	Data	Notes
PPR Resource	Read-only	OP[7:0]	0_B: PPR Resource is not available 1_B: PPR Resource is available	

MR30 Register Information (MA[5:0] = $1E_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Valid 0 or 1							

Function	Register Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don't care	1

Notes:

1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR32 Register Information (MA[5:0] = 20_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern “A” (default = $5A_H$)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	X_B: An MPC command with OP[6:0]= 1000011_B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern “$5A_H$”is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)	

MR33 Register Information (MA[5:0] = 21_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECCON	ERRON	CLR ECC	RFU			ECC 2err	ECC Event

Function	Register Type	Operand	Data
ECCON	READ/WRITE	OP[7]	0: ECC function off 1: ECC function on(default)
ERRON		OP[6]	0: ECC ERR info output through ECC pad function off(default) 1: ECC ERR info output through ECC pad function on
CLR ECC	WRITE only	OP[5]	0: ECC Event Record Clear off(default) 1: ECC Event Record Clear on
ECC 2err	READ only	OP[1]	0: No 2bit err 1: 2bit err detect
ECC Event		OP[0]	0: No ECC event 1: ECC Event detect

Bit “ERRON”(op6) is valid only if bit “ECCON”(bit7) is valid first.
Bit “CLR ECC”(op5) is self clean and will clear both “ECC 2err”(op1) and “ECC Event”(op0) if it is write with “1”.
Bit “ECC 2err” and “ECC Event” will keep error status valid once set by ECC err information until “CLR ECC” bit sent.

MR34 Register Information (MA[5:0] = 22_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECC event Number							

Function	Register Type	Operand	Data
ECC event Number	READ only	OP[7:0]	00000000B: No ECC event detect 00000001B: 1 time ECC event detect 00000010B: 2 times ECC event detect 00000011B: 3 times ECC event detect . . . 11111111B: 255 times ECC event detect

The ECC event number will hold max value (0xFF) if it is overflow. And it can also be cleared by MR33 bit “CLR ECC”.

MR39 Register Information (MA[5:0] = 27_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Valid 0 or 1							

Function	Register Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don't care	1

Notes:
1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR40 Register Information (MA[5:0] = 28_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern “B” (default = $3C_H$)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write only	OP[7:0]	X_B: A default pattern “$3C_H$” is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1,2,3

Notes:

1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized “little endian” such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27_H , then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111_B.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

1.10 Refresh Requirement

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the LPDDR4X DRAM requires minimum of one extra Refresh command prior to Self Refresh Entry command.

Table 18 - Refresh Requirement Parameters per die for Dual Channel SDRAM devices

Refresh Requirements		Symbol	2Gb	2Gb	4Gb	4Gb	8Gb	Units	Notes
Density per Channel			**1Gb**	**2Gb**		**4Gb**			
Number of banks per channel			8						
Refresh Window (tREFW) (TCASE ≤ 85°C)		tREFW	32					ms	
Refresh Window (tREFW) (1/2 Rate Refresh)		tREFW	16					ms	
Refresh Window (tREFW) (1/4 Rate Refresh)		tREFW	8					ms	
Required Number of REFRESH Commands in a tREFW window		R	8192					-	
Average Refresh Interval	REFAB	tREFI	3.904					us	
	REFPB	tREFIpb	488					ns	
Refresh Cycle Time (All Banks)		tRFCab	130			180		ns	
Refresh Cycle Time (Per Bank)		tRFCpb	60			90		ns	

NOTE1 Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
NOTE2 Self refresh abort feature is available for higher density devices starting with 12 Gb device and tXSR一abort(min) is defined as tRFCpb + 17.5ns.

2 Operating Conditions and Interface Specification

2.1 Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device.
This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 19 - Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD1} supply voltage relative to Vss	V_{DD1}	-0.4	2.1	V	1
V_{DD2} supply voltage relative to Vss	V_{DD2}	-0.4	1.5	V	1
V_{DDQ} supply voltage relative to VSSQ	V_{DDQ}	-0.4	1.5	V	1
Voltage on any ball except V_{DD1} relative to Vss	VIN, VOUT	-0.4	1.5	V	
Storage Temperature	TSTG	-55	125	°C	2

Notes:

1. See "Power-Ramp" for relationships between power supplies.
2. Storage Temperature is the case surface temperature on the center/top side of the LPDDR4X device. For the measurement conditions, please refer to JESD51-2.

2.2 AC and DC Operating Conditions

Table 20 - Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Notes
Core 1 Power	V_{DD1}	1.70	1.80	1.95	V	1,2
Core 2 Power/Input Buffer Power	V_{DD2}	1.06	1.10	1.17	V	1,2,3
I/O Buffer Power	V_{DDQ}	0.57	0.6	0.65	V	2,3,4,5

Notes:

1. V_{DD1} uses significantly less current than V_{DD2}.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. VdIVW and TdIVW limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45 mV (peak-to-peak) from DC to 20MHz.
4. V_{DDQ}(max) may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 Mhz.
5. Pull up, pull down and ZQ calibration tolerance spec is valid only in normal VDDQ tolerance range (0.57 V - 0.65 V).

Table 21 - Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current	I_L	-4	4	uA	1,2

Notes:

1. For CK_t，CK_c，CKE, CS, CA, ODT_CA and RESET_n. Any input 0V ≤ VIN ≤ V_{DD2} (All other pins not under test = 0V).
2. CA ODT is disabled for CK_t, CK_c, CS, and CA.

Table 22 - Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output Leakage current	I_{OZ}	-5	5	uA	1,2

Notes:

1. For DQ，DQS_t，DQS_c and DM I. Any I/O 0V ≤ VOUT≤ V_{DDQ}.
2. I/Os status are disabled: High Impedance and ODT Off.

Table 23 - Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-40	85	°C
Elevated		85	105	°C

Notes:

1. Operating Temperature is the case surface temperature on the center-top side of the LPDDR4X device. For the measurement conditions, please refer to JESD51-2.
2. Some applications require operation of LPDDR4X in the maximum temperature conditions in the Elevated Temperature Range between 85 °C and 105 °C case temperature. For LPDDR4X devices, de-rating may be neccessary to operate in this range. See MR4.
3. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Elevated Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

2.3 Interface Capacitance

Table 24 - Input/output capacitance

Parameter	Symbol		LPDDR4X 1600-3200	Units	Notes
Input capacitance, CK_t and CK_c	CCK	Min	0.5	pF	1,2
		Max	0.9		
Input capacitance delta, CK_t and CK_c	CDCK	Min	0.0	pF	1,2,3
		Max	0.09		
Input capacitance, All other input-only pins	CI	Min	0.5	pF	1,2,4
		Max	0.9		
Input capacitance delta, All other input-only pins	CDI	Min	-0.1	pF	1,2,5
		Max	0.1		
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	CIO	Min	0.7	pF	1,2,6
		Max	1.3		
Input/output capacitance delta, DQS_t,DQS_c	CDDQS	Min	0.0	pF	1,2,7
		Max	0.1		
Input/output capacitance delta, DQ, DMI	CDIO	Min	-0.1	pF	1,2,8
		Max	0.1		
Input/output capacitance, ZQ pin	CZQ	Min	0.0	pF	1,2
		Max	5.0		

Notes:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, VSS, VSSQ applied and all other pins floating.
3. Absolute value of CCK_ t, CCK_ c.
4. CI applieds to CS_n, CKE, CA0˜CA5.
5. CDI = CI - 0.5 * (CCK_t + CCK_c)
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS_t and CDQS_c.
8. CDIO = CIO - 0.5 * (CDQS_t + CDQS_c) in byte-lane.

3 Speed Bins, AC Timing and IDD

3.1 Speed Bins

Table 25 - Read and Write Latencies

Read Latency		Write Latency		nWR	nRTP	Lower Clock Frequency Limit [MHz] (>)	Upper Clock Frequency Limit [MHz] (≤)	Notes
No DBI	w/DBI	Set A	Set B					
6	6	4	4	6	8	10	266	1,2,3,4,5,6
10	12	6	8	10	8	266	533	
14	16	8	2	16	8	533	800	
20	22	10	18	20	8	800	1066	
24	28	12	22	24	10	1066	1333	
28	32	14	26	30	12	1333	1600	
32	36	16	30	34	14	1600	1866	
36	40	18	34	40	16	1866	2133	

Notes:

1. The LPDDR4X SDRAM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3 OP[6]. When MR3 OP[6]=0, then the "No DBI" column should be used for Read Latency. When MR3 OP[6]=1, then the "w/DBI" column should be used for Read Latency.
3. Write Latency Set "A" and Set "B" is determined by MR2 OP[6]. When MR2 OP[6]=0, then Write Latency Set "A" should be used. When MR2 OP[6]=1， then Write Latency Set "B" should be used.
4. The programmed value of nWR is the number of clock cycles the LPDDR4X SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (Auto Pre- charge). It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the LPDDR4X SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP (Auto Pre- charge). It is determined by RU(tRTP/tCK).
6. nRTP shown in this Table 25 is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.

The ODT Mode is enabled if MR11 OP[3:0] are non-zero. In this case, the value of RTT is determined by the settings of those bits.
The ODT Mode is disabled if MR11 OP[3] = 0.

Table 26 - ODTLon and ODTLoff Latency

ODTLon Latency[1] tWPRE = 2tCK		ODTLoff Latency[2]		Lower Clock Frequency Limit[MHz] (>)	Upper Clock Frequency Limit[Mhz] (≤)
WL Set "A"	WL Set "B"	WL Set "A"	WL Set "B"		
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	6	N/A	22	533	800
4	12	20	28	800	1066
4	14	22	32	1066	1333
6	18	24	36	1333	1600
6	20	26	40	1600	1866
8	24	28	44	1866	2133

Notes:

1. ODTLon is referenced from CAS-2 command.
2. ODTLoff as shown in table assumes BL=16. For BL32, 8 tCK should be added.

The ODT Mode for non-target DRAM ODT control is enabled if MR11 OP[7,3] is set to a non-zero value.
The ODT Mode for non-target DRAM is disabled if MR11 OP[7,3] = 00B.

Table 27 - ODTLon_rd and ODTLoff_rd Latency Values (MR0 [OP1=0] Normal Latency Support)

ODTLon_rd Latency		ODTLoff_rd Latency[1,2]		Lower Clock Frequency Limit[Mhz] (>)	Upper Clock Frequency Limit[Mhz] (≤)
No DBI	w/DBI	No DBI	w/ DBI		
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	N/A	N/A	N/A	533	800
14	16	32	34	800	1066
18	22	36	40	1066	1333
22	26	42	46	1333	1600
26	30	46	50	1600	1866
28	32	50	54	1866	2133

Notes:
1. ODTLoff_rd assumes BL=16, For BL32, 8tCK should be added.
2. ODTLoff_rd assumes a fixed tRPST of 1.5tCK

3.2 AC Timing

Table 28 - Clock AC Timing

Parameter	Symbol	LPDDR4X-1600		LPDDR4X-2400		LPDDR4X-3200		Units	Notes
		Min	Max	Min	Max	Min	Max		
		Clock Timing							
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	ps	

Table 29 - Core AC Timing

Parameter	Symbol	Min/ Max	Data Rate			Unit	Notes
Core Parameters			1600	2400	3200		
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	MIN	tRAS + tRPab (with all bank precharge) tRAS + tRPpb (with per bank precharge)			ns	
Minimum Self Refresh Time (Entry to Exit)	tSR	MIN	max(15ns, 3nCK)			ns	
Self Refresh exit to next valid command delay	tXSR	MIN	max(tRFCab + 7.5ns, 2nCK)			ns	
Exit Power-Down to next valid command delay	tXP	MIN	max(7.5ns, 5nCK)			ns	
CAS-to-CAS delay	tCCD	MIN	8			tCK(avg)	
Internal READ to PRECHARGE command delay	tRTP	MIN	max(7.5ns, 8nCK)			ns	
RAS-to-CAS delay	tRCD	MIN	max(18ns, 4nCK)			ns	
Row precharge time (single bank)	tRPpb	MIN	max(18ns, 4nCK)			ns	
Row precharge time (all banks)	tRPab	MIN	max(21ns, 4nCK)			ns	
Row active time	tRAS	MIN	max(42ns, 3nCK)			ns	
		MAX	Min(9 * tREFI * Refresh Rate, 70.2) us (Refresh Rate is specified by MR4, OP[2:0])			-	
WRITE recovery time	tWR	MIN	max(18ns, 6nCK)			ns	
WRITE-to-READ delay	tWTR	MIN	max(10ns, 8nCK)			ns	
Active bank-A to active bank-B	tRRD	MIN	max(10ns, 4nCK)			ns	
Precharge to Precharge Delay	tPPD	MIN	4			tCK	1, 2
Four-bank ACTIVATE window	tFAW	MIN	40			ns	

Notes:
1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. The value is based on BL16. For BL32 need additional 8 tCK(avg) delay.

Table 30 - Read output timings (Unit UI = tCK(avg)min/2)

Parameter	Symbol	LPDDR4X-1600		LPDDR4X-2400		LPDDR4X-3200		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data Timing									
DQS_t,DQS_c to DQ Skew total, per group, per access (DBI-Disabled)	tDQSQ	-	0.18	-	0.18	-	0.18	UI	
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	UI	
DQ output window time total, per pin (DBI-Disabled)	tQW_total	0.75	-	0.73	-	0.7	-	UI	3
DQ output window time deterministic, per pin (DBI-Disabled)	tQW_dj	tbd	-	tbd	-	tbd	-	UI	2,3
DQS_t,DQS_c to DQ Skew total,per group, per access (DBI-Enabled)	tDQSQ_DBI	-	0.18	-	0.18	-	0.18	UI	
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	UI	
DQ output window time total, per pin (DBI-Enabled)	tQW_total_DBI	0.75	-	0.73	-	0.70	-	UI	3
Data Strobe Timing									
DQS, DQS# differential output low time (DBI-Disabled)	tQSL	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCK(avg)	3,4
DQS, DQS# differential output high time (DBI-Disabled)	tQSH	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCK(avg)	3,5
DQS, DQS# differential output low time (DBI-Enabled)	tQSL_DBI	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCK(avg)	4,6
DQS, DQS# differential output high time (DBI-Enabled)	tQSH_DBI	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK(avg)	5,6

Notes:
1. The deterministic component of the total timing. Measurement method tbd.
2. This parameter will be characterized and guaranteed by design.
3. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
4. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
5. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
6. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

Table 31 - Read AC Timing

Parameter	Symbol	Min/Max	Data Rate			Unit	Notes
Read Timing			1600	2400	3200		
READ preamble	tRPRE	Min	1.8			tCK(avg)	
0.5 tCK READ postamble	tRPST	Min	0.4			tCK(avg)	
1.5 tCK READ postamble	tRPST	Min	1.4			tCK(avg)	
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	Min	(RL x tCK) + tDQSCK(Min) - 200ps			ps	
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	Max	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2xtCK)-100ps			ps	
DQS_c low-impedance time from CK_t, CK_c	tLZ(DQS)	Min	(RL x tCK) + tDQSCK(Min) -(tRPRE(Max) x tCK) - 200ps			ps	
DQS_c high impedance time from CK_t, CK_c	tHZ(DQS)	Max	(RL x tCK) + tDQSCK(Max) +(BL/2 x tCK) + (RPST(Max) x tCK) • 100ps			ps	
DQS-DQ skew	tDQSQ	Max	0.18			UI	

Table 32 - tDQSCK Timing

Parameter	Symbol	Min	Max	Unit	Notes
DQS Output Access Time from CK_t/CK_c	tDQSCK	1.5	3.5	ns	1
DQS Output Access Time from CK_t/CK_c - Temperature Variation	tDQSCK_temp	-	4	ps/°C	2
DQS Output Access Time from CK_t/CK_c - Voltage Variation	tDQSCK_volt	-	7	ps/mV	3
CK to DQS Rank to Rank variation	tDQSCK_rank2rank	-	1.0	ns	4,5

Notes:

1. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies> 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
2. tDQSCK_temp max delay variation as a function of Temperature.
3. tDQSCK_volt max delay variation as a function of DC voltage variation for V_{DDQ} and V_{DD2}. tDQSCK_volt should be used to calculate timing variation due to V_{DDQ} and V_{DD2} noise < 20 MHz. Host controller do not need to account for any variation due to V_{DDQ} and V_{DD2} noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1- tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. For tester measurement $V_{DDQ} = V_{DD2}$ is assumed.
4. The same voltage and temperature are applied to tDQS2CK_rank2rank.
5. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

Table 33 - DRAM DQs In Receive Mode (UI = tCK(avg)min/2)

Symbol	Parameter	1600		2400		3200		Unit	Notes
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	mV	1,2,3,4
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	UI	1.2,4
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	UI	1,2,4, 12
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	mV	5,13
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		UI	6
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	ps	7
tDQ2DQ	DQ to DQ offset	-	30	-	30	-	30	ps	8
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	ps/°C	9
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	ps/50 mV	10
SRIN_dIVW	Input Slew Rate over VdIVWJotal	1	7	1	7	1	7	V/ns	11
tDQS2DQ_rank2rank	DQ to DQS offset rank to rank variation	-	200	-	200	-	200	ps	14,15

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20 MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2. The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
6. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
7. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
8. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9. TDQS2DQ max delay variation as a function of temperature.
10. TDQS2DQ max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD2}. It includes the V_{DDQ} and V_{DD2} AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement V_{DDQ} = V_{DD2} is assumed.
11. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
12. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13. VIHL_AC does not have to be met when no transitions are occurring.
14. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
15. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

Table 34 - Write AC Timing

Parameter	Symbol	Min/Max	Data Rate			Unit	Notes
Write Timing			1600	2400	3200		
Write command to 1st DQS latching	tDQSS	Min	0.75			tCK(avg)	
		Max	1.25				
DQS input high-level	tDQSH	Min	0.4			tCK(avg)	
DQS input low-level width	tDQSL	Min	0.4			tCK(avg)	
DQS falling edge to CK setup time	tDSS	Min	0.2			tCK(avg)	
DQS falling edge hold time from CK	tDSH	Min	0.2			tCK(avg)	
Write preamble	tWPRE	Min	1.8			tCK(avg)	
0.5 tCK Write postamble	tWPST	Min	0.4			tCK(avg)	1
1.5 tCK Write postamble	tWPST	Min	1.4			tCK(avg)	1

Notes:
1. The length of Write Postamble depends on MR3 OP1 setting.

Table 35 - Power-Down AC Timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Notes
Power Down Timing					
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	Min	Max(7.5ns, 4nCK)	-	
Delay from valid command to CKE input LOW	tCMDCKE	Min	Max(1.75ns, 3nCK)	ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	Min	1.75	ns	
Valid CS Requirement after CKE Input low	tCKELCS	Min	Max(5ns, 5nCK)	ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns, 3nCK)	ns	1
Exit power- down to next valid command delay	tXP	Min	Max(7.5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	Min	1.75	ns	
Valid CS Requirement after CKE Input High	tCKEHCS	Min	Max(7.5ns, 5nCK)	ns	
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	Min	Max(14ns, 10nCK)	ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	Min	Max(1.75ns, 3nCK)	ns	1

Notes:

1. Delay time has to satisfy both analog time(ns) and clock count(nCK).

Table 36 - Command Address Input Parameters (UI = tCK(avg)min/2)

Symbol	Parameter	DQ-1600		DQ-3200		Unit	Notes
		min	max	min	max		
VcIVW	Rx Mask voltage - p-p	-	175	-	155	mV	1,2,3
TcIVW	Rx timing window	-	0.3	-	0.3	UI	1,2,3
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	190	-	mV	4,7
TcIPW	CA input pulse width	0.55		0.6		UI	5
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	V/ns	6

Notes:

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Vcent_CA must be within the adjustment range of the CA internal Vref.
4. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.

Table 37 - Mode Register Read/Write AC timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Notes
Mode Register Read/Write Timing					
Additional time after tXP has expired until MRR command may be issued	tMRRI	Min	tRCD + 3nCK	-	
MODE REGISTER READ command period	tMRR	Min	8	nCK	
MODE REGISTER WRITE command period	tMRW	Min	MAX(10ns, 10nCK)	-	
|Mode register set command delay	tMRD	Min	max(14ns, 10nCK)	-	

Table 38 - Asynchronous ODT Turn On and Turn Off Timing

Parameter	800-2133 tCK	Unit	Notes
tODTon, min	1.5	ns	
tODTon, max	3.5	ns	
tODToff, min	1.5	ns	
tODToff, max	3.5	ns	

Table 39 - Self-Refresh Timing Parameters

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
Self Refresh Timing					
Delay from SRE command to CKE Input low	tESCKE	Min	Max(1.75ns, 3tCK)	ns	1
Minimum Self Refresh Time	tSR	Min	Max(15ns, 3tCK)	ns	1
Exit Self Refresh to Valid commands	tXSR	Min	Max(tRFCab + 7.5ns, 2tCK)	ns	1,2

Notes:

1. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired.
2. MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.

Table 40 - Command Bus Training AC Timing

Parameter	Symbol	Min/ Max	Data Rate			Unit	Notes
			1600	2400	3200		
Command Bus Training Timing							
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)			-	
Data Setup for VREF Training Mode	tDStrain	Min	2			ns	
Data Hold for VREF Training Mode	tDHtrain	Min	2			ns	
Asynchronous Data Read	tADR	Max	20			ns	
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	RU(tADR/tCK)			tCK	2
Valid Strobe Requirement before CKE Low	tDQSCKE	Min	10			ns	1
First CA Bus Training Command Following CKE Low	tCAENT	Min	250			ns	
VREF Step Time -multiple steps	tVREFCA_LONG	Max	250			ns	
Vref Step Time -one step	tVREFCA_SHORT	Max	80			ns	
Valid Clock Requirement before CS High	tCKPRECS	Min	2tck + tXP (tXP = max(7.5ns, 5nCK))			-	
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))			-	
Minimum delay from CS to DQS toggle in command bus training	tCS_VREF	Min	2			tCK	
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS		10			ns	
Valid Clock Requirement before CKE input High	tCKCKEH	Min	Max(1.75ns, 3nCK)			-	
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5			ns	
ODT turn-on Latency from CKE	tCKELODTon	Min	20			ns	
ODT tum-off Latency from CKE	tCKELODToff	Min	20			ns	
Exit Command Bus Training Mode to next valid command delay	tXCBT_Short	Min	Max(5nCK, 200ns)			-	3
	tXCBT_Middle	Min	Max(5nCK, 200ns)			-	
	tXCBT_Long	Min	Max(5nCK, 250ns)			-	

Notes:

1. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
2. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
3. Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Table 41 - Temperature Derating AC Timing

Parameter	Symbol	Min/ Max	Data Rate			Unit	Note
			1600	2400	3200		
Temperature Derating[1]							
DQS output access time from CK_t/CK_c (derated)	tDQSCK	MAX	3600			ps	
RAS-to-CAS delay (derated)	tRCD	MIN	tRCD+ 1.875			ns	
ACTIVATE-to- ACTIVATE command period (derated)	tRC	MIN	tRC + 3.75			ns	
Row active time (derated)	tRAS	MIN	tRAS + 1.875			ns	
Row precharge time (derated)	tRP	MIN	tRP+ 1.875			ns	
Active bank A to active bank B (derated)	tRRD	MIN	tRRD + 1.875			ns	

Notes:
1. Timing derating applies for operation at 85 °C to 105 °C.

3.3 IDD Specification

V_{DD2} = 1.06 ~ 1.17V, V_{DDQ} = 0.57 ~ 0.65V, V_{DD1} = 1.70 ~ 1.95V

Table 42 - IDD Specification (3200Mbps)

Parameter	Supply	2Gb x16	4Gb x16	8Gb x32	Unit
IDD01	V_{DD1}	9	18	36	mA
IDD02	V_{DD2}	39.5	79	158	mA
IDD0Q	V_{DDQ}	0.25	0.5	1	mA
IDD2P1	V_{DD1}	0.6	1.2	2.4	mA
IDD2P2	V_{DD2}	1.25	2.5	5	mA
IDD2PQ	V_{DDQ}	0.15	0.3	0.6	mA
IDD2PS1	V_{DD1}	0.6	1.2	2.4	mA
IDD2PS2	V_{DD2}	1.25	2.5	5	mA
IDD2PSQ	V_{DDQ}	0.15	0.3	0.6	mA
IDD2N1	V_{DD1}	0.75	1.5	3	mA
IDD2N2	V_{DD2}	17.5	35	70	mA
IDD2NQ	V_{DDQ}	0.15	0.3	0.6	mA
IDD2NS1	V_{DD1}	0.75	1.5	3	mA
IDD2NS2	V_{DD2}	12.5	25	50	mA
IDD2NSQ	V_{DDQ}	0.15	0.3	0.6	mA
IDD3P1	V_{DD1}	0.75	1.5	3	mA
IDD3P2	V_{DD2}	7.5	15	30	mA
IDD3PQ	V_{DDQ}	0.15	0.3	0.6	mA
IDD3PS1	V_{DD1}	0.75	1.5	3	mA
IDD3PS2	V_{DD2}	7.5	15	30	mA
IDD3PSQ	V_{DDQ}	0.15	0.3	0.6	mA
IDD3N1	V_{DD1}	1	2	4	mA
IDD3N2	V_{DD2}	22.5	45	90	mA
IDD3NQ	V_{DDQ}	0.25	0.5	1	mA
IDD3NS1	V_{DD1}	1	2	4	mA
IDD3NS2	V_{DD2}	22.5	45	90	mA
IDD3NSQ	V_{DDQ}	0.25	0.5	1	mA
IDD4R1	V_{DD1}	1.5	3	4	mA
IDD4R2	V_{DD2}	250	500	600	mA
IDD4RQ	V_{DDQ}	130	260	280	mA
IDD4W1	V_{DD1}	1.5	3	4	mA
IDD4W2	V_{DD2}	200	400	480	mA
IDD4WQ	V_{DDQ}	0.25	0.5	1	mA
IDD51	V_{DD1}	25	50	100	mA
IDD52	V_{DD2}	60	120	240	mA
IDD5Q	V_{DDQ}	0.25	0.5	1	mA
IDD5AB1	V_{DD1}	5	10	20	mA

Parameter	Supply	2Gb x16	4Gb x16	8Gb x32	Unit
IDD5AB2	V_{DD2}	26.5	53	106	mA
IDD5ABQ	V_{DDQ}	0.25	0.5	1	mA
IDD5PB1	V_{DD1}	5	10	20	mA
IDD5PB2	V_{DD2}	26.5	53	106	mA
IDD5PBQ	V_{DDQ}	0.25	0.5	1	mA

V_{DD2} = 1.06 ~ 1.17V, V_{DDQ} = 0.57 ~ 0.65V, V_{DD1} = 1.70 ~ 1.95V

Table 43 - IDD6 specification (3200Mbps)

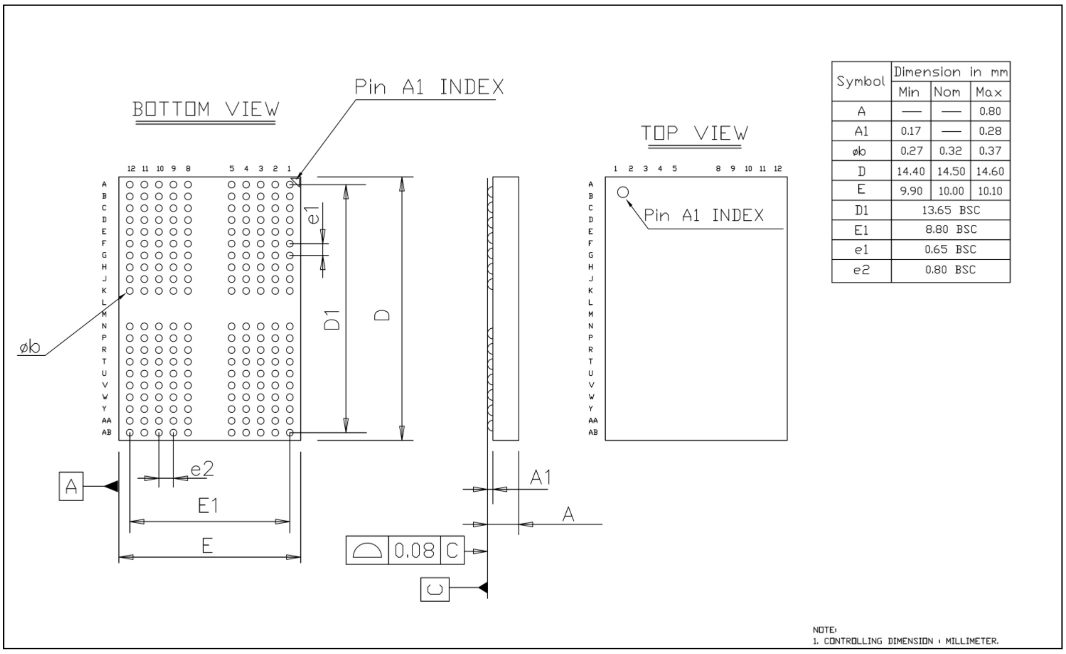
Temperature	Parameter	Supply	2Gb x16	4Gb x16	8Gb x32	Unit
45°C	IDD61	V_{DD1}	2	4	8	mA
	IDD62	V_{DD2}	3.5	7	14	mA
	IDD6Q	V_{DDQ}	0.25	0.5	1	mA
85°C	IDD61	V_{DD1}	4	7.5	15	mA
	IDD62	V_{DD2}	7	13	26	mA
	IDD6Q	V_{DDQ}	0.25	0.5	1	mA

4 Package Outlines

Figure 6 reflects the current status of the outline dimensions of the LPDDR4X SDRAM packages for components with x16/x32 configuration.

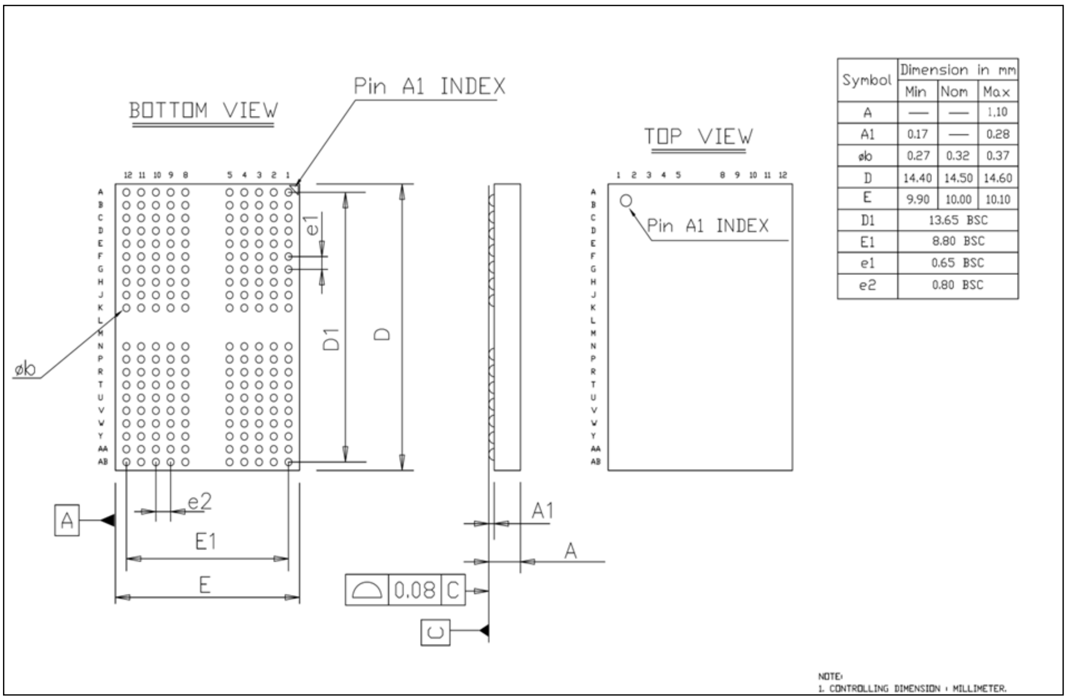
Figure 6 - Package Outline

AS4C128M16MD4V / AS4C256M16MD4V



Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	0.80
A1	0.17	—	0.28
øb	0.27	0.32	0.37
D	14.40	14.50	14.60
E	9.90	10.00	10.10
D1	13.65 BSC		
E1	8.80 BSC		
e1	0.65 BSC		
e2	0.80 BSC		

AS4C256M32MD4V



Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.10
A1	0.17	—	0.28
øb	0.27	0.32	0.37
D	14.40	14.50	14.60
E	9.90	10.00	10.10
D1	13.65 BSC		
E1	8.80 BSC		
e1	0.65 BSC		
e2	0.80 BSC		

PART NUMBERING SYSTEM

AS4C	256M32MD4V	-062	B	A	N	XX
DRAM	128M16=128Mx16 256M16=256Mx16 256M32=256Mx32 MD4V=LPDDR4X	062=1600MHz	B=FBGA	A=Automotive -40°C~ 105°C Grade 2	Indicates Pb and Halogen Free	Packing Type None:Tray TR:Reel

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