

# MOSFET - Power, Single N-Channel

**60 V, 2.9 mΩ, 139.3 A**  
**NVMJS3D0N06C**

## Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DS}$	60	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$ 139.3	A
		$T_C = 100^\circ\text{C}$	98.5	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$ 112.5	W
		$T_C = 100^\circ\text{C}$	56.2	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ 26.9	A
		$T_A = 100^\circ\text{C}$	19	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 4.2	W
		$T_A = 100^\circ\text{C}$	2.1	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$ 900	A	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	93.7	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 9.1 \text{ A}$ )	$E_{AS}$	430	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

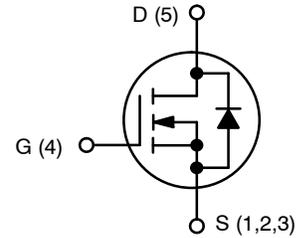
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 1)	$R_{\theta JC}$	1.33	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Notes 1, 2)	$R_{\theta JA}$	35.9	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
60 V	2.9 mΩ @ 10 V	139.3 A

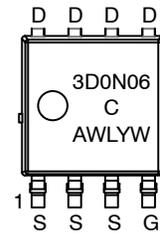


N-CHANNEL MOSFET



LFPAK8  
CASE 760AA

## MARKING DIAGRAM



3D0N06C = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
W = Work Week

## ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMJS3D0N06C

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			25		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V	T <sub>J</sub> = 25°C		10	μA
			T <sub>J</sub> = 125°C		250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

### ON CHARACTERISTICS

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 135 μA	2.0		4.0	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-8.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 27 A		2.2	2.9	mΩ

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V		2675		pF
Output Capacitance	C <sub>OSS</sub>			1920		
Reverse Transfer Capacitance	C <sub>RSS</sub>			21		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V; I <sub>D</sub> = 27 A		34		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			7		
Gate-to-Source Charge	Q <sub>GS</sub>			11		
Gate-to-Drain Charge	Q <sub>GD</sub>			5.5		
Plateau Voltage	V <sub>GP</sub>			4.6		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 27 A, R <sub>G</sub> = 2.5 Ω		16		ns
Rise Time	t <sub>r</sub>			6		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			27		
Fall Time	t <sub>f</sub>			7		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 27 A	T <sub>J</sub> = 25°C		0.8	1.2	V
			T <sub>J</sub> = 125°C		0.67		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 27 A		51		ns	
Charge Time	t <sub>a</sub>			25			
Discharge Time	t <sub>b</sub>			26			
Reverse Recovery Charge	Q <sub>RR</sub>			36			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

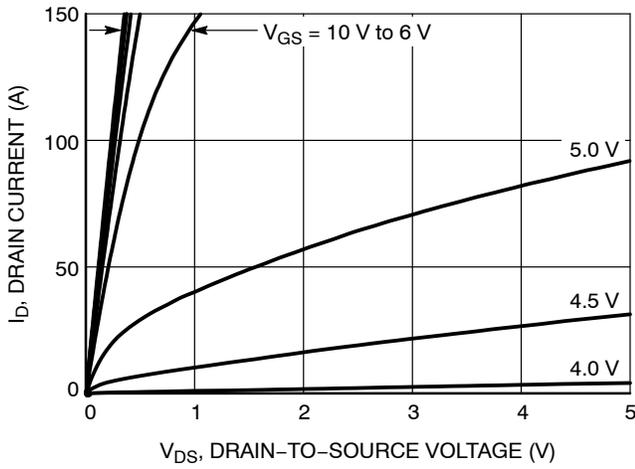


Figure 1. On-Region Characteristics

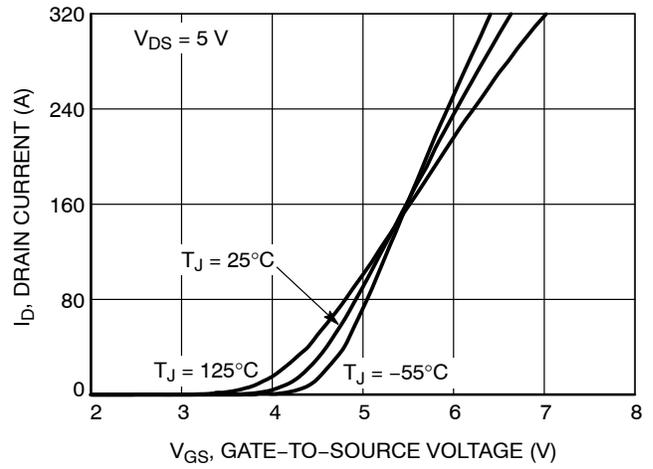


Figure 2. Transfer Characteristics

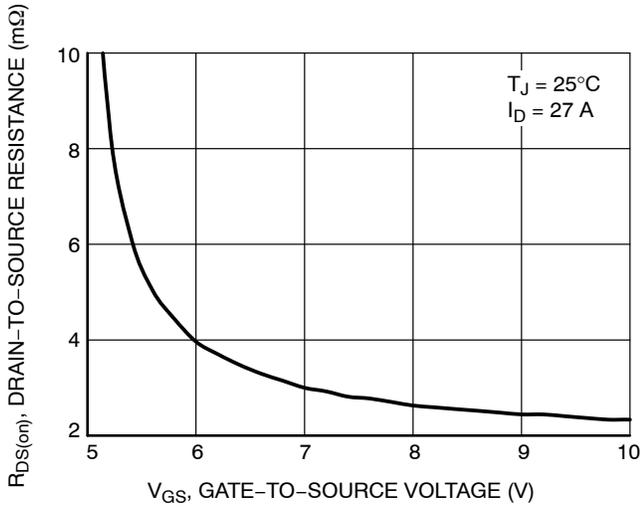


Figure 3. On-Resistance vs. Gate-to-Source Voltage

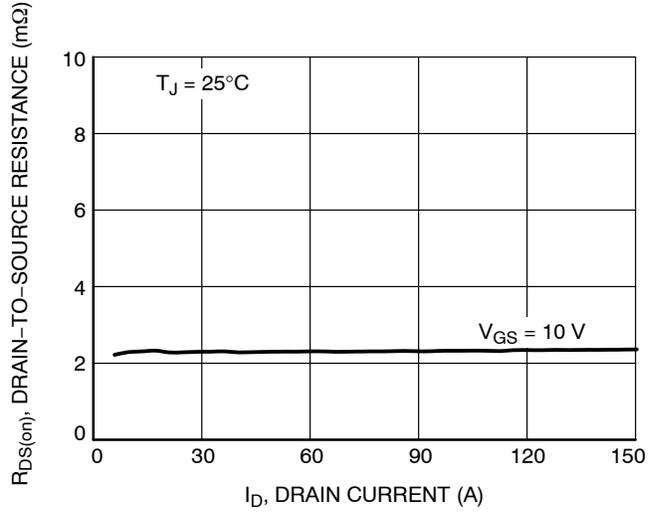


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

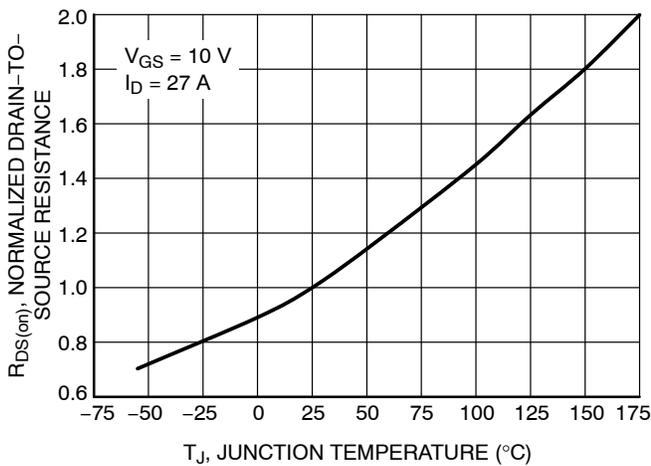


Figure 5. On-Resistance Variation with Temperature

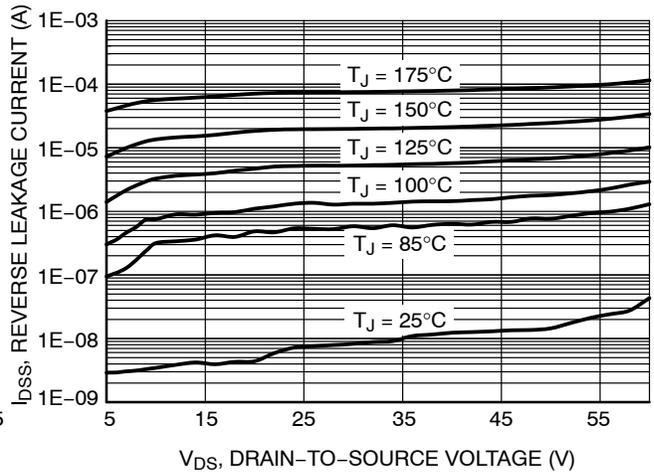


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

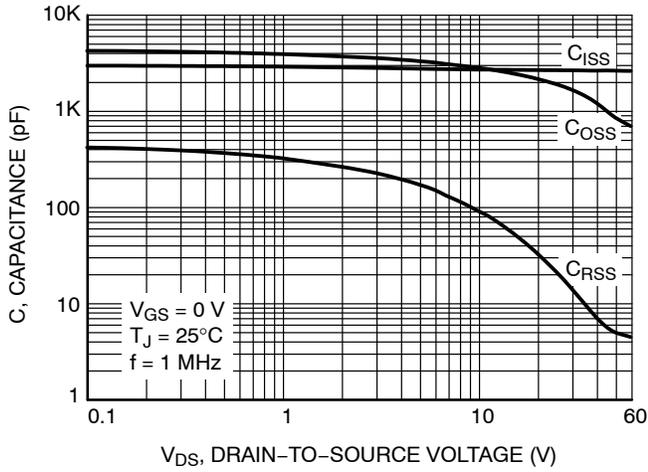


Figure 7. Capacitance Variation

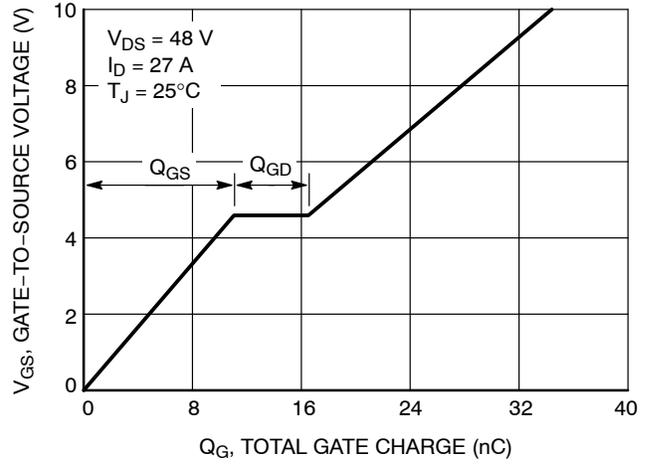


Figure 8. Gate-to-Source vs. Total Charge

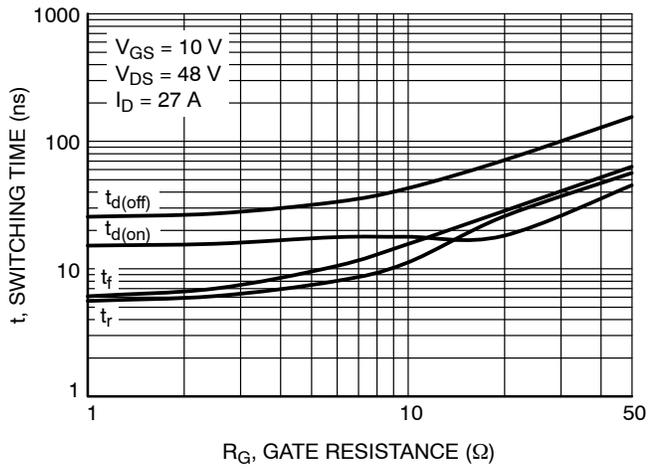


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

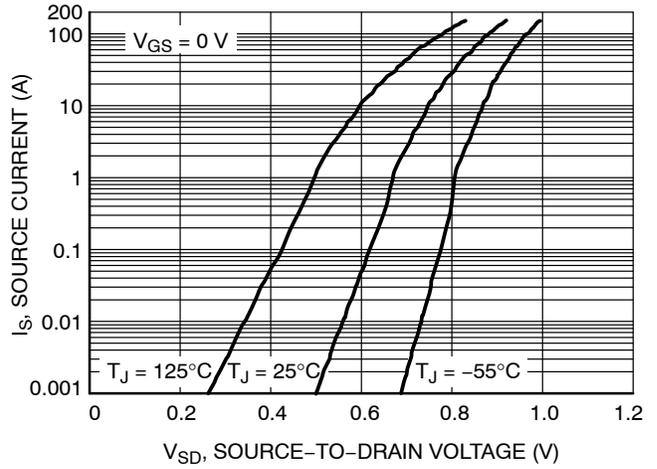


Figure 10. Diode Forward Voltage vs. Current

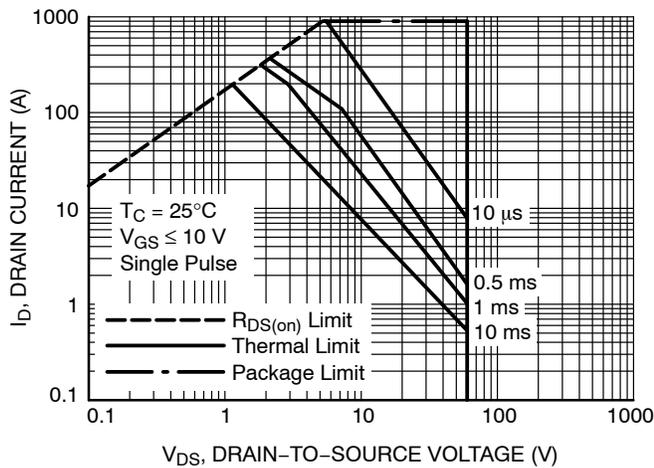


Figure 11. Maximum Rated Forward Biased Safe Operating Area

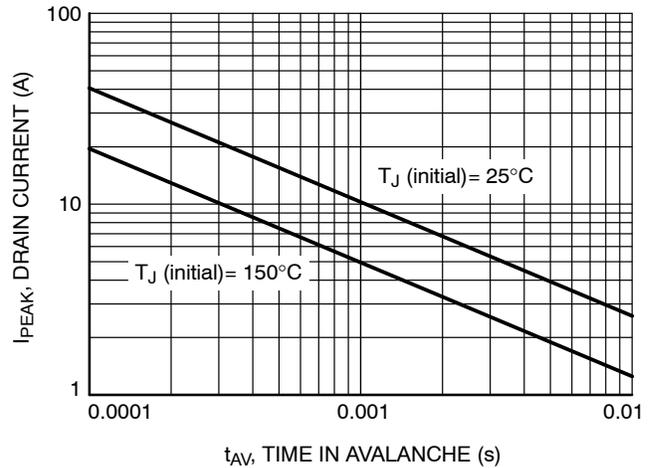


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVMJS3D0N06C

## TYPICAL CHARACTERISTICS

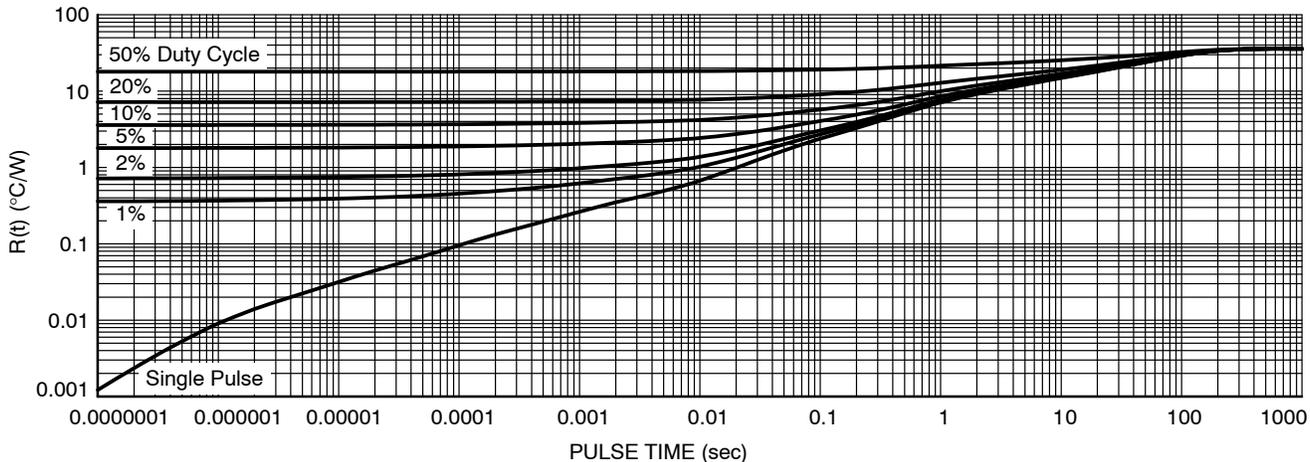


Figure 13. Transient Thermal Impedance

### DEVICE ORDERING INFORMATION

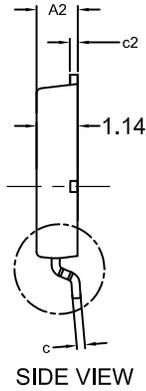
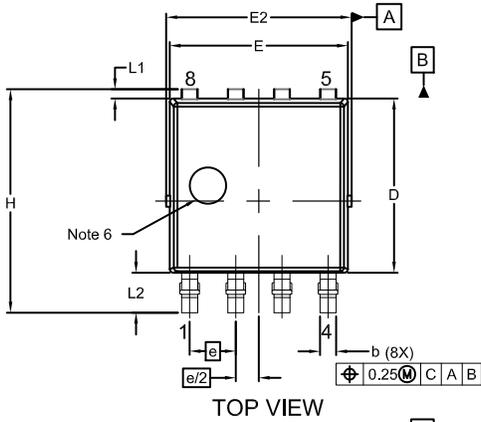
Device	Marking	Package	Shipping <sup>†</sup>
NVMJS3D0N06CTWG	3D0N06C	LFPAK8 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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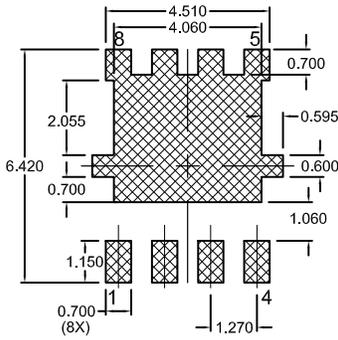
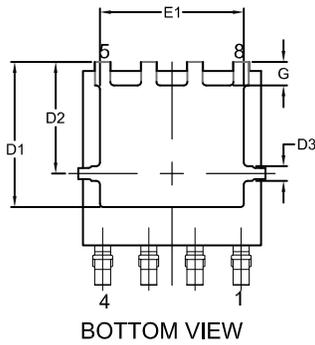
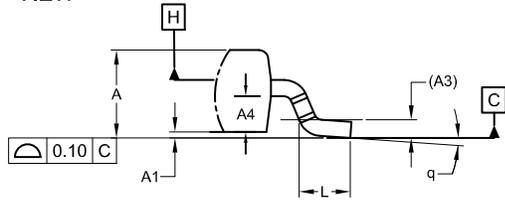
## PACKAGE DIMENSIONS

### LFPAK8 5x6 CASE 760AA ISSUE C



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 REF		
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
E	4.80	4.90	5.00
E1	3.90	4.00	4.10
E2	5.00	5.15	5.30
e	1.27 BSC		
G	0.55	0.65	0.75
H	6.00	6.15	6.30
L	0.45	0.65	0.85
L1	0.15	0.25	0.35
L2	0.90	1.10	1.30
q	0°	4°	8°

#### RECOMMENDED LAND PAD

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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