## General Description

The evaluation circuit EVAL-LT8390A-AZ is a synchronous 4-switch buck-boost controller featuring the LT8390A and 4 EPC GaN FETs. This circuit outputs 24 V and maintains tight regulation with up to 5A load current and over an input voltage from 8 V to 60 V . 2 MHz switching frequency provides a small footprint using a single $6 \mathrm{~mm} x$ $6 \mathrm{~mm} \times 6 \mathrm{~mm}$ inductor while maintaining high efficiency.

The LT8390A features a 5 V gate driver that is used to safely drive GaNFETs. Additionally, the EVAL-LT8390AAZ board features external clamping circuitry around the bootstrap capacitors to guarantee that the gate drive of the top FETs is driven under the absolute maximum gate-tosource voltage of the GaNFET. Additionally, Schottky diodes are placed anti-parallel to the synchronous GaNFETs to help with reverse conduction during the LT8390A's 25ns dead time.

The LT8390A has a wide input voltage range from 4 V to 60 V . It can regulate an output as a boost, a buck, or a

4-switch boost-buck controller. It has an adjustable switching frequency between 600 kHz and 2 MHz . It has an option for external frequency synchronization or spread spectrum frequency modulation. Its high switching frequency is unique to buck-boost controller ICs. Because of this, it can be used for high power when the input may be above, below, or equal to the output.

The LT8390A data sheet gives a complete description of the part, operation, and applications information. The data sheet must be read in conjunction with this user guide. The LT8390AJUFD is assembled in a 28 -lead $4 \mathrm{~mm} \times 5 \mathrm{~mm}$ plastic QFN package with a thermally enhanced ground pad. LT8390A is also available in a 28 -Lead plastic TSSOP (FE) package. Proper board layout is essential for maximum thermal performance. Refer to the data sheet PC Board Layout Checklist section for more details.

Design files for this circuit board are available at Product Evaluation Boards and Kits | Design Center | Analog Devices.

## Performance Summary ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ )

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Voltage Range | $\begin{aligned} & \hline \text { IOUT }=0 \mathrm{~A}-5 \mathrm{~A} \\ & \text { Heatsink }+400 \mathrm{LFM} \text { Airflow } \\ & \text { Maximum Board Temperature }<105^{\circ} \mathrm{C} \\ & \text { after } 10 \text { minutes } \\ & \hline \end{aligned}$ | 8 |  | 60 | V |
|  | IOUT $=0 \mathrm{~A}-5 \mathrm{~A}$, Heatsink Maximum Board Temperature $<105^{\circ} \mathrm{C}$ after 10 minutes | 12 |  | 43 |  |
|  | lout $=0 \mathrm{~A}-5 \mathrm{~A}$, No Heatsink or Airflow Maximum Board Temperature $<115^{\circ} \mathrm{C}$ after 10 minutes | 14.5 |  | 32 | V |
| Output Voltage | $\mathrm{V}_{\mathrm{IN}}=8 \mathrm{~V}-60 \mathrm{~V}$ |  | 24 |  | V |
| EN/UVLO Threshold (Rising Turn-On) |  |  | 8.9 |  | V |
| EN/UVLO Falling Threshold |  |  | 7.9 |  | V |
| Switching Frequency | JP2 = Disable SS (SSFM Off) |  | 2 |  | MHz |
|  | JP2 = Enable SS (SSFM On) | 2 |  | 2.5 | MHz |
| Typical Efficiency | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=5 \mathrm{~A}$ |  | 94 |  | \% |
|  | $\mathrm{V}_{\text {IN }}=24 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=5 \mathrm{~A}$ |  | 93 |  | \% |
|  | $\mathrm{V}_{\text {IN }}=48 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=5 \mathrm{~A}$ |  | 92 |  | \% |

## Quick Start Procedure

Evaluation circuit EVAL-LT8390A-AZ is easy to set up to evaluate the performance of the LT8390A. For a proper measurement equipment setup, see Figure 1 and follow the procedure below.

1. Set the input power supply to a voltage between 9 V and 60 V . Disable the power supply. An input of 8 V can be achieved after start up.

NOTE: Make sure that the input voltage $\mathrm{V}_{\mathrm{IN}}$ does not exceed 60V.
NOTE: Without a heatsink or airflow, we recommend operating with an input of 14.5 V to 32 V if operating at 5 A load. See Figure 4 for more details.
2. Connect the positive terminal of the power supply to $\mathrm{V}_{\mathrm{IN}}$ and the negative terminal to GND.
3. Connect the load $(<5 A)$ between $V_{\text {OUT }}$ and GND.
4. Verify that the output voltage is 24 V on the DMM connected to $\mathrm{V}_{\text {OUT }}$. If there is no output, temporarily disconnect the load to make sure that the load is not set too high.
5. Once the proper output voltage is established, adjust the load and observe the output voltage regulation, ripple voltage, efficiency, and other parameters.

NOTE: When measuring the input or output voltage ripple, care must be taken to minimize the length of the oscilloscope probe ground lead. Measure the input or output voltage ripple by connecting the probe tip directly across the $\mathrm{V}_{\text {IN }}$ or $\mathrm{V}_{\text {OUT }}$ and GND terminals, preferably across the input or output capacitors.
The EVAL-LT8390A-AZ is a fully assembled and tested board that demonstrates the performance of the LT8390A. The evaluation circuit is designed to deliver 24 V output at a load current of up to 5 A from an 8 V to 60 V input supply. The board is programmed at a 2 MHz switching frequency for optimum efficiency and component size.

## Adjusting the Output Voltage

The LT8390A supports an adjustable output voltage range, from 1 V to 60 V . To change the output voltage from the programmed 24 V , change R5 and R6. Refer to the Programming the Output Voltage section on the data sheet for calculating the $\mathrm{V}_{\mathrm{FB}}$ resistor divider values for the desired output voltage. All the corresponding power components must also be changed to meet the desired output voltage.

## Setting the Switching Frequency

Selecting the switching frequency is a trade-off between efficiency and component size. A switching frequency of 2 MHz is chosen for this board for optimal space saving. R23 programs the desired switching frequency. The switching frequency is set using the RT pin. Refer to the Switching Frequency Selection section in the datasheet for more details.

## EN/UVLO

The EN/UVLO turret of the evaluation circuit serves as an external on/off control for the controller. The EVAL-LT8390A$A Z$ includes a resistive voltage divider (R7 and R8) connected between the $V_{I N}$ and GND pins to turn on the device at the required input voltage. The EVAL-LT8390A-AZ is designed to turn on LT8390A at around 8.9V. However, this threshold can be easily adjusted by changing R7 and R8. Short EN/UVLO turret to GND to turn off the device.

## Spread Spectrum and External Frequency Synchronization (SYNC/SSFM, JP1)

The LT8390A features spread-spectrum mode operation to improve EMI. This mode varies the switching frequency within the typical boundaries of the frequency set by the FREQ pin and $+25 \%$. Spread-spectrum operation is enabled by tying the SYNC pin to INTV $C$. The EVAL-LT8390A-AZ includes a jumper (JP1) to conveniently enable or disable the spreadspectrum operation.
The LT8390A also features a phase-locked loop to synchronize the internal oscillator to an external clock source. The EVAL-LT8390A-AZ provides a SYNC turret to connect an external clock source to synchronize with the device switching. Keep the jumper (JP1) in the SYNC position when the external clock signal is applied. Refer to the datasheet for more details about external clock synchronization. See Table 1 to configure JP1.

## Open-Drain $\overline{\text { PGOOD }}$ Output ( $\overline{\text { PGOOD }})$

The EVAL-LT8390A-AZ provides a $\overline{\text { PGOOD }}$ turret to monitor the status of the $\overline{\text { PGOOD output. } \overline{\text { PGOOD }} \text { is low when } V_{F B}}$ voltage is within $\pm 10 \%$ of the 1.00 V reference. PGOOD is high when $\mathrm{V}_{\mathrm{FB}}$ voltage is not within $1.00 \mathrm{~V} \pm 10 \%$. The voltage on the PGOOD pin should not exceed 6 V .

## CTRL and ISMON

The EVAL-LT8390A-AZ provides a resistive divider (R9 and R10) to set the CTRL pin. The default resistive divider to CTRL pin voltage is set to control the maximum voltage threshold of ISP-ISN to 50 mV . With the $8 \mathrm{~m} \Omega$ resistor at R2, the maximum output current threshold is set to 6.25A. These resistors can be changed to fit any output current desired. ISMON is a representation of the output current read at ISP-ISN. Please see the datasheet for more information.

## LOADEN and External Load Switch

The LT8390A can drive an external high-side PMOS as a load switch. The LOADEN pin is used to control this load switch. The EVAL-LT8390A-AZ is not equipped with an external load switch. If an external load switch is required, R25 should be installed with a short, and the copper trace for the external FET on the bottom side of the board must be cut to install the external switch. Refer to the datasheet for more information.

## Thermal Performance

The EVAL-LT8390A-AZ features excellent thermal performance due to the high efficiency of the synchronous GaN FET controller circuitry. The component temperatures of EVAL-LT8390A-AZ with a typical 24 V input and 5A load are shown in Figure 5. The four-layer PCB layout features solid copper planes that provide adequate heat spreading across the whole board. With a heatsink, EVAL-LT8390A-AZ can achieve very high power, see Figure 4.
The board can operate with an input voltage from $14.5 \mathrm{~V}-32 \mathrm{~V}$ at 5 A without a heatsink or forced air under transient conditions. If the input voltage below 14.5 V or above 32 V for over a minute is required, the circuit will require a heatsink and/or forced air flow to keep the maximum temperature of the board under $105^{\circ} \mathrm{C}$ at room temperature. With a heatsink and airflow, the board can operate at the full $\mathrm{V}_{\mathrm{IN}}$ range and load at a steady state.

## Heatsink

The EVAL-LT8390A-AZ features space for a heatsink to extend the power and thermal capabilities significantly. The board is designed for the Wakefield-Vette 567-45AB heatsink and is to be used in conjunction with thermal pads and Wurth Elektronik 9774010243 R spacers. The spacers should be soldered onto P1, P2, P3 , and P4, and a thermal pad placed between the heatsink and the GaN FETs. Properly screw in the heatsink to fully extend the power capabilities of the board.


Figure 1. EVAL-LT8390A-AZ Board Connections

Table 1. SYNC/SPRD Selection Jumper (JP1) Settings

| SHUNT POSITION | MODE PIN | MODE |
| :---: | :---: | :---: |
| 1-2 | Connected to INTV ${ }_{\text {CC }}$ | Spread Spectrum (SSFM) ON |
| 3-4 | Connected to SYNC Turret | Enables external clock synchronization |
| 5-6* | Connected to GND | Spread Spectrum (SSFM) OFF |

*Default position

## Performance

$\left(\mathrm{V}_{\text {IN }}=24 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=24 \mathrm{~V}\right.$, $\mathrm{I}_{\text {OUT }}=5 \mathrm{~A}, \mathrm{f}_{\text {SW }}=2 \mathrm{MHz}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted. $)$


Figure 2. Efficiency vs. Input Voltage at $I_{L O A D}=5 A$. While sweeping $V_{I N}$, the efficiency stays around $92 \%-96 \%$ even at high frequency and high output voltage.


Figure 4. Maximum Load Current vs. Input Voltage. With a Heatsink and airflow, the board can operate at 120 W for all $V_{\text {IN }}$.


Figure 3. Efficiency vs. Load Current. GaN FETs lower switching losses allowing for great efficiency even at 2 MHz switching.


Figure 5. Thermal Image of Top Layer at $V_{I N}=24 \mathrm{~V}$, $V_{\text {OUT }}=24 \mathrm{~V}, I_{\text {OUT }}=5 A$. Without airflow or heatsinks, the EVAL-LT8390A-AZ has great thermal performance.

## Bill of Materials

| ITEM | QTY | DESIGNATOR | DESCRIPTION | MANUFACTURER, PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| REQUIRED CIRCUIT COMPONENTS |  |  |  |  |
| 1 | 1 | C1 | CAP CER 1UF 100V 10\% X7S 0805 | MURATA, GRJ21BC72A105KE11L |
| 2 | 1 | C10 | CAP ALUM POLY 100UF 63V 20\% 10X12.6MM 1000 H | PANASONIC, 63SXV100M |
| 3 | 2 | C12, C32 | CAP CER 10UF 100V 10\% X7S 1210 | MURATA, GRM32EC72A106KE05L |
| 4 | 4 | $\begin{aligned} & \text { C14, C20, } \\ & \text { C21, C45 } \end{aligned}$ | CAP CER 10uF 50V 10\% X7R 1210 | MURATA, GRM32ER71H106KA12L |
| 5 | 1 | C2 | CAP CER 4.7uF 10V 10\% X5R 0402 LOW ESR | TDK, C1005X5R1A475K050BC |
| 6 | 4 | $\begin{aligned} & \mathrm{C} 22, \mathrm{C} 23, \\ & \mathrm{C} 35, \mathrm{C} 36 \end{aligned}$ | CAP CER 0.1uF 100V 10\% X5R 0402 | MURATA, GRM155R62A104KE14D |
| 7 | 4 | $\begin{aligned} & \text { C24, C25, } \\ & \text { C37, C38 } \end{aligned}$ | CAP CER 0.1uF 50V 10\% X5R 0402 AEC-Q200 | TAIYO YUDEN, UMK105BJ104KVHF |
| 8 | 1 | C27 | CAP CER 1uF 16V 10\% 0402 LOW ESR | TDK, C1005X6S1C105K050BC |
| 9 | 1 | C3 | CAP CER 0.47UF 16V 10\% X7S 0402 AEC-Q200 LOW ESR | TDK, CGA2B1X7S1C474K050BC |
| 10 | 2 | C4, C39 | CAP CER 1000pF 50V 1\% C0G 0402 | MURATA, GRM1555C1H102FA01D |
| 11 | 1 | C5 | CAP CER 100NF 25V 10\% X5R 0402 | TDK, C1005X5R1E104K050BC |
| 12 | 1 | C6 | CAP CER 1uF 50V 10\% X7R 0603 | TAIYO YUDEN, UMK107AB7105KA-T |
| 13 | 2 | C7, C8 | CAP CER 0.1uF 25V 10\% X7R 0402 | AVX CORPORATION, 04023C104KAT2A |
| 14 | 2 | D1, D2 | DIODE SCHOTTKY SINGLE BARRIER | NXP SEMICONDUCTORS, BAT46WJ,115 |
| 15 | 2 | D3, D4 | DIO ZNR 5.1V 5\% SOD523 | CENTRAL SEMICONDUCTOR, CMOZ5L1 TR PBFREE |
| 16 | 2 | D5, D6 | DIO SCHOTTKY BARRIER RECTIFIER, 2A | NEXPERIA, PMEG6020EPA,115 |
| 17 | 1 | L1 | IND POWER SHIELDED/MOLDED WIREWOUND 0.68UH 20\% 1MHZ COMPOSITE 22.7A <br> $0.00230 H M$ DCR AEC-Q200 | COILCRAFT INC., XGL6060-681MEC |
| 18 | 4 | $\begin{aligned} & \text { Q1, Q2, } \\ & \text { Q3, Q4 } \end{aligned}$ | TRAN MOSFET N-CH GAN 100V 60A | EFFICIENT POWER CONVERSION CORPORATION, EPC2218 |
| 19 | 1 | R1 | RES SMD 0.002 OHM 2\% 1W 1206 AEC-Q200 | SUSUMU CO, LTD, KRL3216-M-R002-G-T1 |
| 20 | 1 | R10 | RES SMD 75K Ohm 1\% 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2RKF7502X |
| 21 | 1 | R11 | RES SMD 100K Ohm 5\% 1/16W 0402 AEC-Q200 | VISHAY, CRCW0402100KJNED |
| 22 | 2 | R13, R22 | RES SMD 10 Ohm 1\% 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2RKF10R0X |
| 23 | 4 | R14, R16, R24, R26 | RES SMD 0 Ohm JUMPER 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2GE0R00X |
| 24 | 1 | R15 | RES SMD 6.2 OHM 1\% 1/16W 0402 AEC-Q200 | STACKPOLE ELECTRONICS, INC., RMCF0402FT6R20 |
| 25 | 1 | R17 | RES SMD 3.3 Ohm 1\% 1/16W 0402 | YAGEO, RC0402FR-073R3L |
| 26 | 2 | R18, R19 | RES SMD 10 OHM 5\% 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2GEJ100X |
| 27 | 1 | R2 | RES SMD 0.008 OHM 1\% 1/2W 0805 AEC-Q200 CURRENT SENSE ULTRA-LOW OHMIC CHIP | ROHM, PMR10EZPFU8L00 |
| 28 | 2 | R20, R21 | RES SMD 47 Ohm 1\% 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2RKF47R0X |
| 29 | 1 | R23 | RES SMD 59K Ohm 1\% 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2RKF5902X |
| 30 | 1 | R4 | RES SMD 18K Ohm 1\% 1/16W 0402 | YAGEO, RC0402FR-0718KL |


| ITEM | QTY | DESIGNATOR | DESCRIPTION | MANUFACTURER, PART NUMBER |
| :---: | :---: | :--- | :--- | :--- |
| 31 | 1 | R5 | RES SMD 232K Ohm 1\% 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2RKF2323X |
| 32 | 1 | R6 | RES SMD 10K Ohm 1\% 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2RKF1002X |
| 33 | 1 | R7 | RES SMD 357K Ohm 1\% 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2RKF3573X |
| 34 | 1 | R8 | RES SMD 64.9K Ohm 1\% 1/10W 0402 AEC-Q200 | PANASONIC, ERJ-2RKF6492X |
| 35 | 1 | R9 | RES SMD 124K Ohm 1\% 1/16W 0402 | YAGEO, RC0402FR-07124KL |
| 36 | 1 | U1 | IC-ADI 60V 2MHZ SYNCHRONOUS 4-SWITCH <br> BUCK-BOOST CONTROLLER WITH SPREAD <br> SPECTRUM | ANALOG DEVICES, LT8390AJUFD\#PBF |

## Evaluation Board Schematic



Figure 6. EVAL-LT8390A-AZ Evaluation Board Schematic

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
| :---: | :---: | :---: | :---: |
| 0 | $12 / 23$ | Initial Release | - |

ASSUMED BY ANALOG DEVICES FOR ITS USE, NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THIRD PARTIES THAT MAY RESULT FROM ITS USE. SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. NO LICENCE, EITHER EXPRESSED OR IMPLIED, IS GRANTED UNDER ANY ADI PATENT RIGHT, COPYRIGHT, MASK WORK RIGHT, OR ANY OTHER ADI INTELLECTUAL PROPERTY RIGHT RELATING TO ANY COMBINATION, MACHINE, OR PROCESS WHICH ADI PRODUCTS ALL INFORMATION CONTAINED HEREIN IS PROVIDED "AS IS" WITHOUT REPRESENTATION OR WARRANTY. NO RESPONSIBILITY IS OR SERVICES ARE USED. TRADEMARKS AND REGISTERED TRADEMARKS ARE THE PROPERTY OF THEIR RESPECTIVE OWNERS.

