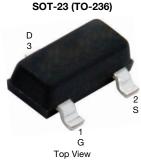
Si2122DS

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Vishay Siliconix



Marking code: G9

PRODUCT SUMMARY				
V _{DS} (V)	100			
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.160			
$R_{DS(on)}$ max. (Ω) at V_{GS} = 7.5 V	0.167			
Q _g typ. (nC)	2.9			
I _D (A) ^a	2.17			
Configuration	Single			

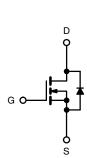
FEATURES

N-Channel 100 V (D-S) MOSFET

- TrenchFET[®] Gen IV power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- DC/DC converters / boost converters
- · Load switch
- LED backlighting in LCD TVs
- · Power management for mobile computing



RoHS

COMPLIANT

HALOGEN

FREE

N-Channel MOSFET

ORDERING INFORMATION

Package	SOT-23
Lead (Pb)-free and halogen-free	Si2122DS-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	100	V
Gate-source voltage		V _{GS}	± 20	v
	T _C = 25 °C		2.17	
	T _C = 70 °C	. [1.74	
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	I _D	1.65 ^{b, c}	
	T _A = 70 °C		1.32 ^{b, c}	A
Pulsed drain current (t = 300 µs)	I _{DM}	8	A	
Continuous source-drain diode current	T _C = 25 °C	1	2.0	
	T _A = 25 °C	I _S	1.1 ^{b, c}	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	3	
Single pulse avalanche energy	L = 0.1 MH	E _{AS}	0.45	mJ
Maximum power dissipation	T _C = 25 °C		1.6	
	T _C = 70 °C		1.0	w
	T _A = 25 °C	P _D	0.96 ^{b, c}	VV
	T _A = 70 °C		0.61 ^{b, c}	
Operating junction and storage temperature range		T _J , T _{sta}	-55 to +150	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b, d	$t \le 5 s$	R _{thJA}	100	130	°C/W
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	60	75	0/10

Notes

a. Based on T_C = 25 °C

b. Surface mounted on 1" x 1" FR4 board

c. t = 5 s

d. Maximum under steady state conditions is 166 °C/W

S23-0526-Rev. A, 03-Jul-2023

1

Document Number: 62287

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Si2122DS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static	-1 L						
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	100	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250μA	-	84	-	mV/°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-0.64	-		
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2	-	4	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	± 100	nA	
Zara gata valtaga drain averant		$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1		
Zero gate voltage drain current	IDSS	V_{DS} = 100 V, V_{GS} = 0 V, T_{J} = 55 °C	-	-	10	μA	
	R	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 2.5 \text{ A}$	-	0.133	0.160		
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, \text{ I}_{D} = 2 \text{ A}$	-	0.139	0.167	Ω	
Forward transconductance ^a	g _{fs}	$V_{DS} = 50 \text{ V}, \text{ I}_{D} = 2.5 \text{ A}$	-	7	-	S	
Dynamic ^b					•		
Input capacitance	C _{iss}		-	210	-	pF	
Output capacitance	C _{oss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	-	28	-		
Reverse transfer capacitance	C _{rss}		-	6.2	-		
Table also de ser	_	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 2 \text{ A}$	-	3.8	6		
Total gate charge	Qg		-	2.9	4.5	nC	
Gate-source charge	Q _{gs}	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 2 \text{ A}$	-	1.3	-		
Gate-drain charge	Q _{gd}		-	0.6	-		
Gate resistance	Rg	f = 1 MHz	0.7	1.5	2.5	Ω	
Turn-on delay time	t _{d(on)}	$\begin{array}{l} V_{\text{DD}} = 50 \; V, \; R_{\text{L}} = 25 \; \Omega \\ I_{\text{D}} = 2 \; A, \; V_{\text{GEN}} = 10 \; V, \; R_{\text{g}} = 1 \; \Omega \end{array}$	-	7	14	-	
Rise time	tr		-	4	8		
Turn-off delay time	t _{d(off)}		-	10	20		
Fall time	t _f		-	3	6		
Turn-on delay time	t _{d(on)}		-	8	16	ns	
Rise time	t _r	$V_{DD} = 50 \text{ V}, \text{ R}_{\text{L}} = 25 \Omega$	-	4	8		
Turn-off delay time	t _{d(off)}	$I_D = 2 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	10	20		
Fall time	t _f		-	3	6		
Drain-Source Body Diode Characteris	tics				•	•	
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	2	•	
Pulse diode forward current ^a	I _{SM}		-	-	8	A	
Body diode voltage	V _{SD}	I _S = 1.3 A	-	0.85	1.2	V	
Body diode reverse recovery time	t _{rr}		-	22	44	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 1.3 A, di/dt = 100 A/μs,	-	23	46	nC	
Reverse recovery fall time	t _a	$T_J = 25 \ ^\circ C$	-	19	-	ns	
Reverse recovery rise time	t _b		-	3	-		

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

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Si2122DS

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8

Ciss

Coss

Crss

80

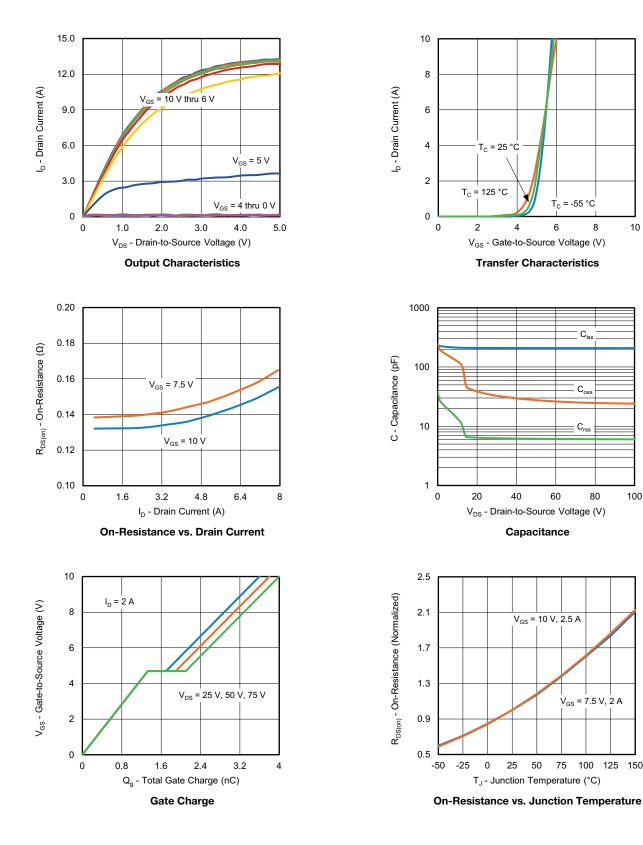
= 7.5 V, 2 A

100 125 150

10

100

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



S23-0526-Rev. A, 03-Jul-2023

3

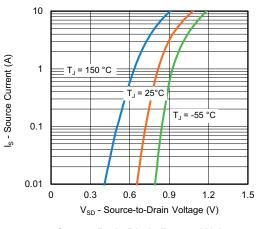
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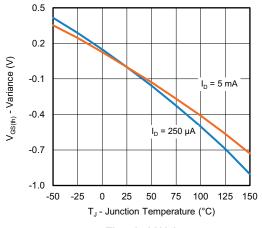


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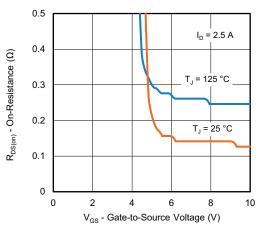
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



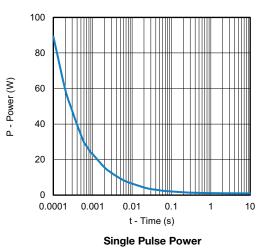
Source-Drain Diode Forward Voltage

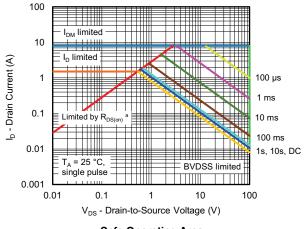


Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



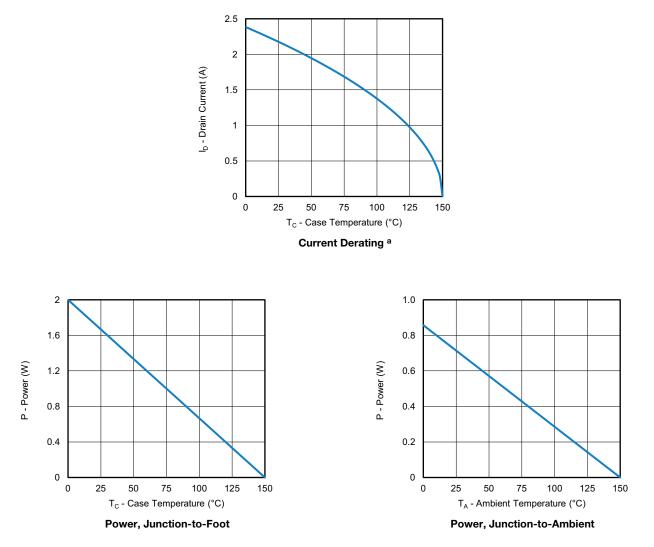


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



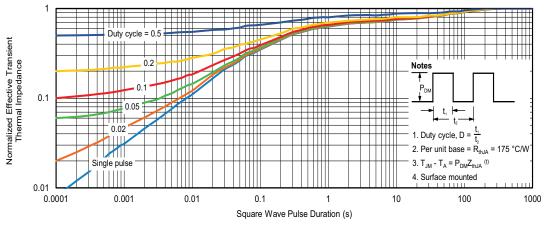
Note

a. The power dissipation P_D is based on T_J max.= 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

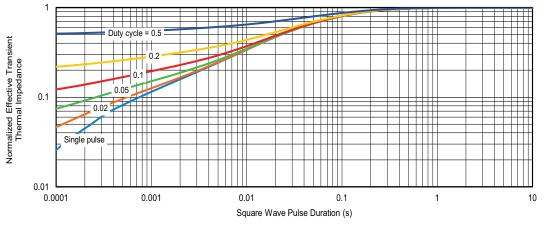


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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S23-0526-Rev. A, 03-Jul-2023	6	Document Number: 62287			
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