THAT Corporation

Pre-trimmed Low-voltage Low-power Analog Engine® Dynamics Processor IC

THAT 4320

FEATURES

- Pre-trimmed VCA & RMS detector
- Wide supply voltage range: 4.5V~16V
- Low supply current: 3.7mA typ. (5V)
- Four opamps
- One low-noise opamp (<5nV/rt-Hz)
- On board PTAT reference
- Wide dynamic range: 120dB as compander

APPLICATIONS

- Companding noise reduction
  - Wireless microphones
  - Wireless instrument packs
  - Wireless in-ear monitors
- Battery operated dynamics processors
  - Compressors
  - Limiters
  - AGCs
  - De-essers

Description

The THAT4320 is a single-chip Analog Engine® optimized for low-voltage, low-power operation. Incorporating a high-performance voltage- controlled amplifier (VCA), RMS-level sensor, and four opamps, the surface mount part is aimed at battery-operated audio applications such as wireless microphones, wireless instruments and in-ear monitors. The 4320 operates from a single supply voltage down to +4.5Vdc, drawing only 3.7mA.

This IC also works at supply voltages up to 16Vdc, making it useful in line-operated products as well. The VCA is pre-trimmed at wafer stage to deliver low distortion without further adjustment. And, one opamp is quiet enough to be used as a microphone preamp.

The part was developed specifically for use as a companding noise reduction system, drawing from THAT's long history and experience with dbx® technology for noise reduction. However, with 22 active pins, the part is extremely flexible and can be configured for a wide range of applications including single and multi-band companders, compressors, limiters, AGCs, de-essers, etc.

What really sets the 4320 apart is the transparent sound of its Blackmer® VCA coupled with its accurate true-RMS level detector. The IC is useful in battery-powered mixers, compressor/limiters, ENG devices and other portable audio products. The part is highly integrated and requires minimal external support circuitry: it even contains an on-board PTAT (proportional to absolute temperature) voltage reference to generate thermally compensated control voltages for thresholds and gain settings.

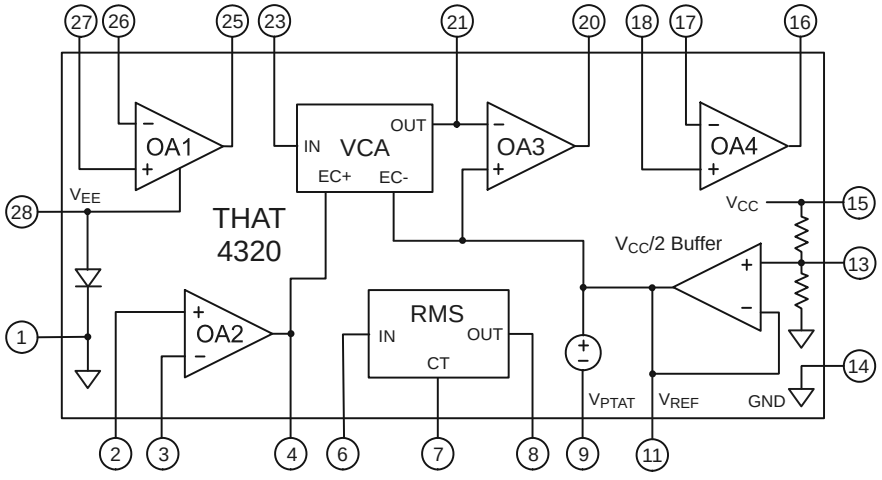

Figure 1. THAT4320 equivalent block diagram (QSOP-28 pin assignments shown)

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SPECIFICATIONS

Absolute Maximum Ratings[1]

Positive Supply Voltage (V_{CC})	+18V	Power Dissipation (P_D) at T_A=85 ºC	400mW
Supply Current (I_{CC})	30mA	Input Voltage	Supply Voltage
Operating Temperature Range (T_{OP})	-40 to +85 ºC	Storage Temperature Range (T_{ST})	-40 to +125 ºC
Junction Temperature (T_J)	-40 to +125 ºC	Lead Temperature Range (Soldering, 10 sec)	300 ºC
Output Short-Circuit Duration	30 sec		

Electrical Characteristics[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Positive Supply Voltage	V_{CC}	Referenced to GND	+4.5	-	+16	V
Negative Supply Voltage (OA_1)	V_{EE}	OA_1 only	V_{CC}-16	0	0	V
Resistive Divider Voltage	V_{PIN13}	When overridden by split supply	V_{CC} - 8	V_{CC} / 2	GND + 8	V
Supply Current	I_{CC}	No Signal				
		V_{CC}=+5 V		3.7	6	mA
		V_{CC}=+15 V		5	10	mA
	I_{EE}	V_{CC}=+5V, V_{EE}=-5 V		0.6	-	mA
Voltage Controlled Amplifier (VCA)						
Max. I/O Signal Current	$i_{IN(VCA)} + i_{OUT(VCA)}$	V_{CC} = +5 V		500		μA_{peak}
		V_{CC} = +15 V		1		mA_{peak}
Gain at 0V Control[3]	G_0	0V at +IN of OA_2	-1.5	0	+1.5	dB
Gain-Control Constant	E_{C+}/Gain (dB)	-60 dB < gain < +40 dB	-	6.0	-	mV/dB
Gain-Control Tempco	$\Delta E_C/\Delta T_{CHIP}$	Ref T_{CHIP}=27ºC	-	+0.33	-	%/ºC
Output Offset Voltage Change[4]	$\Delta V_{OFF(OUT)}$	R_{OUT} = 20 kΩ				
		0 dB gain	-	1	15	mV
		+15 dB gain	-	3	30	mV
		+30 dB gain	-	10	50	mV
Output Noise	$e_{N(OUT)}$	0 dB gain				
		22Hz~22kHz, R_{IN}=R_{OUT}=20 kΩ	-	-98	-95	dBV
Total Harmonic Distortion[3]	THD	V_{IN}= -5dBV, 1kHz, 0V at +IN of OA_2		0.05	0.1	%
RMS Level Detector						
Output Voltage at Reference i_{IN}	$e_{O(0)}$	i_{IN} = 7.5 µA RMS	-8	0	+8	mV
Output Error at Input Extremes	$e_{O(RMS)error}$	i_{IN} = 200 nA RMS		1	3	dB
		i_{IN} = 1 mA RMS		1	3	dB

1. If the devices are subjected to stress above the Absolute Maximum Ratings, permanent damage may result. Sustained operation at or near the Absolute Maximum Ratings conditions is not recommended. In particular, like all semiconductor devices, device reliability declines as operating temperature increases.
2. Unless otherwise noted, T_A=25ºC, V_{CC}=+5V, V_{EE}=0 V. Test circuit is as shown in Figure 2.
3. Assumes OA_2 is configured for unity gain, & includes offset voltage of OA_2.
4. Reference is to output offset with -80 dB VCA gain.

Electrical Characteristics (con't)[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Scale Factor Match to VCA		-20 dB < VCA gain < +20 dB				
		1 µA< $i_{IN(RMS)}$ < 100 µ A	.95	1	1.05	-
Rectifier Balance		±7.5mA DC_{IN}		±1		dB
Timing Current	I_T		-	7.5	-	µA
Filtering Time Constant	τ			3467 X C_{TIME}		s
Output Tempco	$\Delta E_O/\Delta T_{CHIP}$	Ref T_{CHIP} = 27 ºC	-	+0.33	-	%/ºC
Load Resistance	R_L	-250mV < V_{OUTRMS}< +250mV, re:Vref	2			kΩ
Capacitive Load	C_L				150	pF
Operational Amplifier OA_1[5]						
Input Offset Voltage	V_{OS}		-	± 1	± 3.5	mV
Input Bias Current	I_B		-	500	1200	nA
Input Offset Current	I_{OS}		-	± 30	± 120	nA
Input Common Mode Range	V_{ICR+}		4	4.3	-	V
	V_{ICR-}		-	0.4	0.6	V
Equivalent Input Noise Voltage	$e_{N(IN)}$	f = 1 kHz	-	4.5	6	nV/√Hz
Equivalent Input Noise Current	$i_{N(IN)}$	f = 1 kHz	-	0.9	-	pA/√Hz
Gain Bandwidth Product	GBW	f = 50 kHz	-	13	-	MHz
Slew Rate	SR	G = +10, C_L = 100 pF	2.3	4	-	V/μs
Open Loop Gain	A_{VOL}	R_L = 10 kΩ	-	95	-	dB
Output Short Circuit Current	I_{SC+}	Output to V_{CC}/2, V_{ID} = +0.4 V	-2.3	-6.5	-20	mA
	I_{SC-}	Output to V_{CC}/2, V_{ID} = -0.4 V	1.5	3.7	12	mA
Output Voltage Range	V_{O+}	R_L = 10 kΩ to V_{CC}/2, G = +10	V_{CC}-0.9	V_{CC}-0.75	-	V
	V_{O-}			V_{EE}+0.75	V_{EE}+0.95	V
Capacitive Load	C_L				150	pF
Power Supply Rejection Ratio	PSRR	+5 V < V_{CC}-V_{EE} < +15V	-	105	-	dB
Operational Amplifier OA_2 (Control Voltage Buffer)						
Input Offset Voltage	V_{OS}		-	± 1.5	± 6	mV
Input Bias Current	I_B		-	450	1000	nA
Input Offset Current	I_{OS}		-	± 25	± 100	nA
Input Common Mode Range	V_{ICR}		-1		+1	V
Equivalent Input Noise Voltage	$e_{N(IN)}$	f = 1 kHz	-	8	-	nV/√Hz
Equivalent Input Noise Current	$i_{N(IN)}$	f = 1 kHz	-	0.6	-	pA/√Hz
Gain Bandwidth Product	GBW	f = 50 kHz, C_L= 100 nF, R_L= 10 kΩ	-	0.012/C_L	-	Hz
Slew Rate	SR	G = +1		I_{SC}/C_L	-	V/µs

Electrical Characteristics (con't)[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Open Loop Gain	A_{VOL}	R_L = 10 kΩ	-	57.5		dB
				20*log(.075*RI)		dB
Output Short Circuit Current	I_{SC+}	Output to V_{CC}/2, V_{ID} = +0.4 V	-	-4	-	mA
	I_{SC-}	Output to V_{CC}/2, V_{ID} = -0.4 V	-	2.7	-	mA
Power Supply Rejection Ratio	PSRR	+5 V < V_{CC} < +15 V	-	88	-	dB
Capacitive Load [6]	C_L		22			nF
Operational Amplifier OA_3 (VCA Current-to-Voltage Converter)						
Input Offset Voltage	V_{OS}			± 1.5		mV
Input Bias Current	I_B		-	200		nA
Input Offset Current	I_{OS}			Only one input is accessible		
Input Common Mode Range	V_{ICR}			Not meaningful		
Equivalent Input Noise Voltage	$e_{N(IN)}$	f = 1 kHz	-	10.5	-	nV/√Hz
Equivalent Input Noise Current	$i_{N(IN)}$	f = 1 kHz	-	0.3	-	pA/√Hz
Gain Bandwidth Product	GBW	f = 50 kHz	-	7.3	-	MHz
Slew Rate	SR	C_L = 100 pF	-	3.2	-	V/μs
Open Loop Gain	A_{VOL}	R_L = 10 kΩ	-	92	-	dB
Output Short Circuit Current	I_{SC+}	Output to V_{CC}/2		-3.5	-	mA
	I_{SC-}			2.5	-	mA
Output Voltage Range		R_L = 10 kΩ to V_{CC}/2, Rf = 20 kΩ, 0 dB VCA gain				
	V_{O+}	$I_{in(VCA)}$ = +100 μA	4.1	4.25	-	V
	V_{O-}	$I_{in(VCA)}$ = -100 μA		0.75	0.9	V
Capacitive Load	C_L				150	pF
Operational Amplifier OA_4						
Input Offset Voltage	V_{OS}		-	± 1.5	± 5	mV
Input Bias Current	I_B		-	200	500	nA
Input Offset Current	I_{OS}		-	± 10	± 50	nA
Input Common Mode Range	V_{ICR+}		4	4.3	-	V
	V_{ICR-}		-	0.4	0.6	V
Equivalent Input Noise Voltage	$e_{N(IN)}$	f = 1 kHz	-	10.5	14	nV/√Hz
Equivalent Input Noise Current	$i_{N(IN)}$	f = 1 kHz	-	0.3	-	pA/√Hz
Gain Bandwidth Product	GBW	f = 50 kHz	-	7.3	-	MHz
Slew Rate	SR	G = +10, C_L = 100 pF	2.0	3.2	-	V/μs
Open Loop Gain	A_{VOL}	R_L = 10 kΩ	-	92	-	dB

5. OA_1 is stable for closed-loop gains of 2 or greater.
6. Note - OA_2 and the V_{CC}/2 buffer require a capacitve load for stability.

Electrical Characteristics (con't)[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Short Circuit Current	I_{SC+}	Output to $V_{CC}/2$, V_{ID} = +0.4 V	-1.3	-3.5	-12	mA
	I_{SC-}	Output to $V_{CC}/2$, V_{ID} = -0.4 V	1	2.5	8	mA
Output Voltage Range	V_{O+}	R_L = 10 kΩ to $V_{CC}/2$, G = +10	4.1	4.25	-	V
	V_{O-}			0.75	0.9	V
Capacitive Load	C_L				150	pF
Power Supply Rejection Ratio	PSRR	+5V < V_{CC} < +15 V	-	100	-	dB
$V_{CC}/2$ Reference Buffer						
Reference Voltage	V_{REF}	No Signal, No load on pin 13,				
		V_{CC} = +5 V, R_L= 3 kΩ to V_{CC} or GND	2.4	2.5	2.6	V
		V_{CC} = +15 V	-	$V_{CC}/2$	-	V
Voltage Divider Impedance	R_A, R_B		-	20	-	kΩ
Output Short Circuit Current	I_{Osc-}	Output to V_{CC}		-3		mA
	I_{Osc+}	Output to GND		4.5		mA
Output Noise Voltage	$e_{N(OUT)}$	22 Hz ~ 22 kHz, C_{FILT}= 22 μF	-	-120	-117	dBV
Capacitive Load[6]	C_L		22			nF
Proportional To Absolute Temperature (PTAT) Voltage Generator						
Output Voltage	V_{PTAT}	R_L = 10 kΩ, T_{CHIP} = 25 ºC	-	V_{REF} - 0.072	-	V
VCA Gain Change Caused by V_{PTAT}		V_{PTAT} applied to OA_2, A_V = +1				
		VCA Gain at 1 kHz	-11	-12	-13	dB
Output Tempco	$\Delta(V_{PTAT}-V_{REF})/\Delta T_{CHIP}$	Ref T_{CHIP} = 27 ºC	-	+0.33	-	%/ºC
Maximum Sink Current	$I_{SINK(MAX)}$		800			μA
Capacitive Load	C_L				150	pF
Performance as a Compander[7] (through an encode-decode cycle)						
Dynamic Range		(Max signal level) - (No Signal Output Noise)		120		dB
Distortion	THD	f = 1 kHz		0.1		%
Frequency response	-20 dB re: Max Signal	20 Hz ~ 20 kHz		± 1.5		dB

Package Characteristics

Parameter	Symbol	Conditions	QSOP-28	QFN-24	Units
Surface Mount Packages		See page 16 for pinouts and dimensions			
Thermal Resistance	θ_{JA}	Package soldered to board. Thermal pad not soldered on QFN[8]	90	70	ºC/W
Environmental Regulation Compliance			Complies with July 21,2011 RoHS 2 Requirements		
Soldering Reflow Profile			JEDEC JESD22-A113-D (260 ºC)		
Moisture Sensitivity Level		Above-referenced JEDEC soldering profile	MSL-1	MSL-1	

7. Compressor circuit is as shown in Figure 12, Expander circuit is as shown in Figure 13.
8. For best VCA THD performance, QFN thermal pad should not be soldered to the PCB.

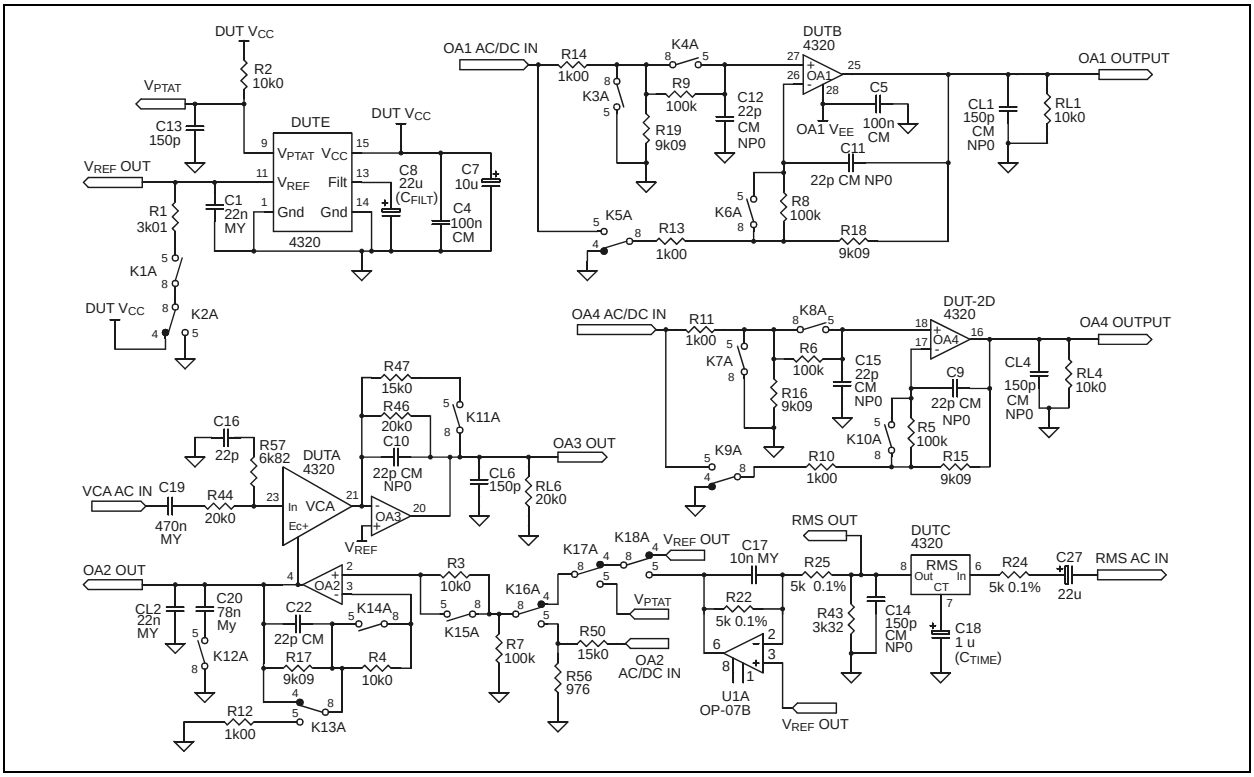


Figure 2. 4320 Test Circuit Schematic (QSOP-28 pin assignments shown)

REPRESENTATIVE DATA

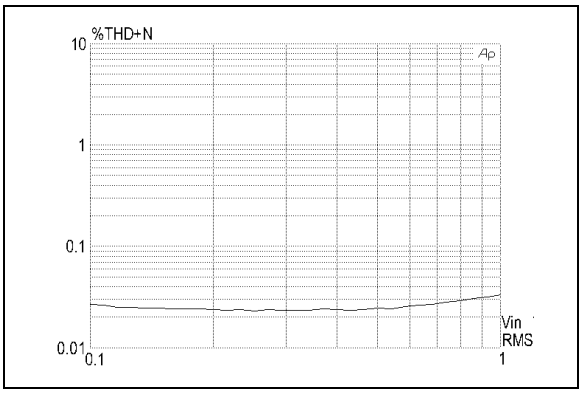


Figure 3. VCA THD vs. Level at 0 dB gain (BW=22kHz)

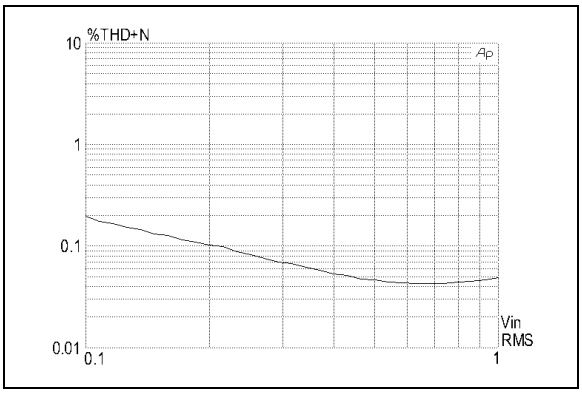


Figure 4. VCA THD vs. Level at +12 dB gain (BW=22kHz)

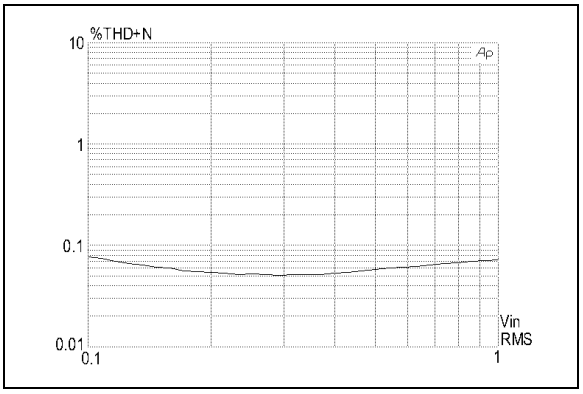


Figure 5. VCA THD vs. Level at -12 dB gain (BW=22kHz)

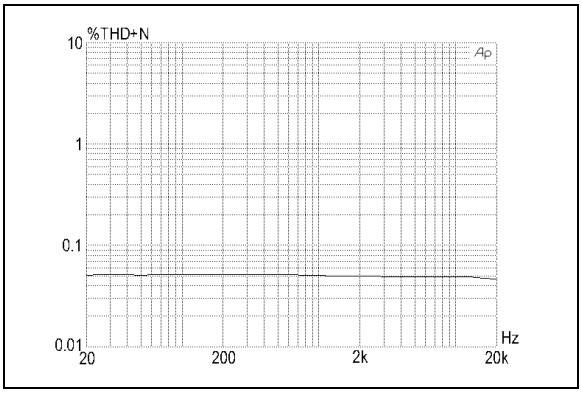


Figure 6. VCA THD vs. Frequency (BW=80kHz)

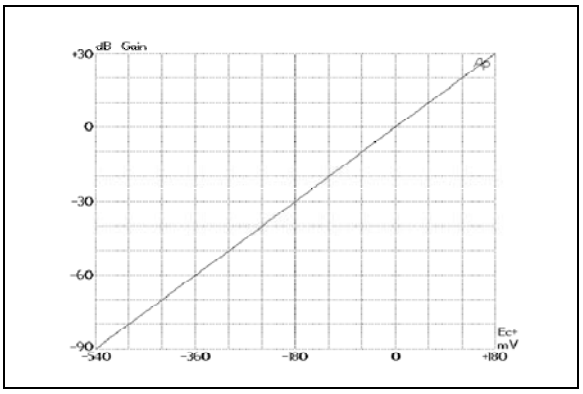


Figure 7. VCA Gain vs. Control Voltage

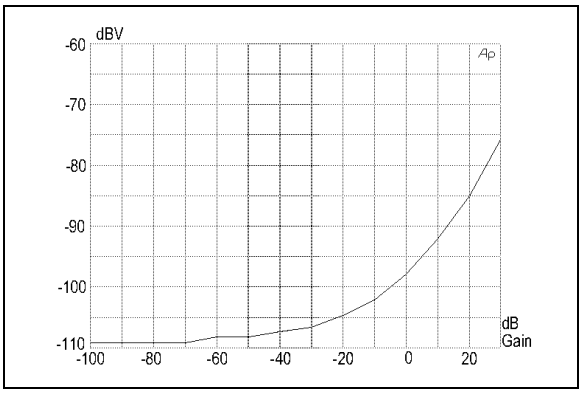


Figure 8. VCA Noise vs. Gain (BW=22kHz)

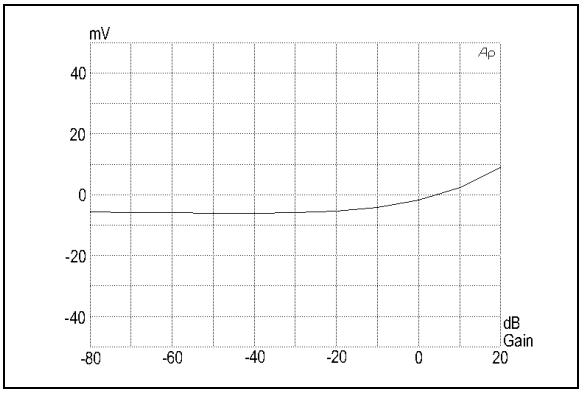


Figure 9. VCA Offset vs. Gain

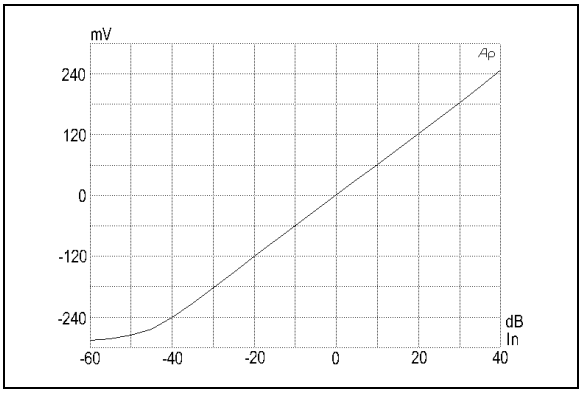


Figure 10. RMS Output vs. Level

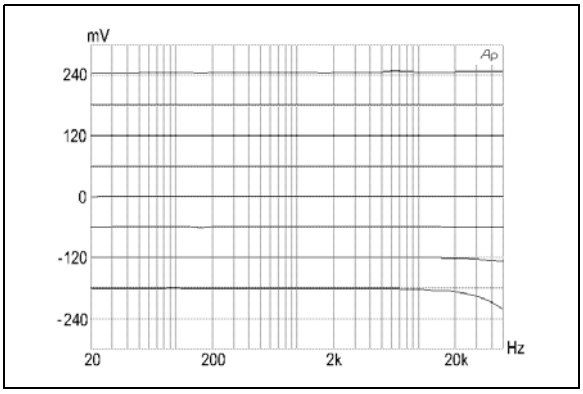


Figure 11. RMS Frequency Response vs. Level

Theory of Operation

The THAT 4320 Dynamics Processor combines THAT Corporation's proven Voltage-Controlled Amplifier (VCA) and RMS-Level Detector designs with four general-purpose opamps to produce an Analog Engine useful in a variety of dynamics processor applications. The part is integrated using a proprietary, fully complementary, dielectric-isolation process. This process produces very high-quality bipolar transistors (both NPNs and PNPs) with unusually low collector-substrate capacitances. The 4320 takes advantage of these devices to deliver wide bandwidth and excellent audio performance while consuming very low current and operating over a wide range of power supply voltages.

For details of the theory of operation of the VCA and RMS Detector building blocks, the interested reader is referred to THAT Corporation's data sheets on the 2180-Series VCAs and the 2252 RMS Level Detector. Theory of the interconnection of exponentially-controlled VCAs and log-responding level detectors is covered in

THAT Corporation's design note DN01, The Mathematics of Log-Based Dynamic Processors.

The VCA — in Brief

The VCA in THAT 4320 is based on THAT Corporation's highly successful complementary log-antilog gain cell topology -- The Blackmer® VCA -- as used in THAT 2180-Series IC VCAs. VCA symmetry is trimmed during wafer probe for minimum distortion. No external adjustment is allowed. See Figures 3 ~ 6, page 6 for the representative THD data.

Input signals are currents in the VCA's IN pin. This pin is a virtual ground with dc level approximately equal to V_{REF}, so in normal operation an input voltage is converted to input current via an appropriately sized resistor (R_{44} in Figure 2, Page 6). Because the currents associated with dc offsets present at the input pin and any dc offset in preceding stages will be modulated by gain changes (thereby becoming audible as thumps), the input pin is normally ac-coupled (C_{19} in Figure 2).

The VCA output signal is also a current, inverted with respect to the input current. In normal operation, the output current is converted to a voltage via inverter OA_3, where the ratio of the conversion is determined by the feedback resistor (R_{46} or R_{47}, Figure 2) connected between OA_3's output and its inverting input. The signal path through the VCA and OA_3 is noninverting.

The gain of the VCA is controlled by the voltage applied between E_{C+} and E_{C-}. Note that E_{C-} is an internal node connected to the V_{REF} generator. Gain (in decibels) is proportional to ($E_{C+} - E_{C-}$). See Figure 7 [page 7]. The constant of proportionality is 6.0 mV/dB for the voltage at E_{C+} (relative to V_{REF}).

The VCA's noise performance varies with gain in a predictable way, but due to the way internal bias currents vary with gain, noise at the output is not strictly the product of a static input noise times the voltage gain commanded. Figure 8 [page 7] plots noise (in dBV — referenced to 1 V — in a 22 kHz bandwidth) at the output of OA_3 vs. VCA gain commands over a range of -100 dB to +30 dB gain. At large attenuation, the noise floor of ~-109 dBV is limited by the input noise of OA_3 and its feedback resistor. At 0 dB gain, the noise floor is ~-98 dBV as specified. In the vicinity of 0 dB gain, the noise increases more slowly than the gain: approximately 5 dB noise increase for every 10 dB gain increase. Finally, as gain approaches 30 dB, output noise begins to increase directly with gain.

While the 4320's VCA circuitry is very similar to that of the THAT 2180 Series VCAs, there are several important differences, as follows.

1) Supply current for the VCA depends on V_{CC}. At +5 V V_{CC}, approximately 500 μA is available for the sum of input and output signal currents. This increases to about 1 mA at +15 V V_{CC}. (Compare this to ~1.8 mA for a 2180 Series VCA when biased as recommended. This is appropriate given the lower supply voltage for the 4320.)

2) The signal current output of the VCA is internally connected to the inverting input of on-chip opamp OA_3. In order to provide external feedback around this opamp, this node is brought out to a pin.

3) Only the E_{C+} node is available for gain control. A SYM control port (similar to that on the 2180 VCA) exists, but is driven from an internally trimmed current generator. The negative control port (E_{C-}) is internally connected to V_{REF}.

4) The control-voltage constant is approximately 6.0 mV/dB, due primarily to the lower internal operating temperature of the 4320 compared to that of the 2180 Series (and the 4301).

5) The OTA used for the VCA's internal opamp in the 4320 uses less emitter degeneration resistance in its output than that of the 2180 VCA. This requires that the source impedance at the VCA's input (which is a summing junction) must be under 5 kΩ at frequencies over 1 MHz. In Figure 2, C_{16} and R_{57} accomplish this. See the applications section for an alternative on how to address this issue.

The RMS Detector — in Brief

The 4320's detector computes RMS level by rectifying input current signals, converting the rectified current to a logarithmic voltage, and applying that voltage to a log-domain filter. The output signal is a dc voltage proportional to the decibel-level of the RMS value of the input signal current. Some ac component (at twice the input frequency) remains superimposed on the dc output. The ac signal is attenuated by a log-domain filter, which constitutes a single-pole rolloff with cutoff determined by an external capacitor and a programmable dc current.

As in the VCA, input signals are currents to the RMS IN pin. This input is a virtual ground with dc level equal to V_{REF}, so a resistor (R_{24} in Figure 2) is normally used to convert input voltages to the desired current. The level detector is capable of accurately resolving signals well below 10 mV (with a 5 kΩ input resistor). However, if the detector is to accurately track such low-level signals, ac coupling is normally required (C_{27} in Figure 2). Note also that small, low-voltage electrolytic capacitors used for this purpose may create significant leakage if they support half the supply voltage, as is the case when the source is dc-referenced to ground. To

ensure good detector tracking to low levels, a tantalum capacitor or high-voltage electrolytic may be required for input coupling.

The log-domain filter cutoff frequency is usually placed well below the frequency range of interest. For an audio-band detector, a typical value would be 5 Hz, or a 32 ms time constant (τ). The filter's time constant is determined by an external capacitor C_{TIME} attached to the C_T pin, and an internal current source (I_T) connected to C_T. The current source is internally fixed at 7.5 μA. The resulting time constant in seconds is approximately equal to 3467 * C_{TIME}. Note that, as a result of the mathematics of RMS detection, the attack and release time constants are fixed in their relationship to each other.

The RMS detector is capable of driving large spikes of current into C_{TIME}, particularly when the audio signal input to the RMS detector increases suddenly. This current is drawn from V_{CC} at pin 15 (QFN pin 16), fed through C_{TIME} at pin 7 (QFN pin 10), and returns to the power supply through the ground end of C_{TIME}. If not handled properly through layout and bypassing, these currents can mix with the audio with unpredictable and undesirable results. As noted in the Applications section, local bypassing from the V_{CC} pin to the ground end of C_{TIME} is strongly recommended in order to keep these currents out of the ground structure of the device.

The dc output of the detector is scaled with the same constant of proportionality as the VCA gain control: 6.0 mV/dB. See figure 10 [page 7]. The detector's 0 dB reference (i_{in0}), the input current which causes the detector's output to equal V_{REF}), is trimmed during wafer probe to approximately equal 7.5 μA. The RMS detector output stage is capable of sinking or sourcing 125 μA. It is also capable of driving up to 150 pF of capacitance.

Frequency response of the detector extends across the audio band for a wide range of input signal levels. Note, however, that it does fall off at high frequencies at low signal levels. See figure 11 (page 7).

Differences between the 4320's RMS Level Detector circuitry and that of the THAT 2252 RMS Detector include the following.

1) The rectifier in the 4320 RMS Detector is internally balanced by design, and cannot be balanced via an external control. The 4320 will typically balance positive and negative halves of the input signal within 10 %, but in extreme cases the mismatch may reach +40, -30 % (±3 dB). However, even such extreme-sounding mismatches will not significantly increase ripple-induced distortion in dynamics processors over that caused by signal ripple alone.

2) The time constant of the 4320's RMS detector is determined by the combination of an external capacitor (connected to the C_T pin) and an internal current source. The internal current source is set to about 7.5 μA. A resistor is not normally connected directly to the C_T pin on the 4320.

3) The 0 dB reference point, or level match, is also set to approximately 7.5 μA. However, as in the 2252, the level match will be affected by any additional currents drawn from the C_T pin.

The Opamps — in Brief

The four opamps in the 4320 have been optimized independently to suit each one's intended application. While they all use PNP input stages, they differ in bandwidth, noise level, and compensation scheme depending on their expected uses. Therefore, to get the most out of the 4320, it is useful to know the major differences among these opamps.

OA_1 - Low Source Impedance Pre-amp

OA_1, with typical equivalent input noise of 4.5 nV/√Hz, is the quietest opamp on the 4320. This opamp is intended for signal conditioning such as preamplification from low-impedance sources. (At source impedances of >5.6 kΩ, the input current noise contribution will surpass the voltage contribution.)

OA_1 is stable for closed-loop gains of 2 or greater. Its output typically swings to within 0.75 V of V_{CC} or V_{EE}, allowing it to support a 1.2 V_{RMS} sine wave from a single +5 V supply (4.75 V_{RMS} with a +15 V supply). Its typical slew rate is ~ 4 V/μs, allowing the part to support maximum level sine waves at up to 360 kHz on a +5 V supply (94 kHz on a +15 V supply). OA_1's output is capable of driving up to 150 pF, so it is possible to directly bypass RF to ground via a small capacitor at OA_1's output, as is often desired in wireless transmitter applications.

OA_1's most unusual feature[9] is that it's negative power supply connection is brought out separately to V_{EE} at pin 28 (QFN pin 3) to provide additional headroom in certain applications. While V_{EE} is normally connected to the power supply ground (and pins 1 and 14 (QFN pin 4 and 15), which are the ground connections for the rest of the chip), it can be connected to a separate negative supply. OA_1's positive supply connection is internally connected to V_{CC} at pin 15 (QFN pin 16). Therefore, OA_1 sees as its supply voltage the difference between V_{CC} and V_{EE}. Note that this difference must not exceed 16 V.

To gain an advantage from the separate V_{EE} connection for this opamp, the design must provide a negative

9. THAT has applied for patent coverage on this novel approach.

supply below ground to this pin. By doing, so, OA_1 can gain additional voltage swing over that available to the rest of the IC. Because OA_1 is commonly used as a pre-amp before a noise reduction compressor based on the rest of the chip, headroom is most critical at this point. (The VCA will reduce the audio signal's dynamic range to a more manageable level for subsequent stages.) The rest of the chip can run from +5 V and ground to maintain low power dissipation, while only OA_1 is run from, say, a ±5 V supply to gain additional headroom.

To see how this works in practice, suppose V_{CC} is +5 V. If V_{EE} is set to 0 V (ground), the maximum swing at OA_1's output is typically 3.5 V (typically, OA_1 reaches within ~0.75 V of its supply rails), If, instead, V_{EE} is set to -5 V, the maximum swing at OA_1's output increases to 8.5 V — for a 7.7 dB increase in dynamic range!

OA_2 - Control Voltage Buffer

OA_2 is intended as a control voltage buffer, and is the least general purpose of the four opamps. It is externally compensated, and requires at least 22 nF at its output to remain stable. This was a deliberate design choice based on several factors including the relatively limited bandwidth and voltage swing required for the VCA control port and the importance of low noise (and low RF content) at this node. Additionally, the capacitive high-frequency output impedance guarantees stability in the VCA.

Because it is intended to handle only the VCA control port signal (consisting primarily of dc with added low frequency content), OA_2 is optimized for dc at the expense of ac performance. This opamp has limited input compliance (±1 V common mode range), is relatively slow (120 kHz gain-bandwidth product with a typical 100 nF capacitive load), has low open-loop gain (57 dB with the typical 10 kΩ resistive load), and has approximately a 10 Ω output impedance. These characteristics, while limiting in an opamp intended for handling audio signals, are ideal for the control voltage buffer. In particular, compensating the opamp at its output takes advantage of an often-required RF-bypass capacitor to minimize noise pickup at the sensitive VCA control port.

OA_3 - VCA Current-to-Voltage Converter

OA_3 is intended to translate the VCA's output currents into voltage signals. It is a unity-gain stable, 7.3 MHz opamp with moderately low input noise of 10.5 nv/√Hz. This noise floor complements that of the VCA.

Like OA_1, because it handles audio signals directly, OA_3 is optimized for audio performance. It's output typically swings to within 0.75 V of V_{CC} or ground, allowing it to support a 1.2 V_{RMS} sine wave from a single +5 V supply (4.75 V_{RMS} with a +15 V supply). It's typical slew rate is ~3.2 V/μs, allowing the part to support maximum level sine waves at up to 290 kHz on a +5 V supply (75 kHz on a +15 V supply).

As with the other opamps, OA_3's output is capable of driving up to 150 pF, so it is possible to directly bypass RF to ground via a small capacitor at OA_3's output. It's output section is capable of supplying at least 1 mA, making it possible to use this opamp directly as the output stage in lightly loaded applications. Note, however, that OA_3's output is not designed to withstand an indefinite short-circuit to a power supply or ground rail, and a resistor should be included in series with such outputs to ensure stability with capacitive loads larger than 150 pF.

OA_4 - General Purpose OpAmp

OA_4 is intended for either signal or control voltage applications. It is a unity-gain stable, 7.3 MHz opamp with moderately low input noise voltage of 10.5 nV/√Hz, and moderately low input noise current of 0.3 pA/√Hz. Because of it's lower current noise, OA_4 is a better choice for an audio pre-amp than OA_1 in cases where the source impedance feeding it is high.

All other characteristics of OA_4 are similar to those of OA_3.

$V_{CC}/2$ Reference Buffer

For single-supply applications, the 4320 requires a center-tap to provide a synthetic "ground" reference for its circuitry. The 4320 contains a built-in resistive divider (at pins 13/14/15), followed by a buffer, to provide a low-impedance source at approximately half V_{CC}. Note that the center tap of the resistive divider is brought out to filter the voltage, thereby minimizing noise in the divider. A large electrolytic capacitor (typically 22 μF or greater) is used for this purpose.

The output of the buffer is available at pin 11. This is "V_{REF}". The buffer is capable of delivering ~3 mA at its output. Like OA_2, it is compensated by capacitance at its output, working against an internal output impedance of approximately 10 Ω; at least 22 nF should be used to ensure stability, reduce high-frequency output impedance, and attenuate high-frequency noise.

V_{REF} may be used to supply a "ground" reference voltage to other sections of circuits beyond the 4320 itself. However, in any such uses, the designer should take care to minimize currents, especially signal currents, that flow through the V_{REF} line. Any signal currents should return to the real circuit ground (GND); V_{REF} should be connected only to relatively high impedance loads (e.g., the positive input of opamps). Where

significant currents (signal or otherwise) must be delivered at the V_{REF} dc level, an opamp should be used to buffer the V_{REF} line itself.

Another approach to power supply arrangements is to operate the 4320 from symmetrical split supplies (e.g., ±5 V and ground). In such cases, the center-tap of the resistive divider at pin 13 (QFN pin 14) should be grounded. This will force V_{REF} to very nearly ground (within the offset of the $V_{CC}/2$ buffer).

A final note on the subject of power supply connections is that both of the 4320's two GND, pins 1 and 14 (QFN pins 4 and 15), *must* be tied together for proper operation of the device. While these pins *are* tied together internally on the chip, due to the large size of the die inside the part, the resistance and inductance of the internal connection is not as low as an external PCB trace can provide. The 4320 may not meet all its specifications unless a short PCB connection is made between these two pins.

PTAT Voltage Generator

The VCA control port and the RMS-level detector output both share a fundamental temperature drift proportional to absolute temperature. Room temperature is approximately 300 ºK (or 27 ºC), so near room temperature the drift amounts to +0.33 %/ºC. The drift is expressed in *percent* per degree Celsius because the magnitude of the change with temperature depends on the gain control command or detected level being presented. There is *no* temperature drift at 0 dB gain, or at the RMS' reference level. But, away from either of these 0 dB points, the scale factor of these parameters varies by 0.33 % for each degree Celsius of temperature change.

The PTAT voltage generator produces an output that varies directly with absolute temperature. At 25 ºC, it's output is 72 mV. One end of the generator is connected to V_{REF}, the other (negative end) is buffered and brought out at V_{PTAT} at pin 9 (QFN pin 12). While one application for the voltage on this pin might be to read the temperature of the IC, it has many important practical uses in audio applications based on the 4320. Basically, it provides a voltage that can be used, after appropriate scaling, to supply any gain controls or offsets used to condition the RMS detector output and/or the VCA gain control signals.

An example may help make this clear. Suppose a designer wants to provide a potentiometer to control signal gain through the VCA. If the desired gain range is 0 to +20 dB, the VCA control port must be driven from 0 mV (for 0 dB gain) to +120 mV (for +20 dB gain), but *only at room temperature*. (At room temperature, the gain control constant is 6.0 mV/dB.) If the temperature increases by 10 ºC, the voltage for 0 dB gain remains the same, but that for 20 dB gain increases by 3.3 %, to 124 mV. If the same 120 mV gain command is applied (because it comes from a source that does not vary with temperature), the gain will be 19.35 dB, not 20 dB.

If the supply that feeds the gain-control pot derives from a stable voltage source, the commanded gain will drift with temperature. Alternatively, if the supply can be made to *vary* with temperature just as the control port's sensitivity drifts, the two can compensate each other and the result will be stable. That is the purpose of the 4320's PTAT voltage generator: to supply a voltage that drifts *exactly* as the VCA and the RMS detector drifts. The PTAT voltage can be used, with appropriate scaling, to reference all gain controls, gain offsets, and threshold setting amplifiers throughout the level-processing side chain. And, because the PTAT generator is integrated on the same IC as its VCA and RMS detector, temperature tracking between these three components is excellent.

The No Connection Pins

Some pins on the THAT4320 are labeled "No Connection" (N/C). These pins are not internally connected to the 4320 die, so it is acceptable to leave these pins unconnected or to connect these pins to some external circuit nodes. In fact, the placement of the N/C pins was chosen partly to facilitate passive guarding to certain pins which are sensitive to low-level leakage currents (e.g., the RMS and VCA inputs).

Because the dc potential at the most sensitive circuit nodes is very close to V_{REF}, THAT Corporation recommends that all the N/C pins be connected to V_{REF} wherever possible. However, layout constraints may preclude such a connection. In this case, either leave the pins open, or choose a slow moving (dc) signal that is close in dc potential to V_{REF}, such as V_{PTAT}. Tying the N/C pins to V_{CC} or GND -- *not recommended* -- will guard against AC signals, but runs the risk of generating unanticipated dc leakage currents which can spoil the performance of the 4320's VCA and RMS detector.

Noise Reduction (Compander) Configurations

A primary use of the 4320 is for noise reduction systems, particularly within battery-operated devices. In these applications, one 4320 is configured for use as a compressor to condition audio signals before feeding them into a noisy channel. A second 4320, configured as an expander, is located at the receiver end of the noisy channel. The compressor increases gain in the presence of low-level audio signals, and reduces its gain in the presence of high-level audio signals. The expander works in opposite, complementary fashion to restore the original signal levels present at the input of the compressor.

During low-level audio passages, the compressor increases signal levels, bringing them up above the noise floor of the noisy channel. At the receiving end, the expander reduces the signal back to it's original level, in the process attenuating the channel noise.

During high-level audio passages, the compressor decreases signal levels, reducing them to fit within the headroom limits of the noisy channel. The expander increases the signal back to its original level. While the channel noise may be increased in this action, a well-designed compander will mask the noise floor with the signal itself.

The 4320 was designed to facilitate the design of a wide variety of companding noise reduction systems. The RMS detector responds accurately over a wide range of levels; the VCA responds accurately to a wide range of gain commands; the detector output and the VCA control input are fully configurable; and the part contains enough opamps to provide many options in signal conditioning. All these features mean that the 4320 will support a wide range of compander designs (and more), including simple 2:1 wide range (level-independent) systems, level-dependent systems with thresholds and varying compression slopes, systems including noise gating and/or limiting, and systems with varying degrees of pre-emphasis and filtering in both the signal and detector paths. Furthermore, much of this can be accomplished by extensively conditioning the control voltage sidechain rather than the audio signal itself. The audio signal can pass through as little as one VCA and one opamp, and still support multiple ratios, thresholds, and time constants.

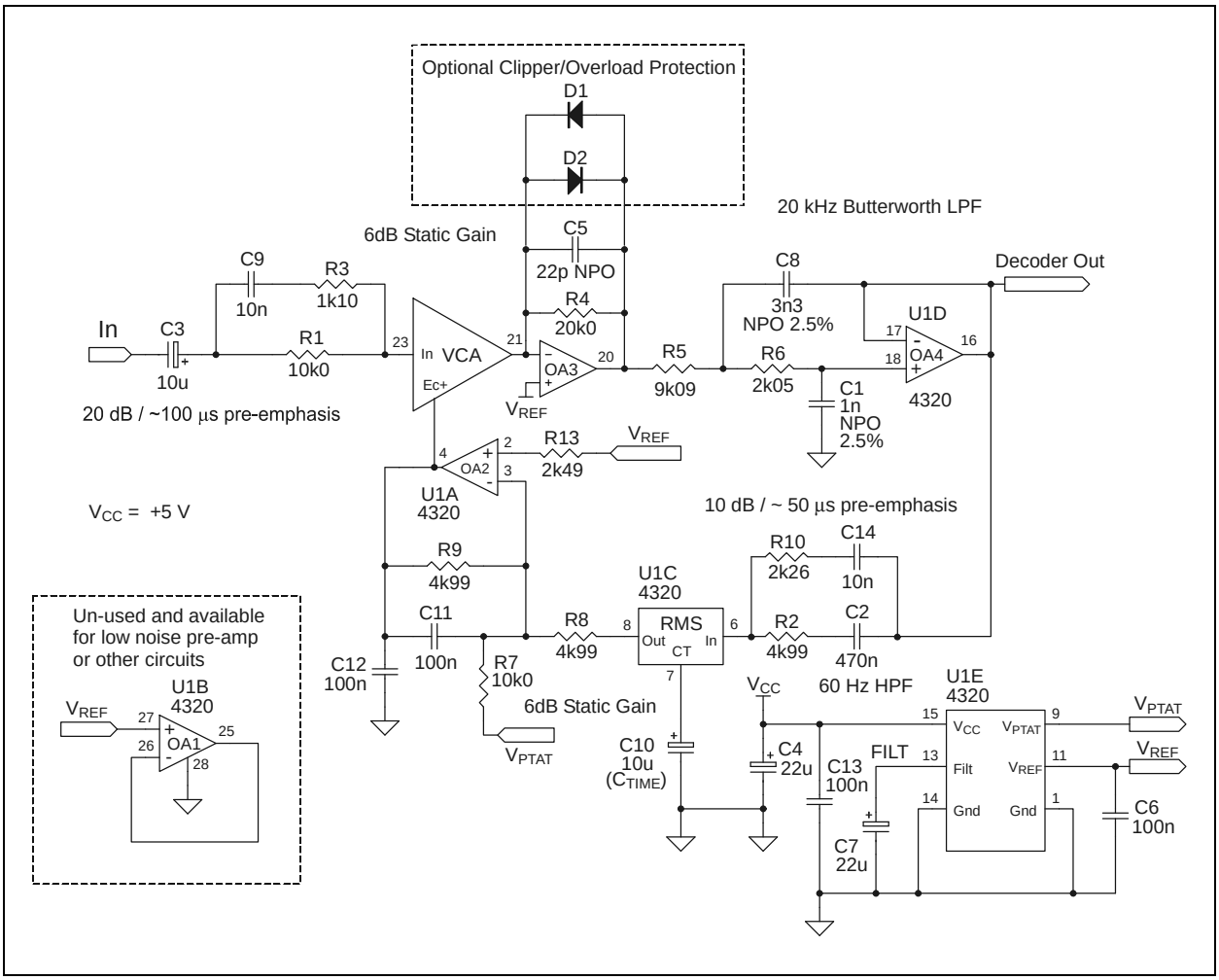


Figure 12. THAT4320 2:1 Encoder Circuit (QSOP-28 pin assignments shown)

Applications

The 4320 includes so many useful building blocks and operates from such a wide range of supply voltages that it is suitable for a wide variety of dynamics processing applications. Chief among these are wireless companding systems. For this datasheet, we show the part in a simple 2:1 companding noise reduction system that performs as well or better than any analog companding solution on the market today. Many other configurations of the 4320 are possible, but are not shown here. THAT intends to publish additional circuits in forthcoming applications notes. Please check with THAT's applications engineering department to see if your application has been covered yet, and for personalized assistance with specific designs.

The encoder

Figure 12 shows a simple 2:1 encoder or feedback compressor. The encoder in a wireless companding system is located in the transmitter and generally operates from a battery supply.

To optimize signal levels within the voltage limitations of the battery supply, the encoder VCA gain is offset by 6 dB via the ratio of R_4 to R_1. Additionally, another 6 dB of static gain is injected at the control port opamp, via V_{PTAT} and R_7. (A 36 mV dc offset is required to produce 6 dB of static gain. Since $V_{PTAT} \sim$ -72 mV, a gain of -1/2 will create the required 36 mV. Because the PTAT generator voltage tracks in temperature with the VCA gain control constant, this gain will be stable over temperature.)

This encoder includes a high-frequency pre-emphasis network at the input of the VCA (R_3/C_9) that ultimately provides 20 dB of gain at 20 kHz. Its lower corner frequency is at approximately 1.5 kHz (f_1); the upper corner is near 15 kHz (f_2).

Companding noise reduction encoders often include a clipper somewhere in the signal path to prevent overmodulation of the RF channel. The optional anti-parallelled diodes D_1 and D_2, can perform that function in this circuit, and should be placed ahead of the 20 kHz Butterworth low-pass filter composed of OA_4 and its surrounding components. This placement helps reduce "spectral splatter" that results from momentary clipping. What clipping takes place is limited in duration to transients only, since the encoder will eventually reduce its gain to below the clip point.

The output of the low-pass filter is the output of the encoder. This is where the input to the RMS detector is derived. The input circuit for the RMS detector includes another pre-emphasis network which provides a maximum of 10 dB of pre-emphasis (R_{10}/C_{14}), rising at approximately 2.9 kHz (f_3), and stopping at around 6.5 kHz (f_4). These frequencies were chosen such that

$$\sqrt{f_1 \times f_2} = \sqrt{f_3 \times f_4}$$

This effectively centers the rising sections of both the RMS and VCA pre-emphasis curves. This network feeds the input of the RMS detector, which is a virtual ground referenced to V_{REF}.

As described in the Theory of Operation section "The RMS Detector - In Brief" (on page 9), the RMS detector is capable of driving large spikes of current into the averaging capacitor C_{TIME}. To prevent these currents from upsetting circuit grounds, it is necessary to bypass V_{CC} to a point very near the grounded end of the C_{TIME} with a capacitor (C_4 in Figure 12) equal to or greater than the value of C_{TIME}. The grounded ends of these two capacitors should be connected together before being tied to the rest of the ground system. Doing so will ensure that the current spikes flow within the local loop consisting of the two capacitors, and stay out of the ground system. This requirement applies to the decoder and other applications of the THAT4320 as well.

The output of the RMS detector is zero volts when the RMS input current is equal to the timing current (internally set to ~7.5 μA). A low-frequency voltage level of -26 dBu was chosen as the desired zero dB reference since this, in conjunction with the applied static gain, makes optimal use of the available gain in the VCA. Then, the RMS detector's low-frequency input resistance can be calculated as:

$$R2 = \frac{0.775 \times 10^{\frac{-26}{20}}}{7.5\,\mu A} \cong 4.99\,k\Omega$$

From the desired 10 dB pre-emphasis, the value for R_{10} can then be calculated to be 2.26 kΩ. C_{14} is calculated based on the desired pre-emphasis starting frequency.

In THAT Corporation's design note DN03, A Signal Limiter for Power Amplifiers, the compression ratio for a feedback compressor was derived using the analytical technique described in DN01A, The Mathematics of Log Based Dynamics Processors. This technique is referred to as 'working in the log domain'. Using these methods, it can be shown that the compression ratio (C.R.) of a feedback compressor is

C.R. = 1 + A,

where A is the absolute value of the gain of the side chain.

The RMS detector's output is connected to the VCA gain control port (E_{C+}) through OA_2, configured for an

inverting gain of one. This fixes the compression ratio at 2:1. Note that the negative sign in the side chain gain makes this circuit a compressor.

The decoder

Figure 13 shows the THAT4320 configured as a 2:1 expander, an arrangement intended to complement the encoder in Figure 12. This circuit is optimized for low-voltage operation, as might be the case for a decoder in an in-ear monitoring system which will run from battery power.

The pre-emphasis network from the VCA input in Figure 12 is now in the feedback loop of OA_3; This provides de-emphasis. The VCA is set up with -12 dB of static gain to keep output signal levels low for battery operation. Because the VCA is not stable unless it sees a high frequency source impedance of 5 kΩ or less, R_5 and C_9 provide the necessary compensation to maintain stability.

OA_1 is used to implement another 20 kHz Butterworth low-pass filter. This ensures that noise picked up in the transmission channel will not cause mistracking between the detectors in the encoder and decoder. The output of this filter feeds the RMS detector input, which in turn has the same pre-emphasis network as in the encoder RMS detector.

Using the same log based mathematics described earlier, the expansion ratio of a feedforward expander can be shown to be

E.R. = 1 + A

OA_2 is configured as a gain-of-one follower. This reverses the polarity of the control signal relative to the encoder, and makes this circuit a 2:1 expander.

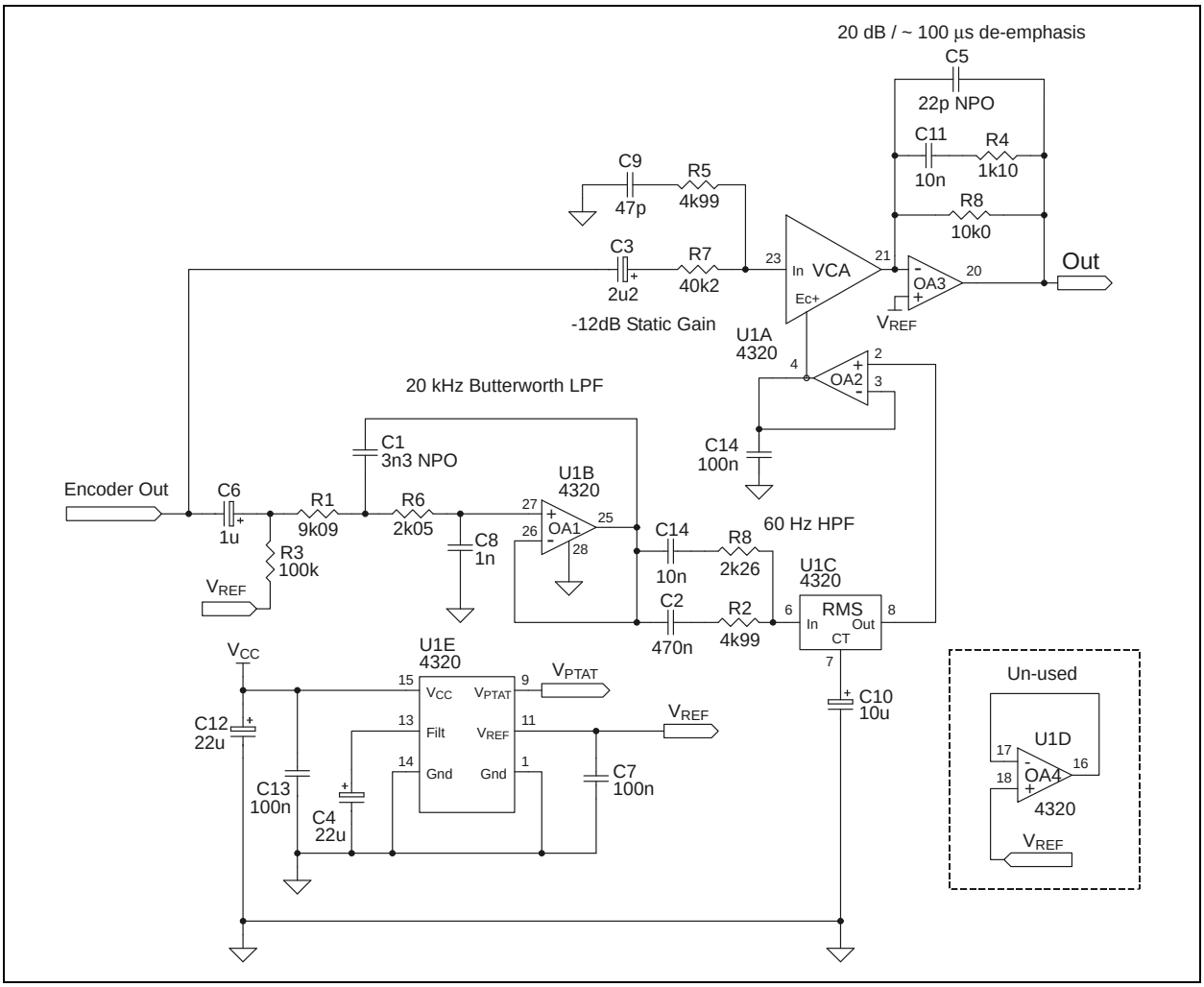


Figure 13. THAT4320 2:1 Decoder Circuit (QSOP-28 pin assignments shown)

General Dynamics Processor Configurations

The same distinguishing features that make the 4320 so applicable to companding noise reduction systems also qualify it for application to dynamics processors of all types. This is even more so when the application must run from battery power. The 4320 is versatile enough to be used as the heart of a compressor, expander, noise gate, AGC, de-esser, frequency-sensitive compressor, and many other dynamics processors. It is beyond the scope of this data sheet to provide specific advice about any of these functional classes. We refer the interested reader to THAT's applications notebooks volumes 1 and 2, which contain many circuits based on THAT's other VCAs and RMS level detectors, but are largely applicable to the 4320 with only minor variations. Of course, look for more applications information aimed specifically at the 4320 in the future.

Where to go from here

The design of compander systems and dynamics processors is a very intricate art: witness the proliferation of first analog, then digital companding systems, and the many different dynamics processors available in the market today. In the applications section of this data sheet, we offer a single example of a compander as a starting point only. THAT Corporation's applications engineering department is ready to assist customers with suggestions for tailoring and extending these basic circuits to meet specific needs.

Ordering Information

Package	Order Number
28 pin QSOP	4320Q28-U
24 pin QFN (5x5)	4320N24-U

Table 1. Ordering information

For sales:
Tel: +1 (508) 634-9922
Fax: +1 (508)634-6698
E-mail: sales@thatcorp.com

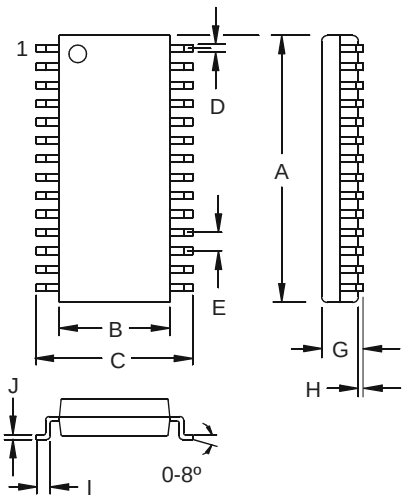
Revision History

Revision	ECO	Date	Changes	Page
05	2258	04/06/09	Fixed errors in specification table and Figure 4.	—
06	2377	02/23/10	Added QFN-24 package. Corrected equation.	—
07	2856	03/18/14	Clarified the minimum gain for stability of OA1	3, 4, 9
08	2933	07/22/15	Corrected Package Characteristics table and Figure 11.	5, 7

Package Information

Pin Name	Pin Number
GND	1
OA2 +IN	2
OA2 -IN	3
OA2 OUT	4
No Connection	5
RMS IN	6
CAP	7
RMS OUT	8
V_{PTAT}	9
No Connection	10
V_{REF}	11
No Connection	12
FILTER	13
GND	14
V_{CC}	15
OA4 OUT	16
OA4 -IN	17
OA4 +IN	18
No Connection	19
OA3 OUT	20
VCA OUT	21
No Connection	22
VCA IN	23
No Connection	24
OA1 OUT	25
OA1 -IN	26
OA1 +IN	27
OA1 V_{EE}	28

Table 2. QSOP-28 pin assignments



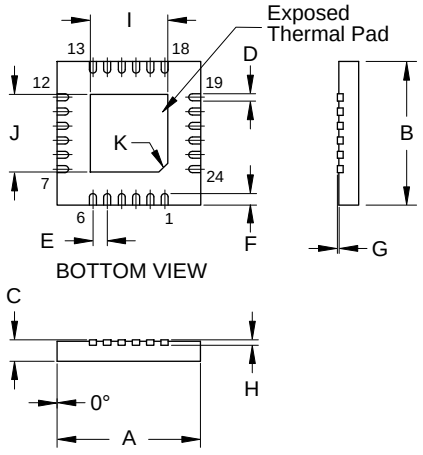
ITEM	MILLIMETERS	INCHES
A	9.80 - 9.98	0.386 - 0.393
B	3.81 - 3.99	0.150 - 0.157
C	5.79 - 6.20	0.228 - 0.244
D	0.20 - 0.30	0.008 - 0.012
E	0.635 BSC	0.025 BSC
G	1.35 - 1.75	0.0532 - 0.0688
H	0.10 - 0.25	0.004 - 0.010
I	0.40 - 1.27	0.016 - 0.050
J	0.19 - 0.25	0.0075 - 0.0098

Figure 14. QSOP-28 package drawing

Pin Name	Pin Number
OA1 -IN	1
OA1 +IN	2
OA1 V_{EE}	3
GND	4
OA2 +IN	5
OA2 -IN	6
OA2 OUT	7
No Connection	8
RMS IN	9
CAP	10
RMS OUT	11
V_{PTAT}	12
V_{REF}	13
FILTER	14
GND	15
V_{CC}	16
OA4 OUT	17
OA4 -IN	18
OA4 +IN	19
No Connection	20
OA3 OUT	21
VCA OUT	22
VCA IN	23
OA1 OUT	24
GND*	THERMAL PAD (25)

Table 3. QFN-24 (5x5) pin assignments

* For best VCA THD performance the QFN's thermal pad should not be soldered to the PCB.



ITEM	MILLIMETERS	INCHES
A	5.00 ± 0.10	0.197 ± 0.004
B	5.00 ± 0.10	0.197 ± 0.004
C	0.90 ± 0.05	0.035 ± 0.002
D	0.25 ± 0.05	0.010 ± 0.002
E	0.65 ± 0.05	0.026 ± 0.002
F	0.40 ± 0.05	0.016 ± 0.002
G	0.00 ~ 0.05	0.000 ~ 0.020
H	0.20 ± 0.05	0.008 ± 0.002
I	3.40 ± 0.05	0.134 ± 0.002
J	3.40 ± 0.05	0.134 ± 0.002
K	C' 0.4 x 45°	C' 0.016 x 45°

Figure 15. QFN-24 (5x5) package drawing

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