Automotive MOSFET

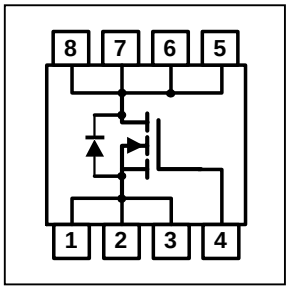
## OptiMOS™ 7 Power-Transistor

RoHS | Infineon Automotive Quality | AEC Qualified

PG-TDSON-8-43


## Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested




## Potential applications

General automotive applications.

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.

## Product Summary

| | | |
|---|---|---|
| $V_{DS}$ | 40 | V |
| $R_{DS(on)}$ | 0.52 | mΩ |
| $I_D$ (chip limited) | 430 | A |

| Type | Package | Marking |
|---|---|---|
| IAUCN04S7L005 | PG-TDSON-8-43 | 7N04L005 |

## Table of Contents

## Maximum ratings

at Tj=25 °C, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Continuous drain current | $I_D$ | $V_{GS}$=10 V, Chip limitation[1,2)] | 430 | A |
| | | $V_{GS}$=10V, DC current | 175 | |
| | | $T_a$=100 °C, $V_{GS}$=10 V, $R_{thJA}$ on 2s2p[2,3)] | 54 | |
| Pulsed drain current[2)] | $I_{D,pulse}$ | $T_C$=25 °C, $t_p$= 100 µs | 1410 | |
| Avalanche energy, single pulse[2)] | $E_{AS}$ | $I_D$=88 A | 285 | mJ |
| Avalanche current, single pulse | $I_{AS}$ | – | 175 | A |
| Gate source voltage | $V_{GS}$ | – | ±16 | V |
| | | limited to duty factor of 1% | +20 | V |
| Power dissipation | $P_{tot}$ | $T_C$=25 °C | 179 | W |
| Operating and storage temperature | $T_j$, $T_{stg}$ | – | -55 ... +175 | °C |

## Thermal characteristics[2)]

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| Thermal resistance, junction - case | $R_{thJC}$ | – | – | 0.42 | 0.84 | K/W |
| Thermal resistance, junction - ambient[3)] | $R_{thJA}$ | – | – | 26 | – | |

## Electrical characteristics

at Tj=25 °C, unless otherwise specified

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Static characteristics** | | | | | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}$=0 V, $I_D$=1 mA | 40 | – | – | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=95 µA | 1.2 | 1.5 | 1.8 | |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$=40 V, $V_{GS}$=0 V, $T_j$=25 °C | – | – | 1 | µA |
| | | $V_{DS}$=40 V, $V_{GS}$=0 V, $T_j$=100 °C[2)] | – | – | 24 | |
| Gate-source leakage current | $I_{GSS}$ | $V_{GS}$=16 V, $V_{DS}$=0 V | – | – | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$=4.5 V, $I_D$=88 A | – | 0.64 | 0.75 | mΩ |
| | | $V_{GS}$=10 V, $I_D$=88 A | – | 0.46 | 0.52 | |
| Gate resistance[2)] | $R_G$ | – | – | 1.1 | – | Ω |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Dynamic characteristics**[2] | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$=0 V, $V_{DS}$=20 V, $f$=1 MHz | – | 7242 | 9415 | pF |
| Output capacitance | $C_{oss}$ | | – | 3639 | 4730 | |
| Reverse transfer capacitance | $C_{rss}$ | | – | 121 | 181 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=20 V, $V_{GS}$=10 V, $I_D$=88 A, $R_G$=3.5 Ω | – | 8 | – | ns |
| Rise time | $t_r$ | | – | 8 | – | |
| Turn-off delay time | $t_{d(off)}$ | | – | 67 | – | |
| Fall time | $t_f$ | | – | 33 | – | |
| **Gate Charge Characteristics**[2] | | | | | | |
| Gate to source charge | $Q_{gs}$ | $V_{DD}$=20 V, $I_D$=88 A, $V_{GS}$=0 to 10 V | – | 18 | 24 | nC |
| Gate to drain charge | $Q_{gd}$ | | – | 19 | 28 | |
| Gate charge total | $Q_g$ | | – | 109 | 141 | |
| Gate plateau voltage | $V_{plateau}$ | | – | 2.5 | – | V |
| **Reverse Diode** | | | | | | |
| Diode continous forward current[2] | $I_S$ | $T_C$=25 °C | – | – | 175 | A |
| Diode pulse current[2] | $I_{S,pulse}$ | $T_C$=25 °C, $t_p$= 100 µs | – | – | 1410 | |
| Diode forward voltage | $V_{SD}$ | $V_{GS}$=0 V, $I_F$=88 A, $T_j$=25 °C | – | 0.8 | 0.95 | V |
| Reverse recovery time[2] | $t_{rr}$ | $V_R$=20 V, $I_F$=50A, $di_F/dt$ =100 A/µs | – | 52 | 78 | ns |
| Reverse recovery charge[2] | $Q_{rr}$ | | – | 54 | 107 | nC |

[1] Practically the current is limited by the overall system design including the customer-specific PCB.

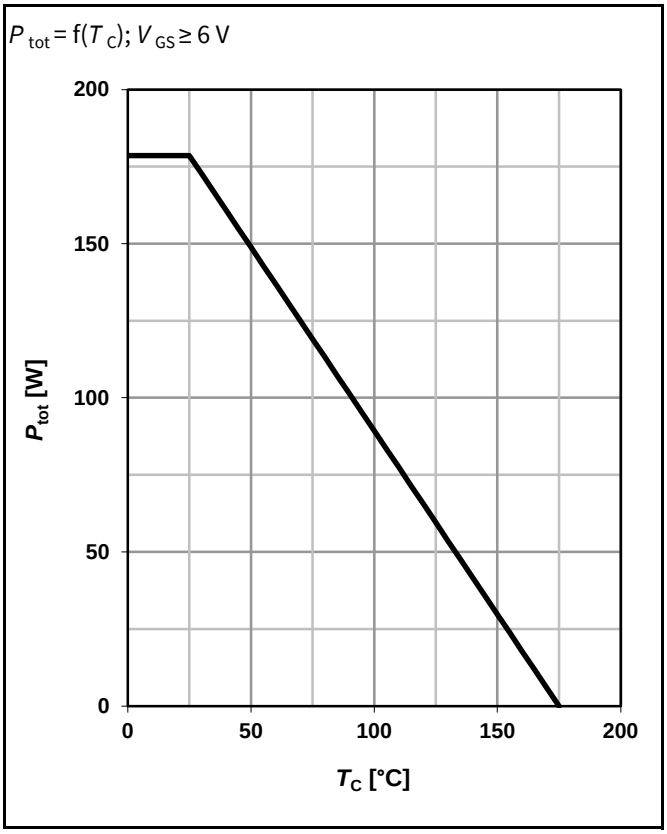
[2] The parameter is not subject to production testing – specified by design.

[3] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

## Electrical characteristics diagrams

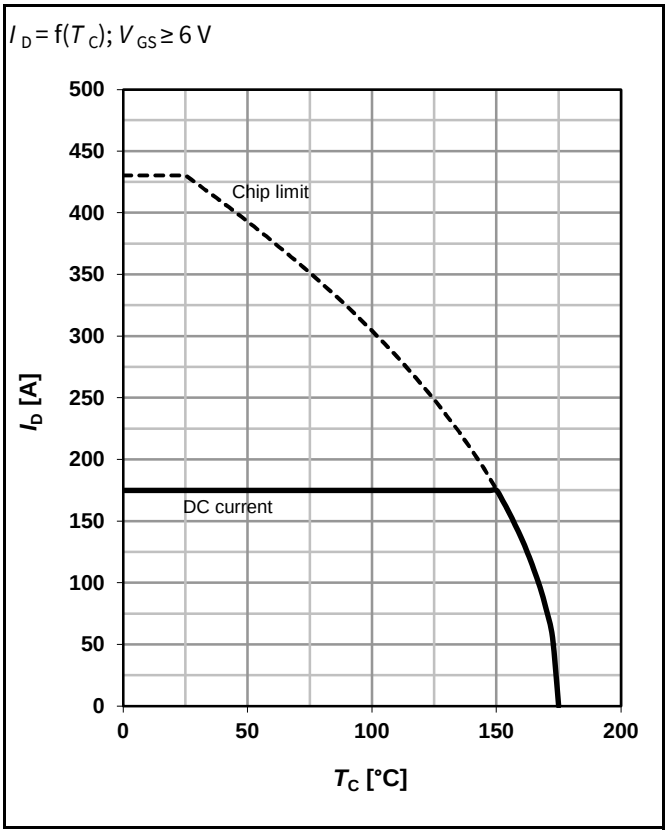
### 1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



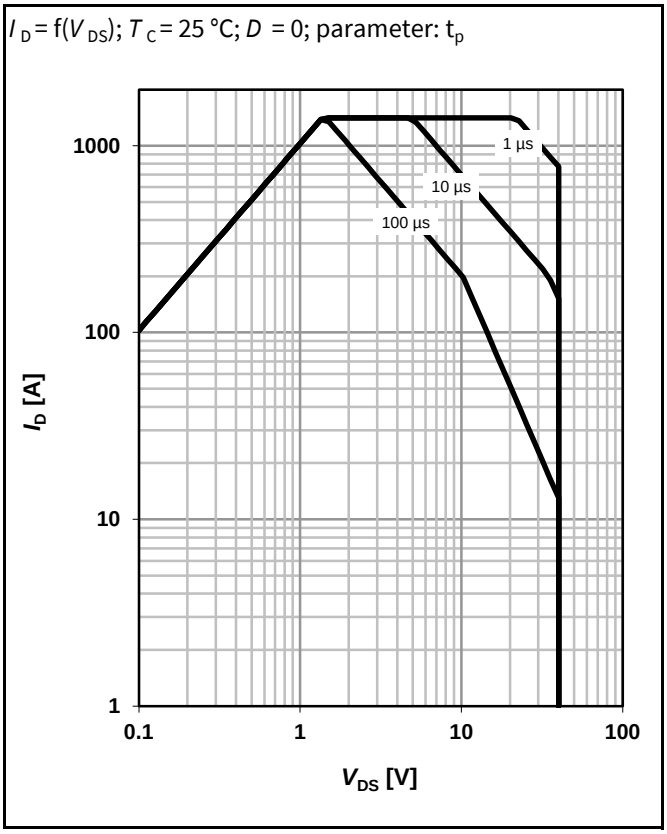

### 2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6$ V



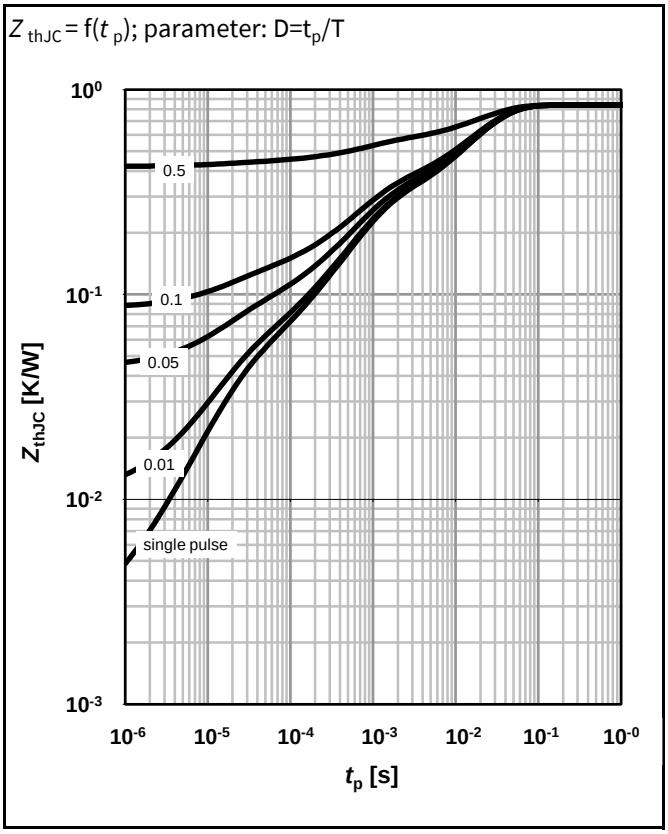

### 3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: $t_p$



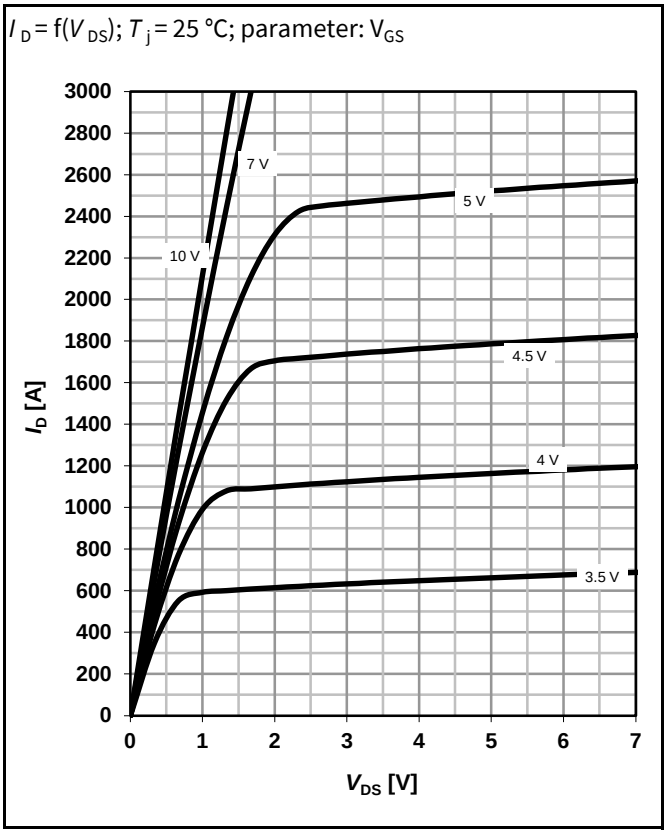

### 4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$; parameter: $D=t_p/T$



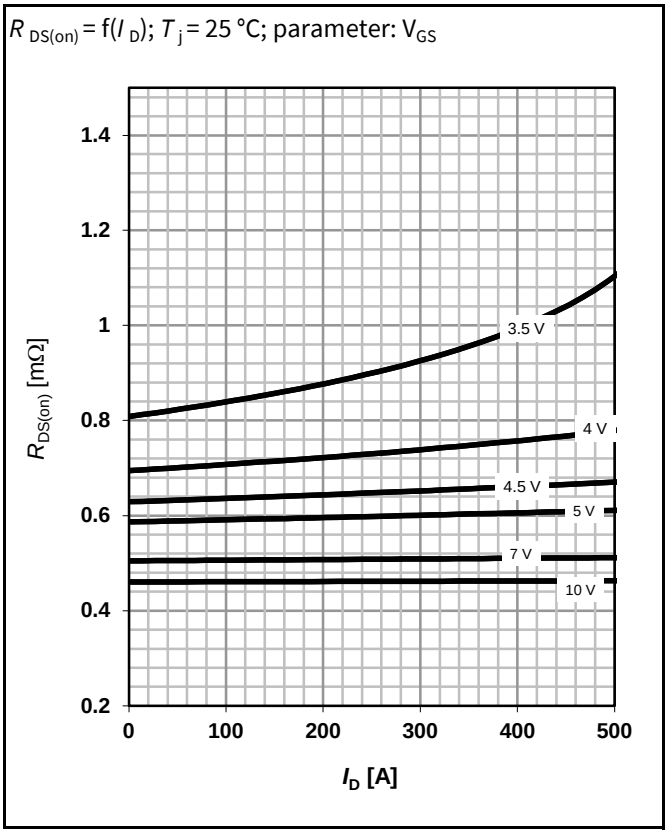
### 5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: $V_{GS}$



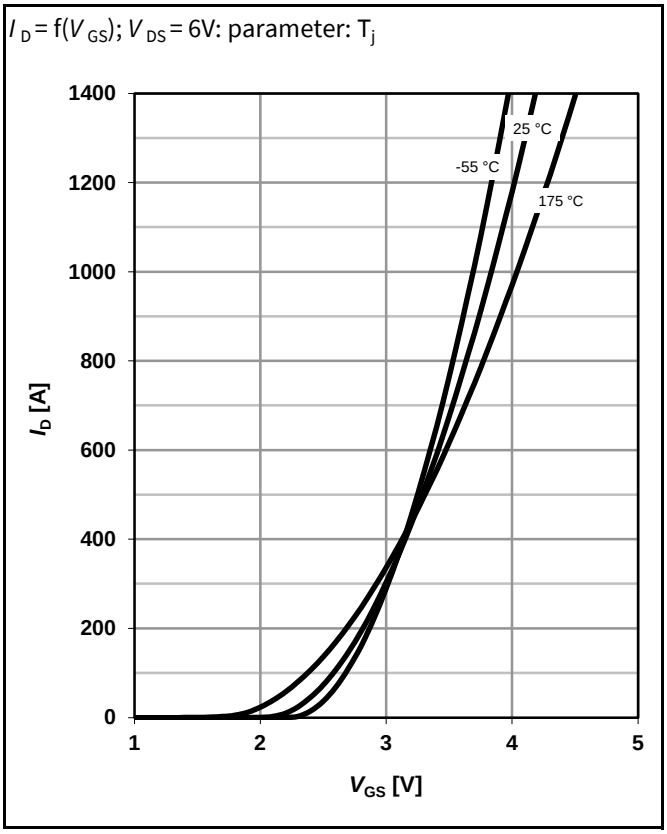

### 6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: $V_{GS}$



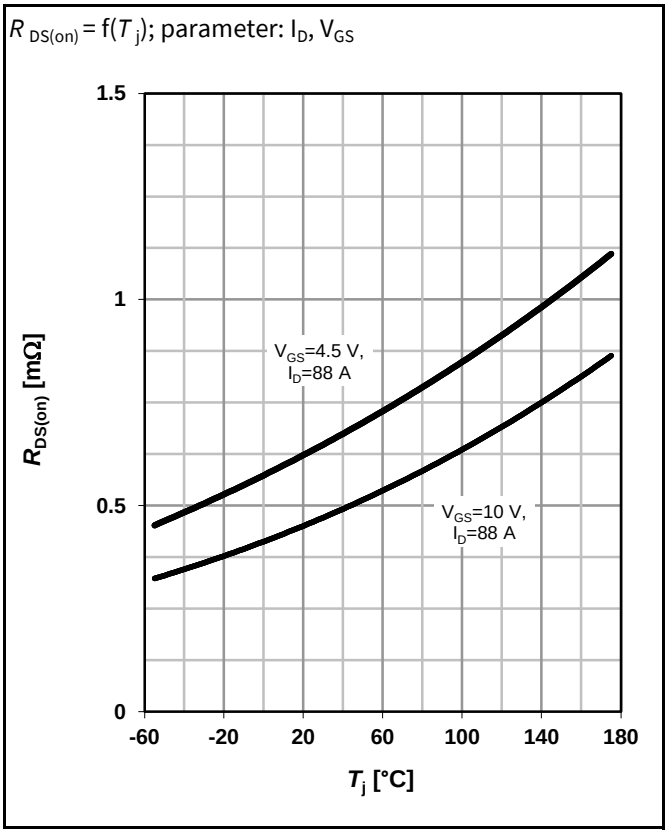

### 7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$V: parameter: $T_j$



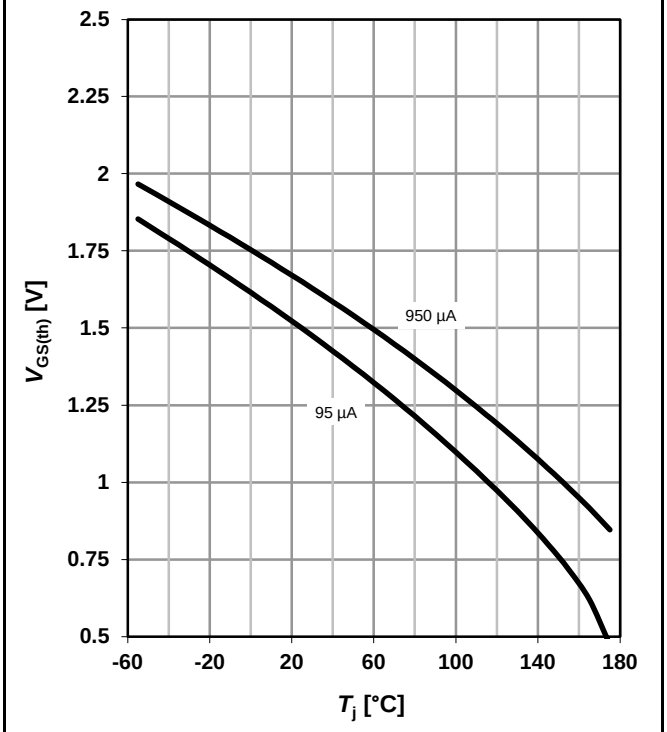

### 8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; parameter: $I_D$, $V_{GS}$



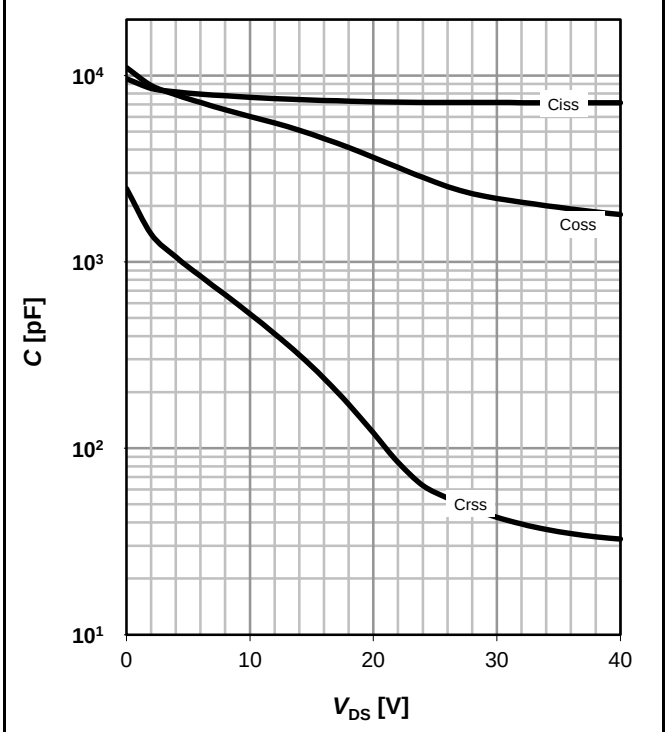
### 9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: $I_D$



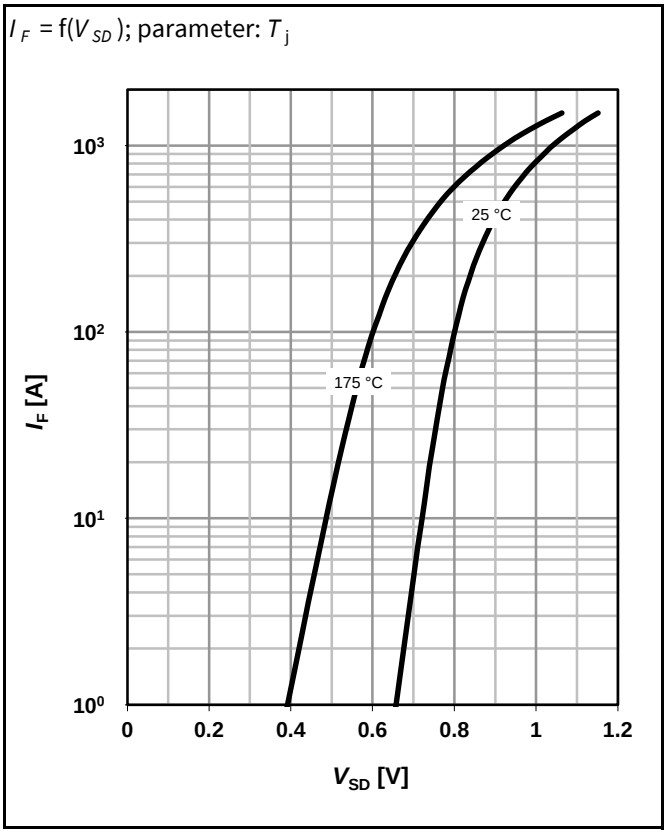

### 10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



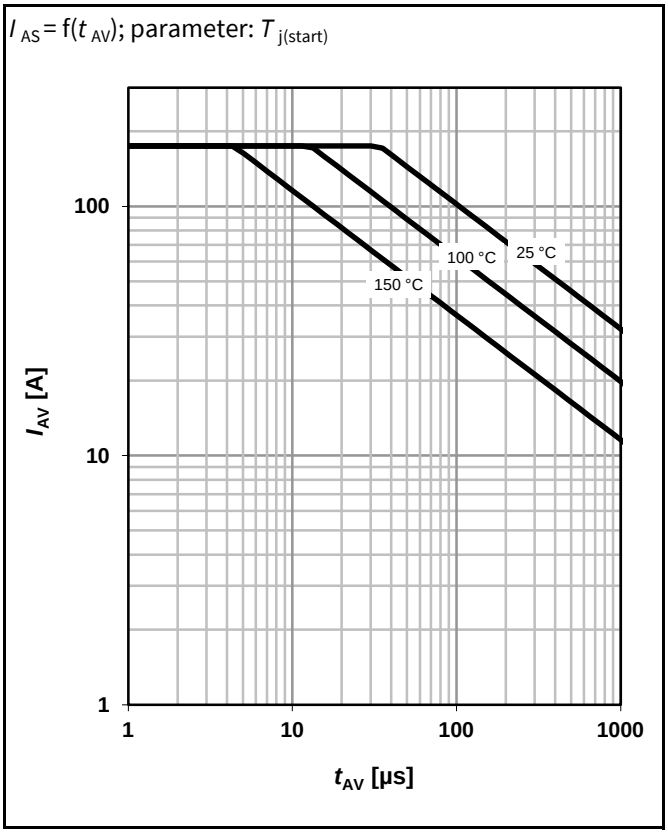

### 11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: $T_j$



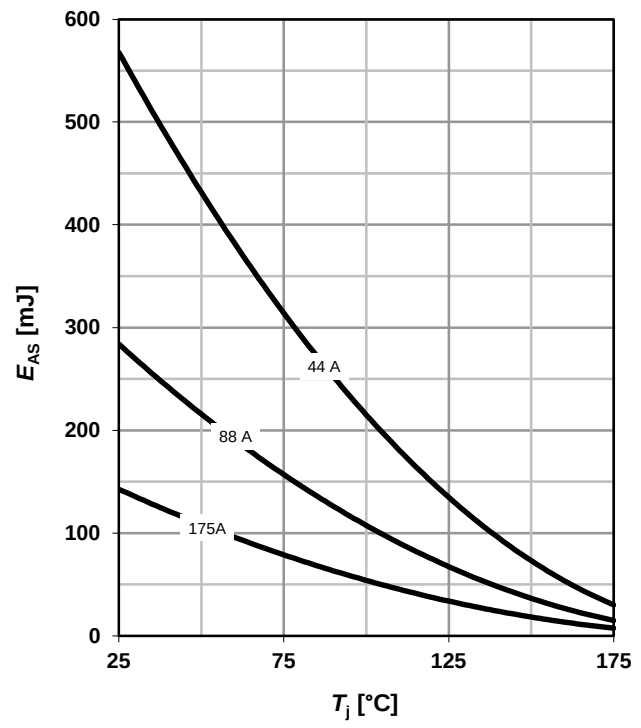

### 12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



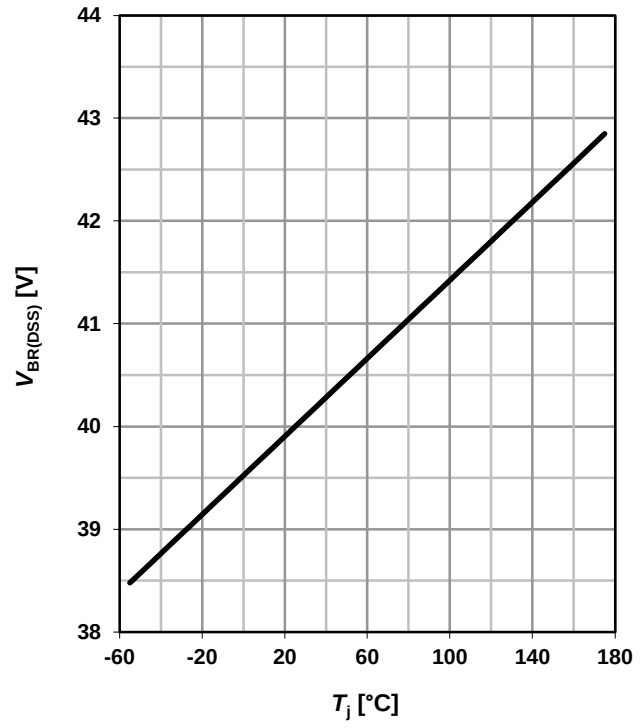
### 13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: ID



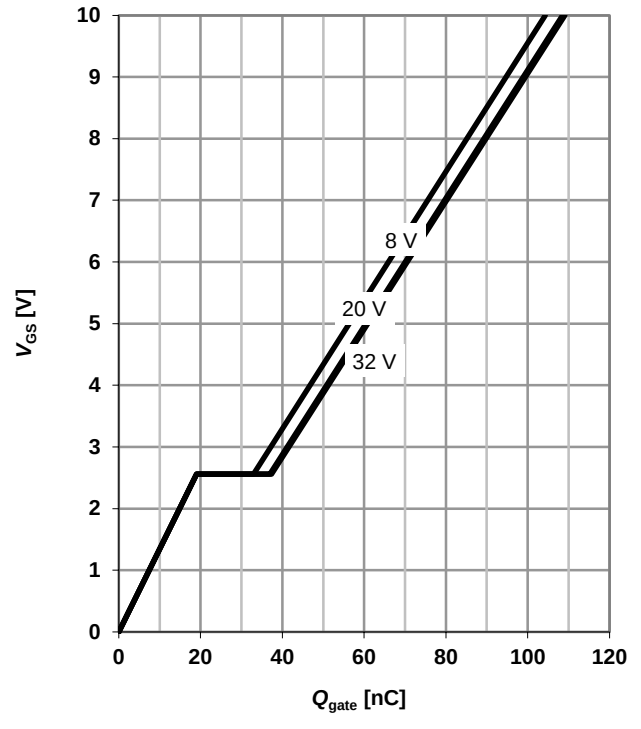

### 14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$; $I_{D\_typ}$ = 1 mA

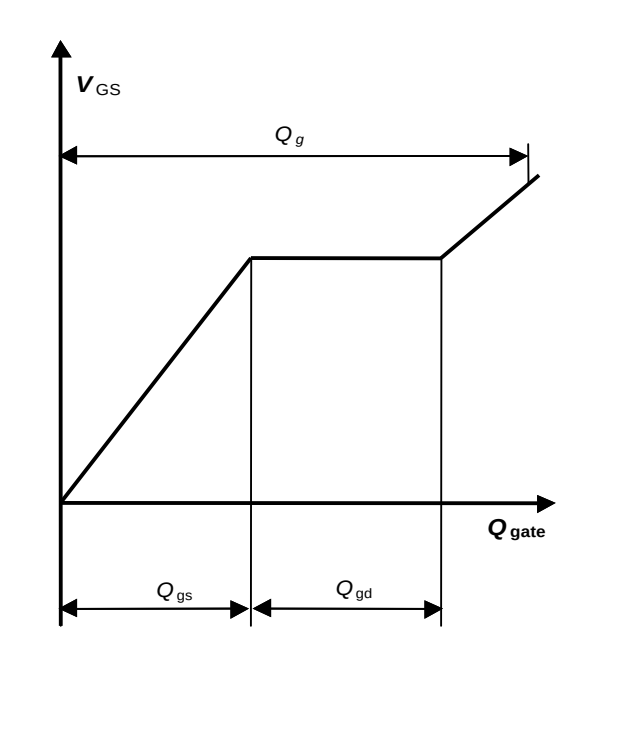



### 15 Typ. gate charge

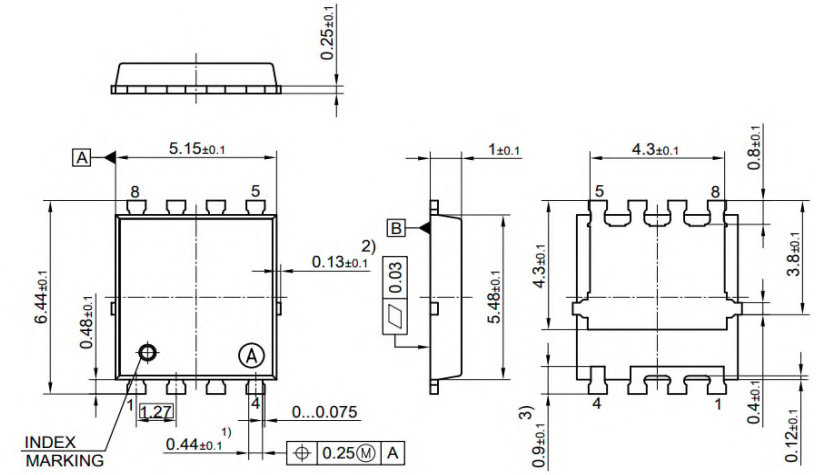
$V_{GS} = f(Q_{gate})$; $I_D$ = 88 A pulsed; parameter: $V_{DD}$




### 16 Gate charge waveforms



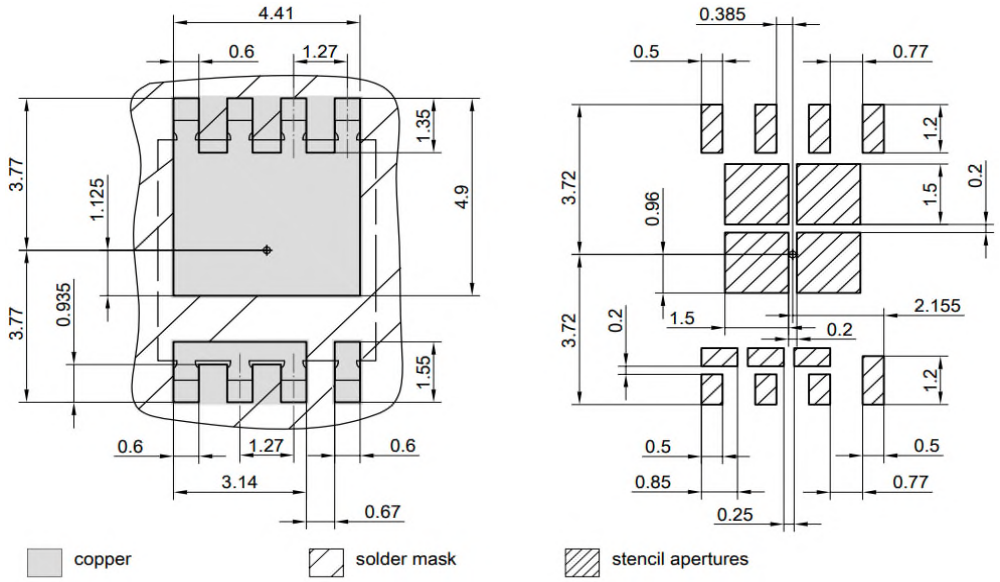
## Package Outline




1) EXCLUDE MOLD FLASH
2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
3) LEAD LENGTH UP TO ANTI FLASH LINE
4)ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]

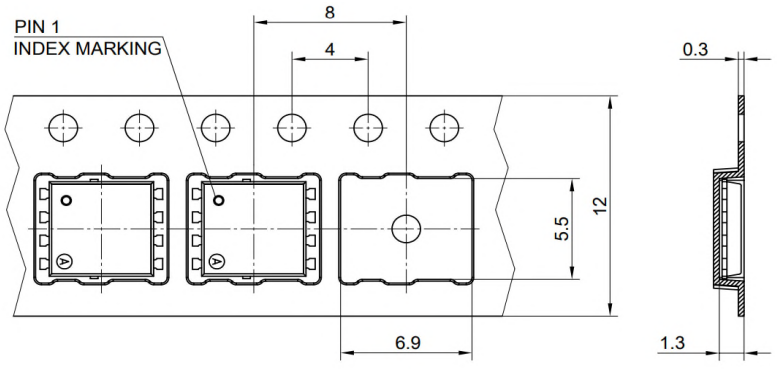
All dimensions are in units mm

## Footprint




All dimensions are in units mm

## Packaging




All dimensions are in units mm

## Revision History

| Revision | Date | Changes |
|---|---|---|
| Revision 1.0 | 15.11.2023 | Final Data Sheet |
| | | |
| | | |

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**Edition 2023-11-15**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**



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**Document reference**
**IAUCN04S7L005-Data-Sheet-10-Infineon**

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