

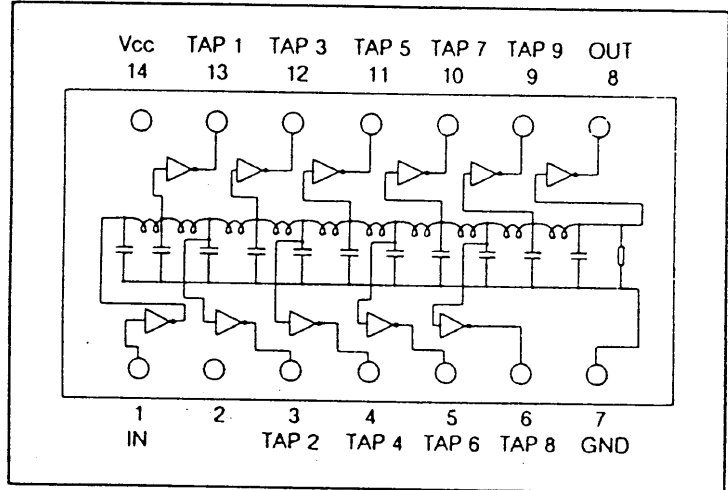
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DIGITAL DELAY MODULES 50A, 52A, 52S Series  
10 Tap 14 Pin Moulded DIP

- Schottky TTL compatible
- 10 equally spaced taps
- 14 pin package
- Low profile
- TTL compatible
- Auto insert or surface mount package styles

DUAL - IN - LINE PACKAGE (TOP VIEW)



**description**

The 50A series of Digital Delay Modules are Schottky TTL buffered delay lines providing precise delay times and direct compatibility with TTL. Ten equally spaced fixed delay taps are packaged in a low profile 14 pin dual-in-line configuration. Internal termination of the delay line and compensation for propagation delays and thermal drift are incorporated in the design so that no additional external components are required. These modules are particularly suitable for high density board designs.

The 52A series is the auto insertable version.

The 52S series is the surface mount version which may be vapour phased at temperatures below 218C for durations of up to 2 minutes.

**absolute maximum ratings over operating free-air temperature range**

Supply voltage $V_{cc}$ . . . . .	.7V
Input voltage . . . . .	.5.5V
Min. pulse width as % of total delay . . . . .	.40%
Input pulse repetition rate PRR . . . . .	3 x pulse width min.
Operating free-air temperature range . . . . .	.0C to 70C
Storage temperature range . . . . .	-.55C to 125C
Temperature coefficient of delay . . . . .	$\pm 500$ ppm/C
Lead temperature 1.5mm from case for 10 seconds . . . . .	300C

**drive capabilities**

Logic 0 output . . . . .	10 TTL loads per tap max. 20 TTL loads per unit max.
Logic 1 output . . . . .	20 TTL loads per unit max.

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**electrical specifications over operating free-air temperature range**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IH</sub> High-level input voltage		2			V
V <sub>IL</sub> Low-level input voltage				0.8	V
V <sub>OH</sub> High-level output voltage	V <sub>IH</sub> = 2V, I <sub>OH</sub> = -1mA V <sub>CC</sub> = 4.75V	2.7	3.4		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = 4.75V I <sub>OL</sub> = 20mA, V <sub>IL</sub> = 0.8V			0.5	V
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = 5.25V, V <sub>IH</sub> = 2.7V			50	μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = 5.25V, V <sub>IL</sub> = 0.5V			-2	mA
I <sub>CC</sub> Supply current outputs high	V <sub>CC</sub> = 5.25V			48	mA
I <sub>CC</sub> Supply current outputs low	V <sub>CC</sub> = 5.25V			108	mA

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**delay characteristics  $V_{cc} = 5V$ ,  $T_a = 25C$ , no load at taps, input pulse width 100% of total delay, input rise time 3ns.**

delay tolerance from input to tap  $\pm 2ns$  or  $\pm 5%$  whichever is greater

**50A SERIES 10 Tap 14 Pin DIP**  
**Package style I**

<b>PART No.</b> <b>(1)</b>	<b>TOTAL DELAY</b> <b>(ns)</b> <b><math>\pm 5\%</math></b>	<b>TAP TO TAP DELAY</b> <b>(ns)</b>	<b>OUTPUT RISE TIME</b> <b>(ns)</b>
50A - 10250	25	$2.5 \pm 2$	3
50A - 10500	50	$5 \pm 2$	3
50A - 10750	75	$7.5 \pm 2$	3
50A - 10101	100	$10 \pm 2$	3
50A - 10151	150	$15 \pm 2$	3
50A - 10201	200	$20 \pm 2$	4
50A - 10251	250	$25 \pm 3$	4
50A - 10301	300	$30 \pm 3$	4
50A - 10351	350	$35 \pm 4$	4
50A - 10401	400	$40 \pm 4$	4
50A - 10451	450	$45 \pm 5$	4
50A - 10501	500	$50 \pm 5$	4

Note: Delays measured at 1.5V on leading edge, Rise Time measured from 0.75V to 2.4V  
(1) Auto insert part No. starts with 52A package style C. Surface mount part No. starts with 52S package style D