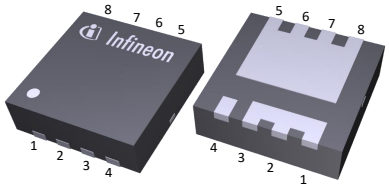
MOSFET

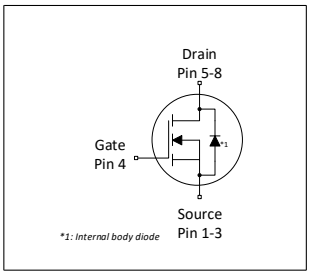
OptiMOS™ 6 Power-Transistor, 200 V

PG-TSDSON-8 FL



Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low reverse recovery charge (Q_{rr})
- High avalanche energy rating
- 175°C operating temperature
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020
- 100% avalanche tested



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	200	V
$R_{DS(on),max}$	52	mΩ
I_D	26	A
Q_{oss}	29	nC
Q_G	9.9	nC
Q_{rr} (1000A/µs)	143	nC

Type / Ordering Code	Package	Marking	Related Links
ISZ520N20NM6	PG-TSDSON-8 FL	520N20N	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - -	- - - -	26 18.7 19.5 4.5	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=15 V, T_C=100 °C V_{GS}=10 V, T_A=25°C,R_{thJA}=60°C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	104	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	62	mJ	I_D=9 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	88 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=60 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	1.05	1.7	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area[2]	R_{thJA}	-	-	60	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3.0	3.7	4.5	V	V_{DS}=V_{GS}, I_D=31 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=160 V, V_{GS}=0 V, T_j=25 °C V_{DS}=160 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	44.1 38.2	52.0 47.8	mΩ	V_{GS}=10 V, I_D=15 A V_{GS}=15 V, I_D=15 A
Gate resistance	R_G	-	4.2	-	Ω	-
Transconductance[1]	g_{fs}	4.3	8.7	-	S	|V_{DS}|≥2|I_D|$R_{DS(on)max}$, I_D=15 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	740	960	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	120	160	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	10	17	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5.7	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=7.5 A, $R_{G,ext}$=3 Ω
Rise time	t_r	-	3.8	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=7.5 A, $R_{G,ext}$=3 Ω
Turn-off delay time	$t_{d(off)}$	-	6.6	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=7.5 A, $R_{G,ext}$=3 Ω
Fall time	t_f	-	9.2	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=7.5 A, $R_{G,ext}$=3 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5.1	-	nC	V_{DD}=100 V, I_D=7.5 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	2.7	-	nC	V_{DD}=100 V, I_D=7.5 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	2.3	3.5	nC	V_{DD}=100 V, I_D=7.5 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	4.6	-	nC	V_{DD}=100 V, I_D=7.5 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	9.9	14.9	nC	V_{DD}=100 V, I_D=7.5 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	6.8	-	V	V_{DD}=100 V, I_D=7.5 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	8	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	29	38	nC	V_{DS}=100 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition

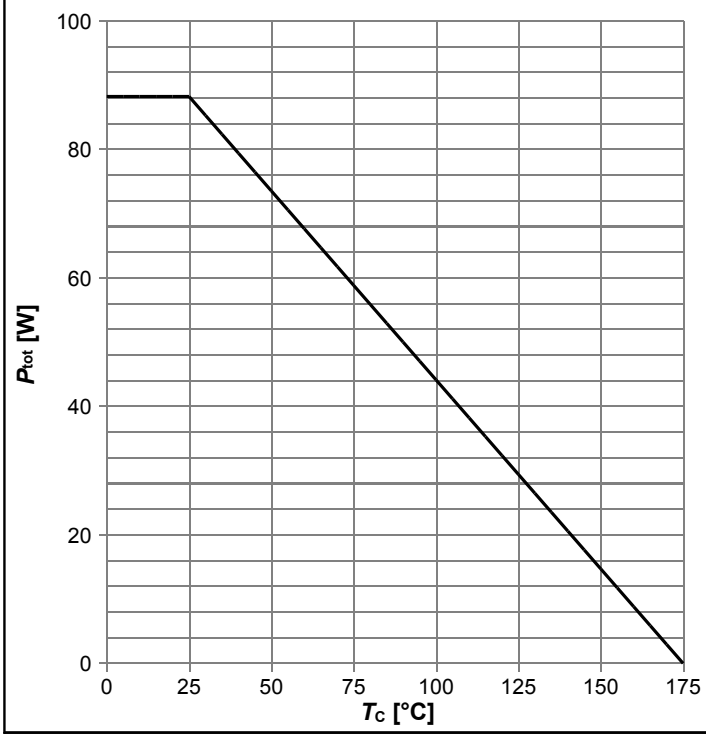
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	26	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	104	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.88	1.0	V	V_{GS}=0 V, I_F=15 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	37	-	ns	V_R=100 V, I_F=7.5 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	30	60	nC	V_R=100 V, I_F=7.5 A, di_F/dt=100 A/µs
Reverse recovery time	t_{rr}	-	18	-	ns	V_R=100 V, I_F=7.5 A, di_F/dt=1000 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	143	286	nC	V_R=100 V, I_F=7.5 A, di_F/dt=1000 A/µs

[1)] Defined by design. Not subject to production test.

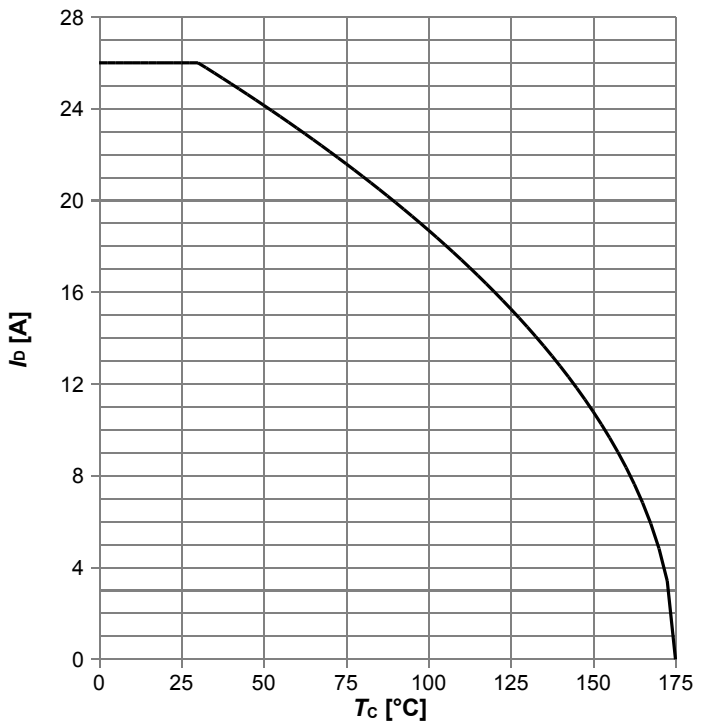
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



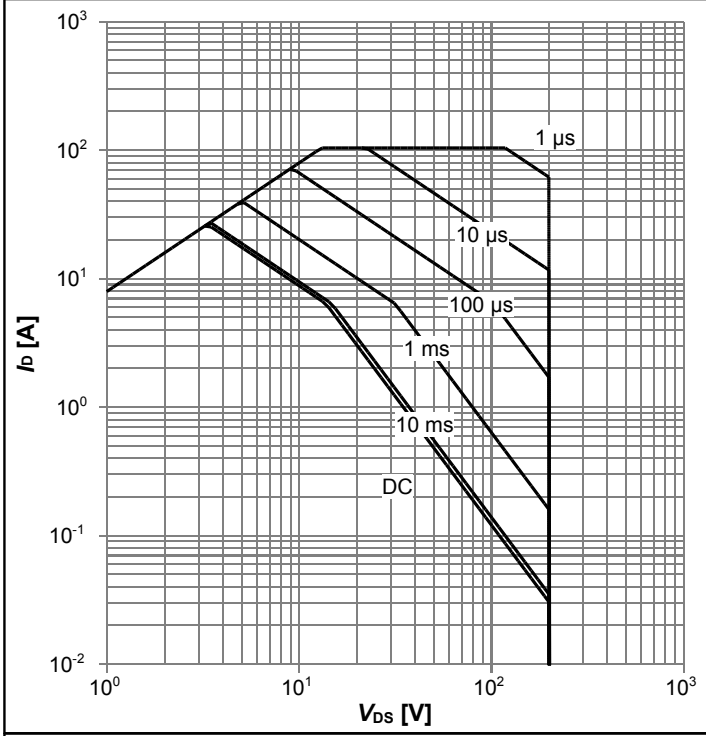
$P_{tot}=f(T_C)$

Diagram 2: Drain current



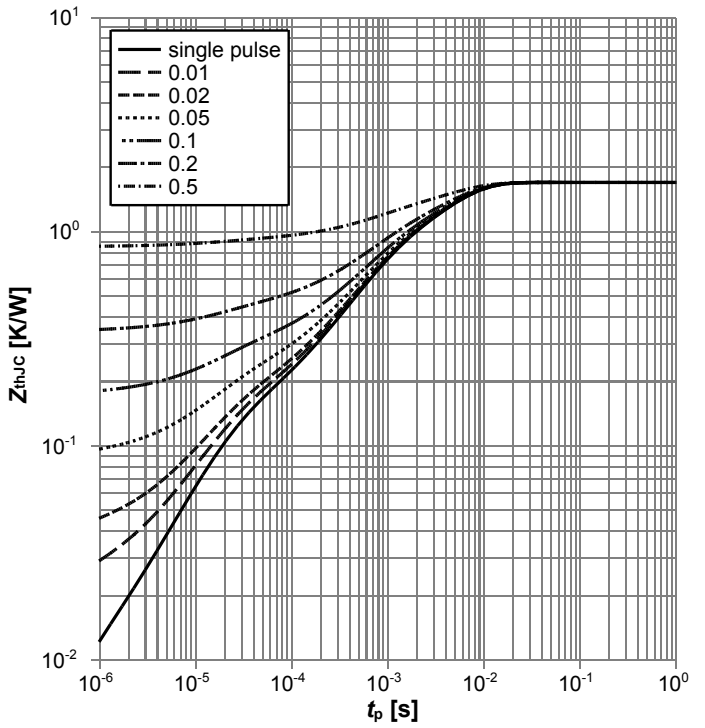
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



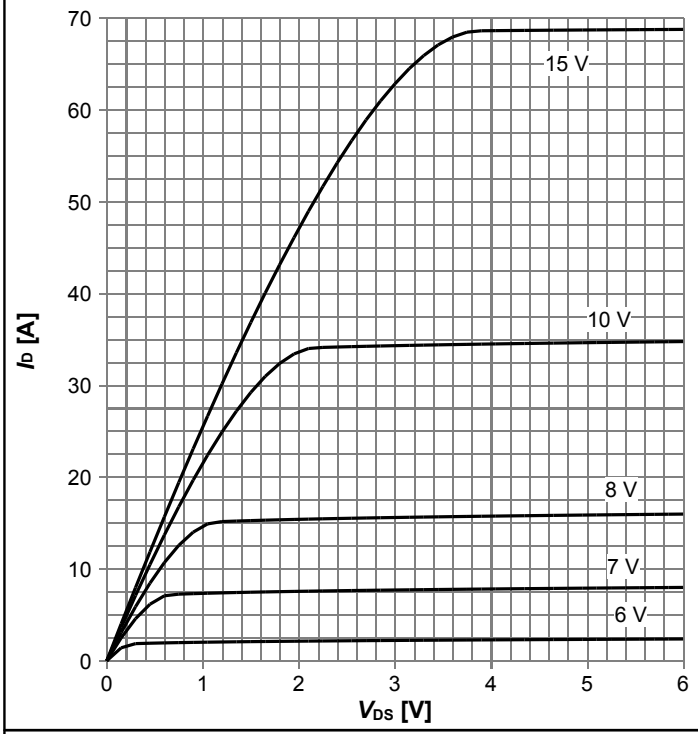
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



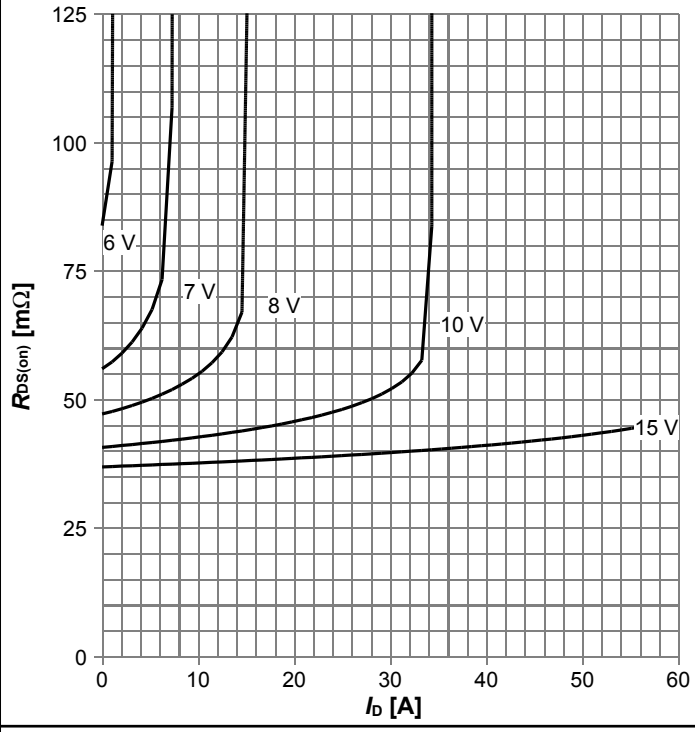
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



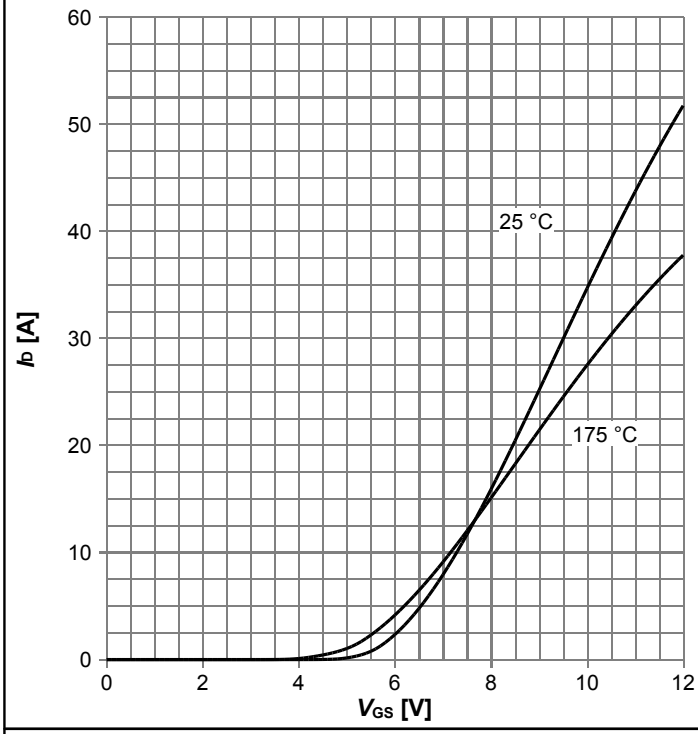
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



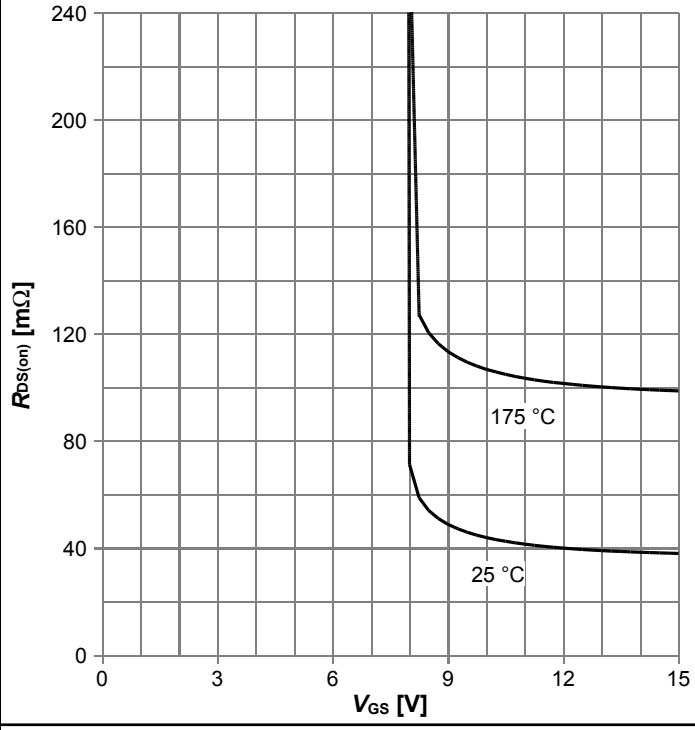
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



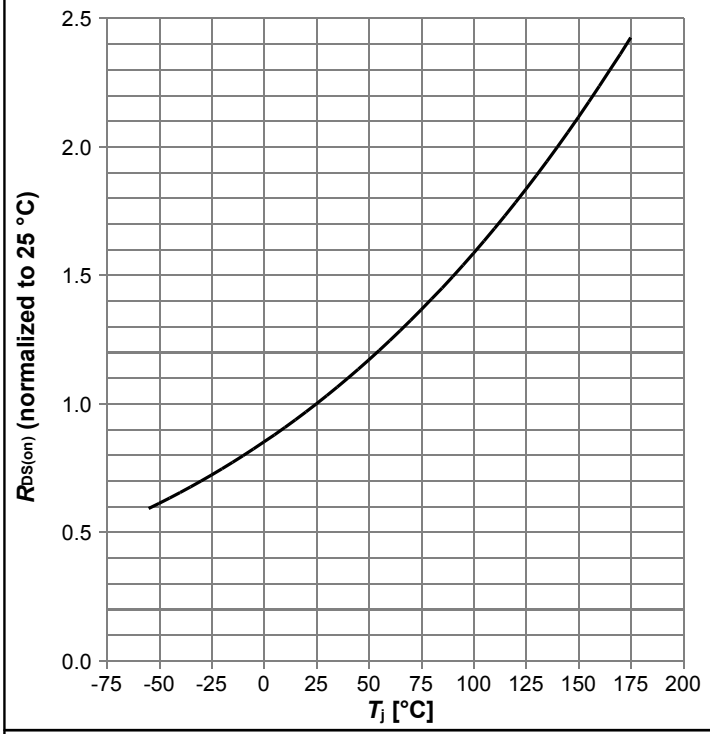
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



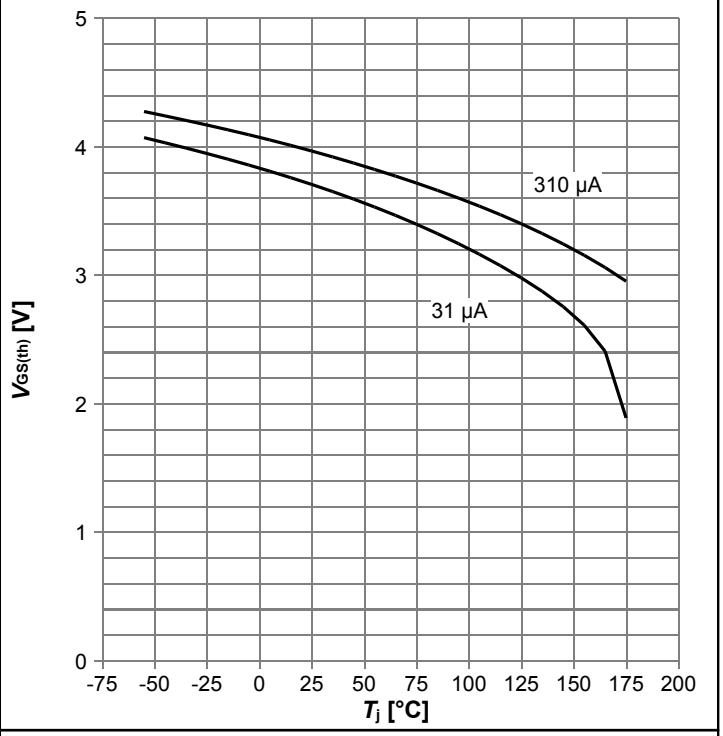
$R_{DS(on)}$=f(V_{GS}), I_D=15 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



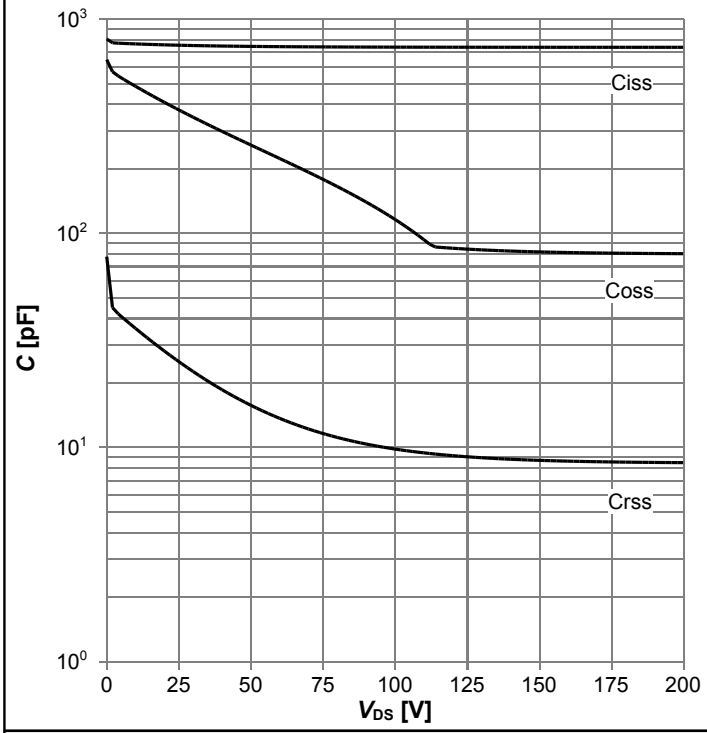
$R_{DS(on)}$=f(T_j), I_D=15 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



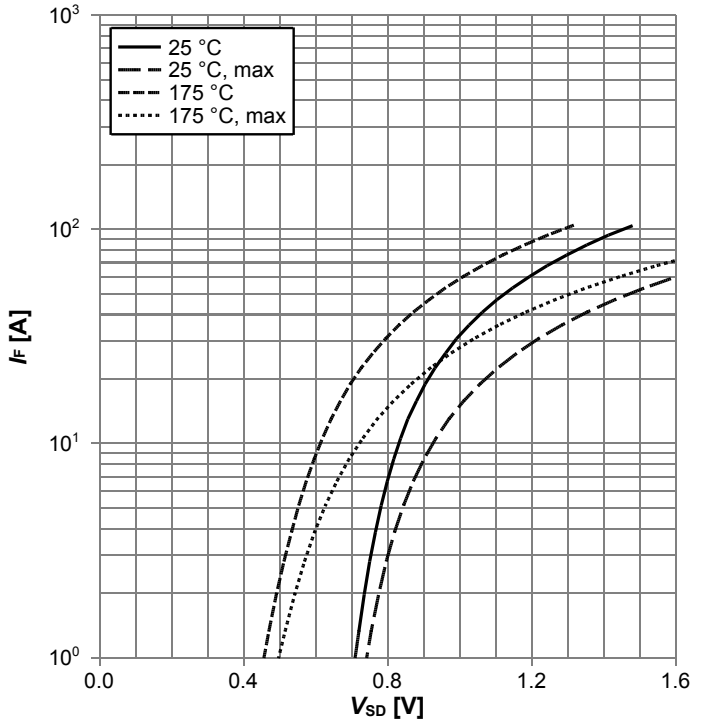
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



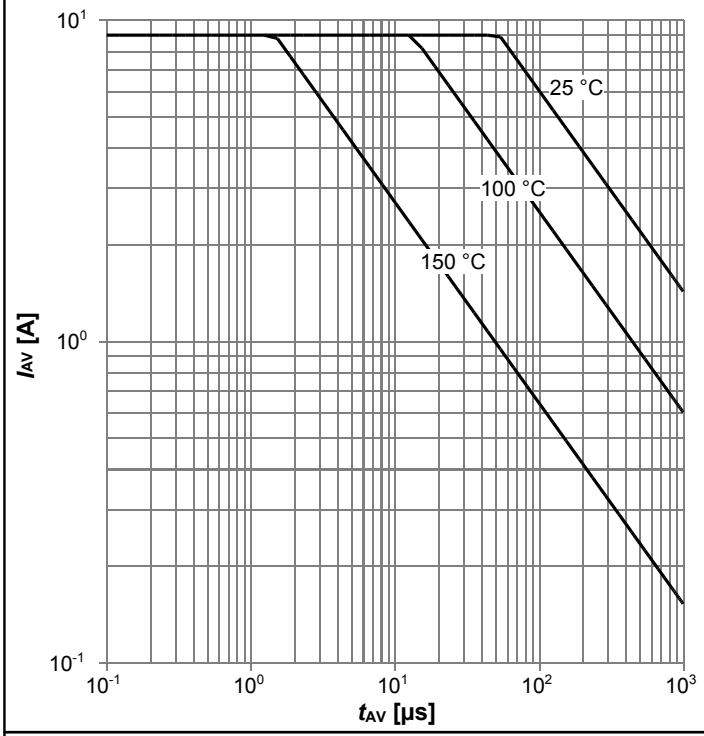
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



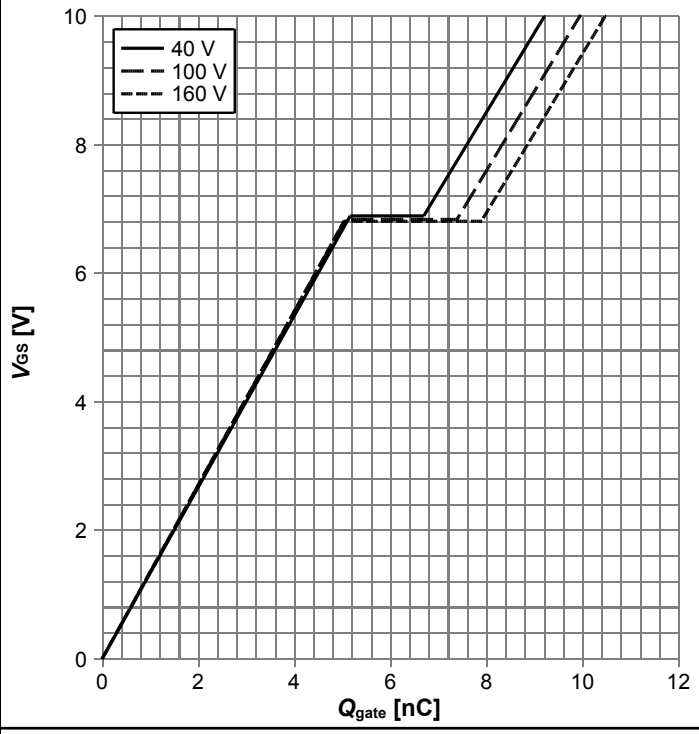
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



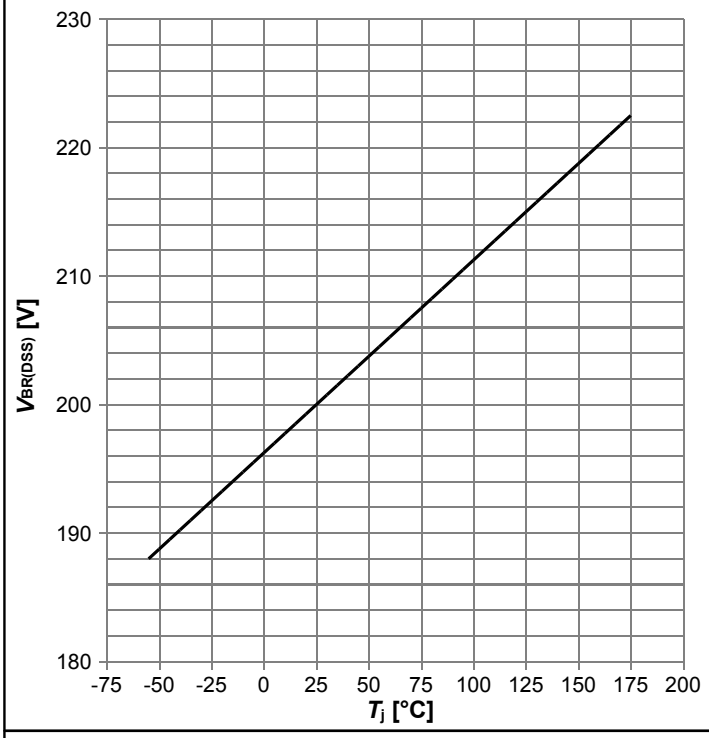
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



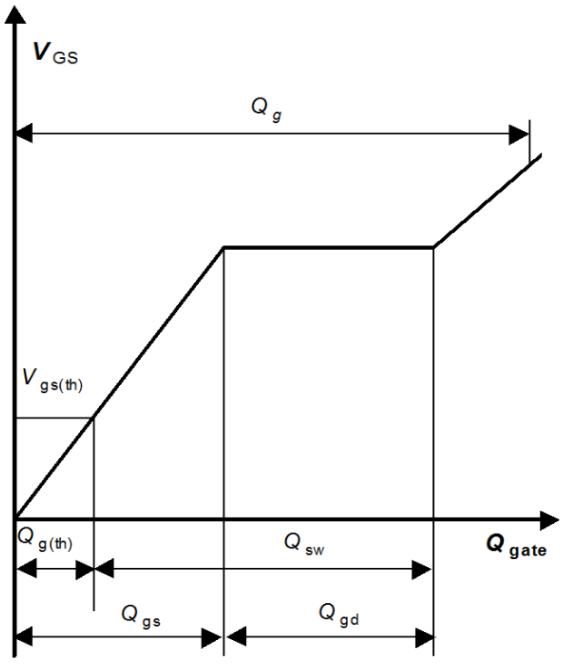
V_{GS}=f(Q_{gate}), I_D=7.5 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

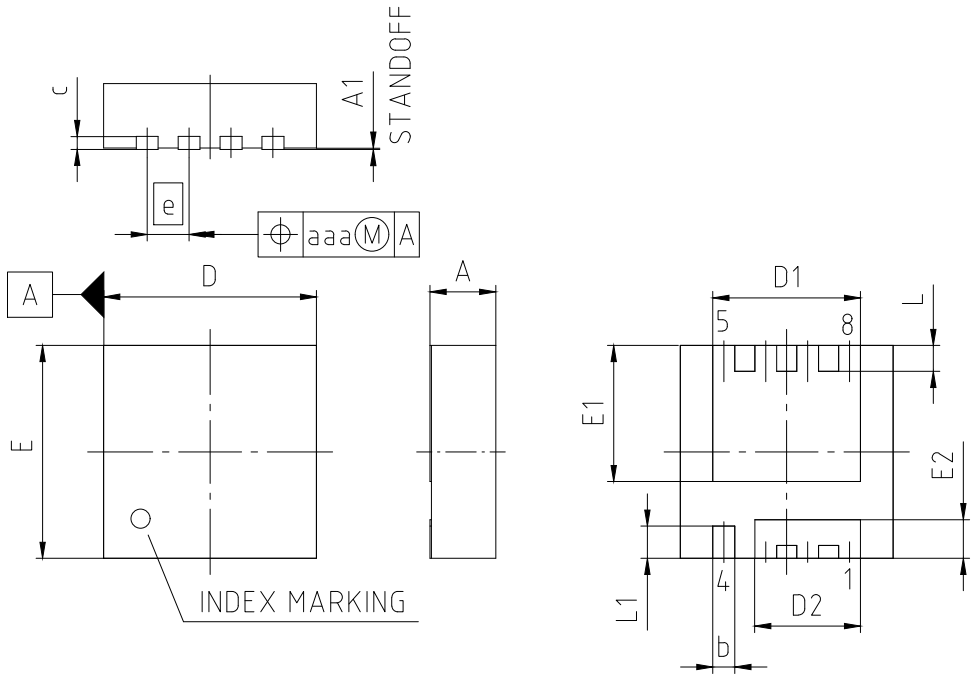


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TSDSON-8-U03	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A	0.90	1.10
A1	0	0.05
b	0.24	0.44
c	0.10	0.30
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.50	0.70
e	0.65	
L	0.30	0.50
L1	0.40	0.60
aaa	0.06	
N	8	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm

Revision History

ISZ520N20NM6

Revision: 2023-12-07, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2023-12-07	Release of final version

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