MP1653A

17V, 3A, 1.2MHz, 0.6V V_{REF}, High-Efficiency, Synchronous Step-Down Converter with Internal MOSFETS in a SOT563 Package

DESCRIPTION

The MP1653A is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs. The MP1653A offers a very compact solution that can achieve up to 3A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range, with excellent load and line regulation. Synchronous mode provides high efficiency across the entire I_{OUT} load range.

Constant-on-time (COT) control provides fast transient response, easy loop design, and tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP1653A requires a minimal number of readily available, standard external components, and is available in a space-saving SOT563 (1.6mmx1.6mm) package.

FEATURES

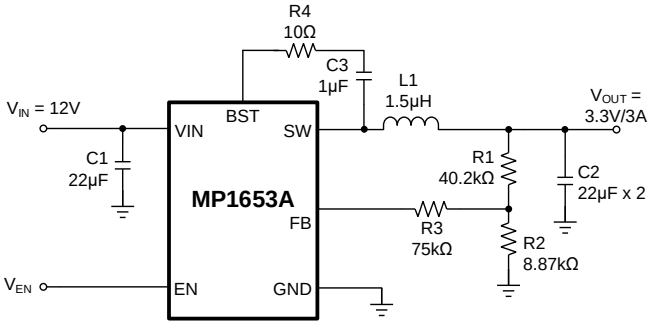
- Forced Pulse-Width Modulation (PWM) Mode
- 1.2MHz Switching Frequency (f_{SW})
- Output Adjustable from 0.6V
- Wide 4.2V to 17V Operating Input Voltage (V_{IN}) Range
- 63mΩ and 36mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 200µA Low Quiescent Current (I_Q)
- High-Efficiency Synchronous Mode
- Fast Load Transient Response
- Internal Soft Start (SS)
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown
- Available in a SOT563 (1.6mmx1.6mm) Package

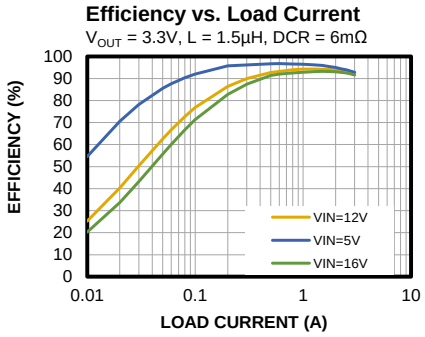
MPL Optimized Performance with MPS Inductor MPL-AL Series

APPLICATIONS

- Routers and Access Points (APs)
- Security Cameras
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General-Purpose Power Supplies

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP1653AGTF	SOT563 (1.6mmx1.6mm)	*See Below*	1

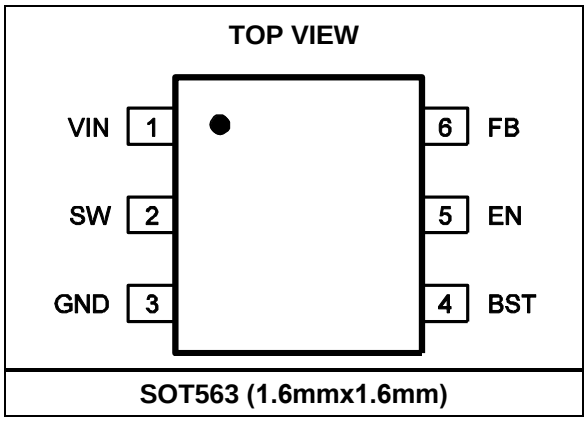
* For Tape & Reel, add suffix -Z (e.g. MP1653AGTF-Z)

TOP MARKING

CADY
LLL

CAD: Product code of MP1653AGTF
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



SOT563 (1.6mmx1.6mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Input voltage.** The MP1653A operates from a 4.2V to 17V input rail. An input capacitor (C1) is required to decouple the input rail. Connect VIN using a wide PCB trace.
2	SW	**Switch output.** Connect SW using a wide PCB trace.
3	GND	**System ground.** GND is the reference ground of the regulated output voltage (V_{OUT}). GND requires careful consideration during PCB layout. Connect GND using copper traces and vias.
4	BST	**Bootstrap.** Connect a 1µF bootstrap (BST) capacitor and a resistor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
5	EN	**Enable.** Pull EN high to turn the converter on; pull EN low to turn it off. For automatic start-up, connect EN to VIN via a 100kΩ pull-up resistor.
6	FB	**Feedback.** To set V_{OUT} , connect FB to the tap of an external resistor divider between the output and GND.

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +18V
V_{SW}.....-0.6V (-6.5V for <10ns) to V_{IN} + 0.3V (19V for <10ns)
V_{BST} ..... V_{SW} + 5V
V_{EN} .....-0.3V to +5V (2)
All other pins .....-0.3V to 5V
Continuous power dissipation (T_A = 25°C) (3) (5) 2.2W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±2000V

Recommended Operating Conditions (4)

Input voltage (V_{IN}) .....4.2V to 17V
Output voltage (V_{OUT})..... 0.6V to V_{IN} x D_{MAX} or 10V max
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance

SOT563	θ_{JA}	θ_{JC}	
EV1653A-TF-00A (5)	55	21	°C/W
JESD51-7 (6)	130	60	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For details on the EN pin's ABS maximum rating, see the Enable (EN) Control section on page 11.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on the EV1653A-TF-00A, 2-layer PCB, 64mmx48mm.
6) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input current (shutdown)	I_{SD}	V_{EN} = 0V			10	μA
Quiescent current	I_Q	V_{EN} = 2V, V_{FB} = 0.65V	170	200	250	μA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BST-SW} = 3.3V		63		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			36		mΩ
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 12V			10	μA
Valley current limit	I_{LIMIT}	V_{OUT} = 0V	2.7	4	5.8	A
Switching frequency	f_{SW}	V_{FB} = 0.55V	1000	1200	1500	kHz
Minimum on time [8]	t_{ON_MIN}			45		ns
Minimum off time [8]	t_{OFF_MIN}			180		ns
Feedback (FB) voltage	V_{FB}	T_J = 25°C	590	603	616	mV
		T_J = -40°C to 125°C	586	603	620	mV
FB current	I_{FB}			10	100	nA
FB under-voltage protection (UVP) threshold (high to low)	V_{UVP}	Hiccup entry		42		% of V_{REF}
Hiccup duty cycle [8]	D_{HICCUP}			25		%
Enable (EN) rising threshold	V_{EN_RISING}		1.14	1.2	1.26	V
EN hysteresis	V_{EN_HYS}			100		mV
EN input current	I_{EN}	V_{EN} = 2V		2		μA
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.7	4	4.18	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			330		mV
Soft-start time	t_{SS}		1.6	2.5	3	ms
Thermal shutdown [8]	T_{SD}			150		°C
Thermal shutdown hysteresis [8]	T_{SD_HYS}			20		°C

Notes:

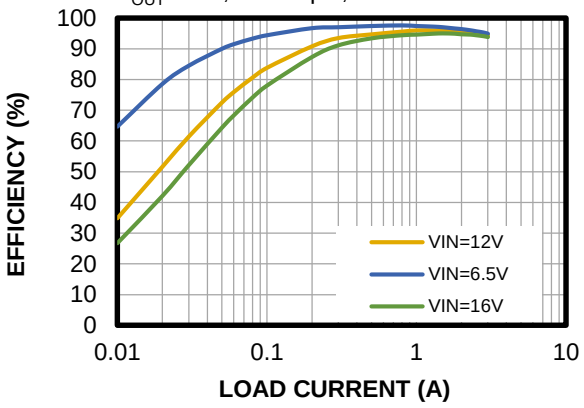
7) Derived by over-temperature (OT) correlation. Not tested in production.
8) Derived by sample characterization. Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

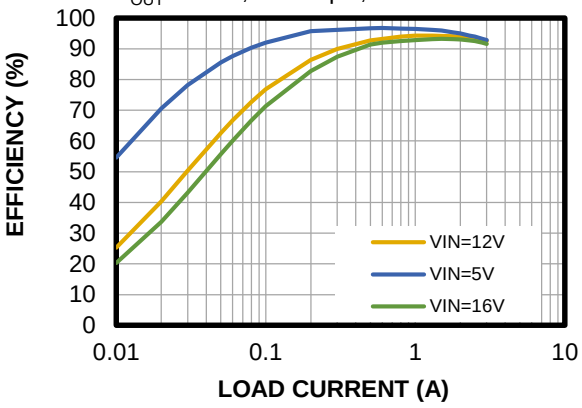
Efficiency vs. Load Current

V_{OUT} = 5V, L = 2.2µH, DCR = 8.3mΩ



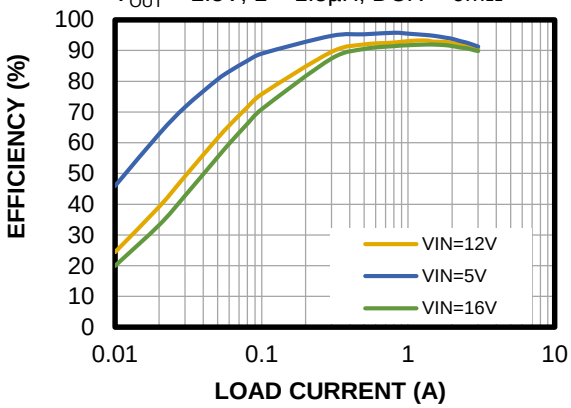
Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 1.5µH, DCR = 6mΩ



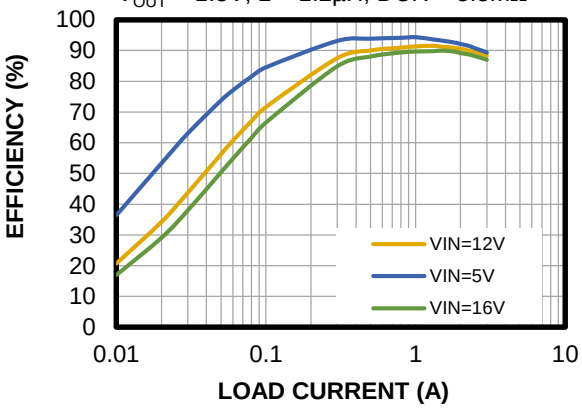
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 1.5µH, DCR = 6mΩ



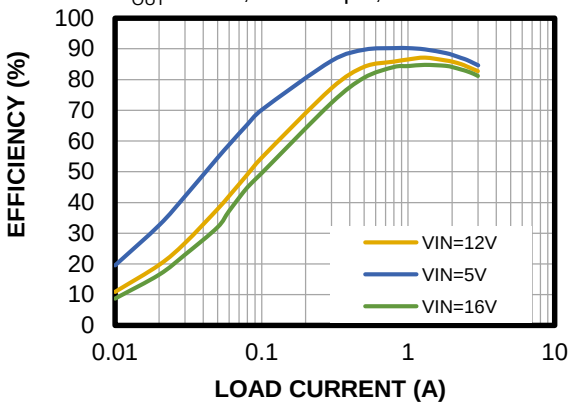
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 1.2µH, DCR = 5.3mΩ



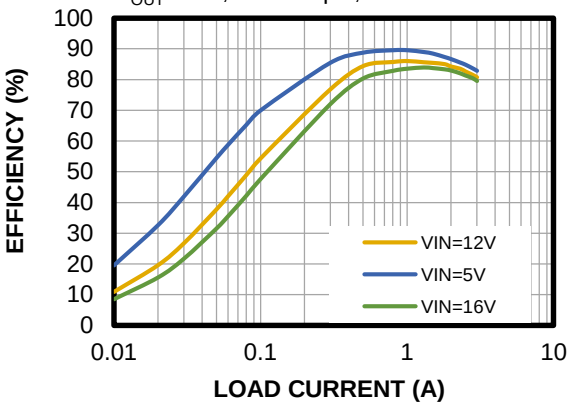
Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 0.68µH, DCR = 7.5mΩ



Efficiency vs. Load Current

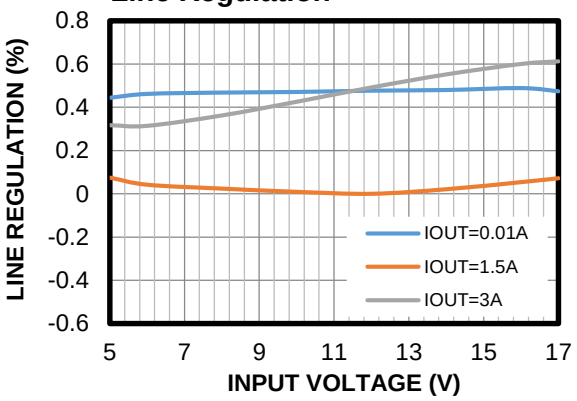
V_{OUT} = 1V, L = 0.68µH, DCR = 7.5mΩ



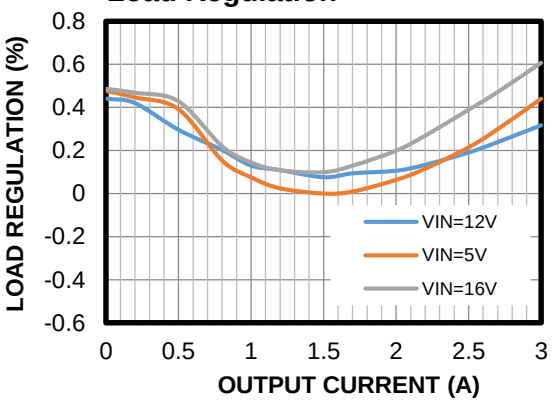
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Line Regulation

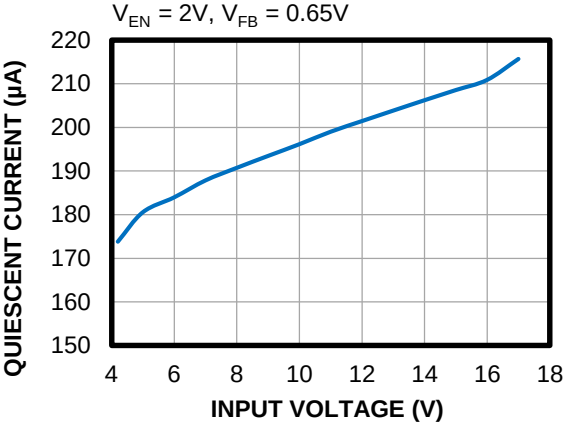


Load Regulation



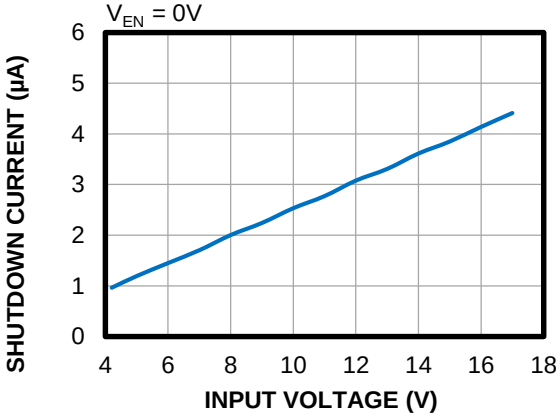
Quiescent Current vs. Input Voltage

V_{EN} = 2V, V_{FB} = 0.65V



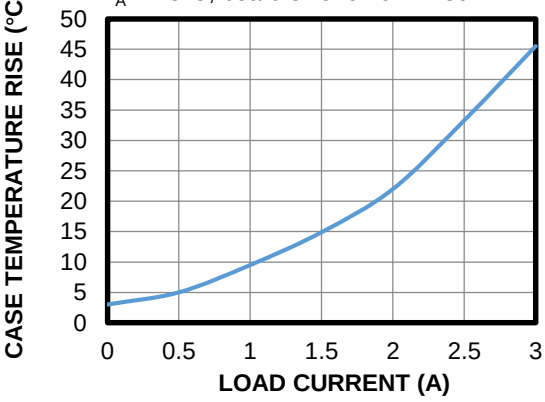
Shutdown Current vs. Input Voltage

V_{EN} = 0V



Case Temperature Rise

T_A = 25°C, board size: 6.4cmx4.8cm

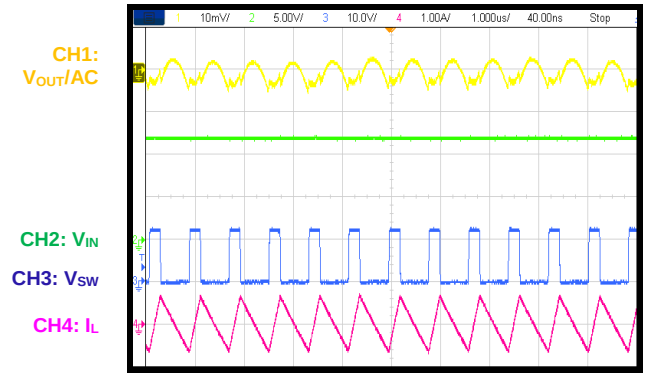


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

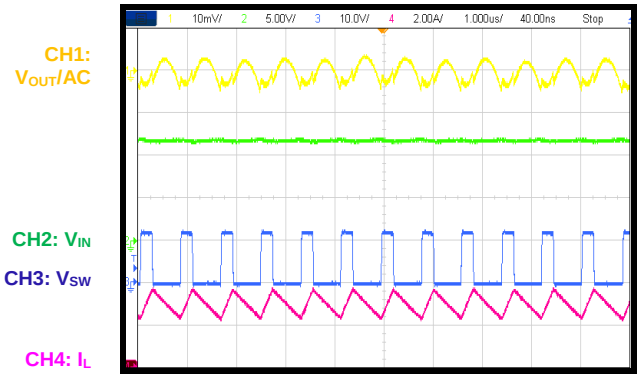
Output Ripple

I_{OUT} = 0A



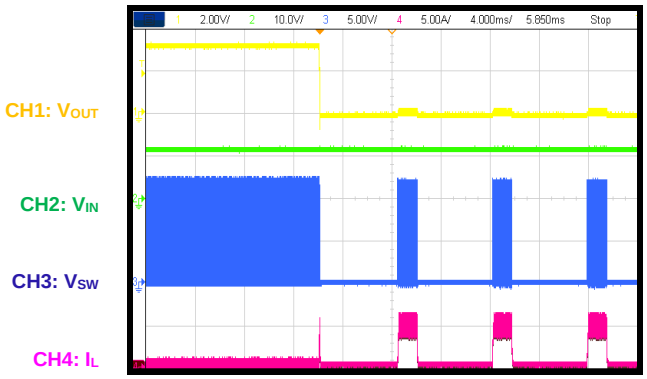
Output Ripple

I_{OUT} = 3A



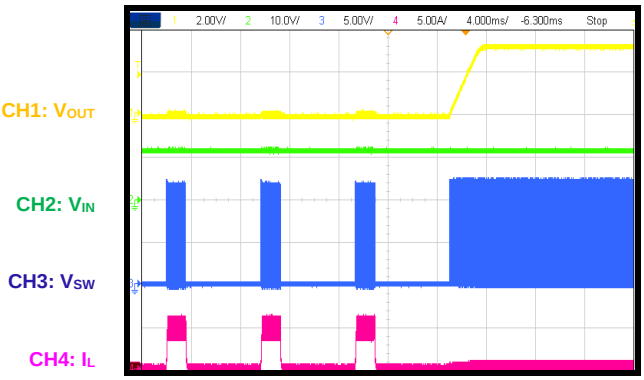
Short-Circuit Entry

I_{OUT} = 0A



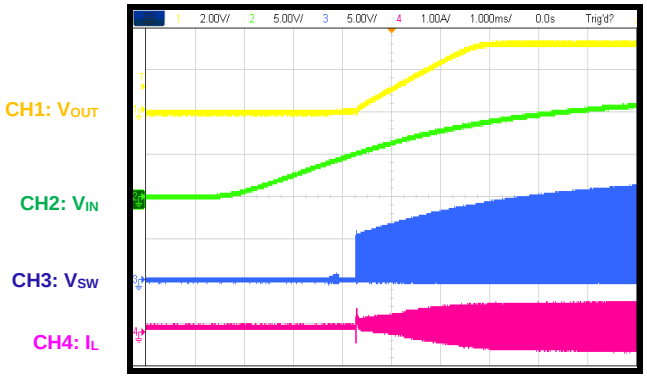
Short-Circuit Recovery

I_{OUT} = 0A



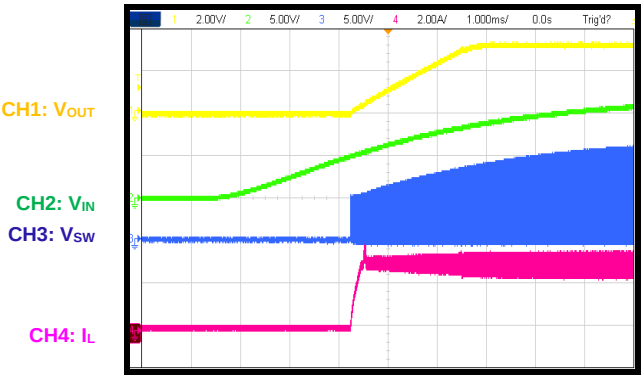
Start-Up through VIN

I_{OUT} = 0A



Start-Up through VIN

I_{OUT} = 3A

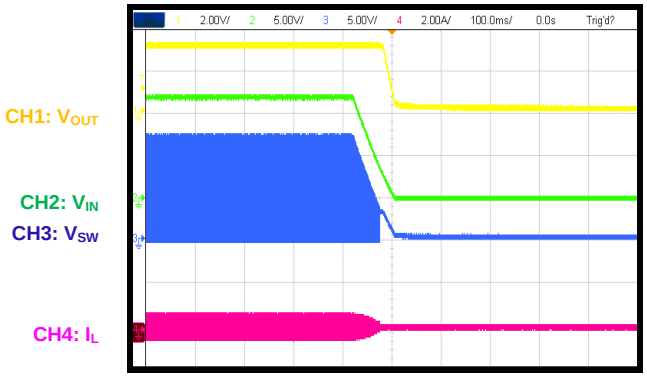


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

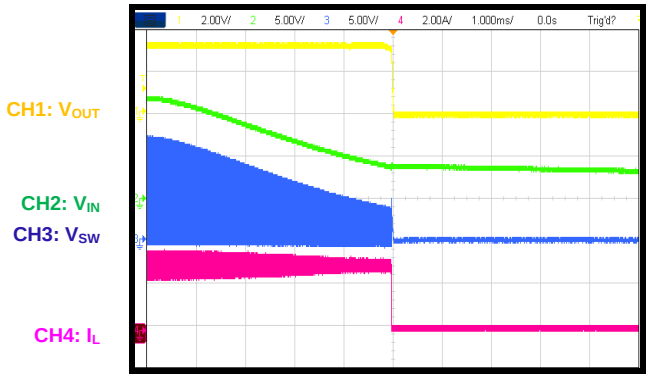
Shutdown through VIN

I_{OUT} = 0A



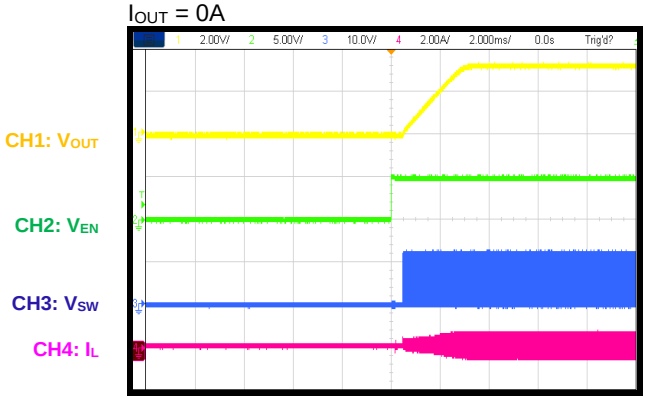
Shutdown through VIN

I_{OUT} = 3A



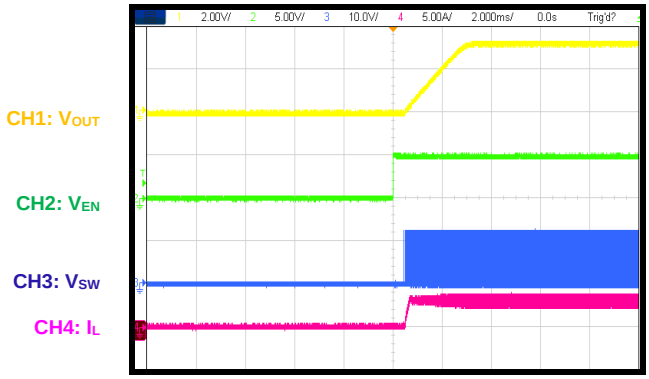
Start-Up through Enable

I_{OUT} = 0A



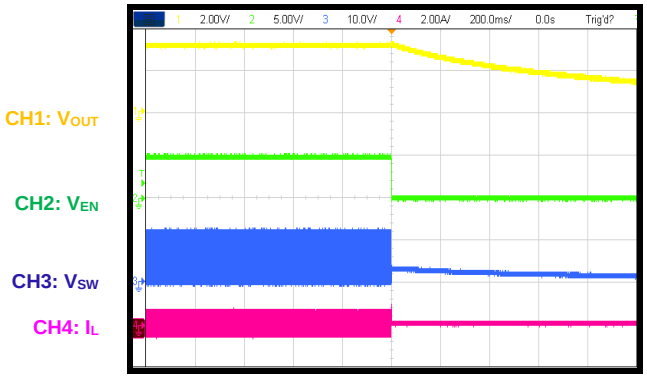
Start-Up through Enable

I_{OUT} = 3A



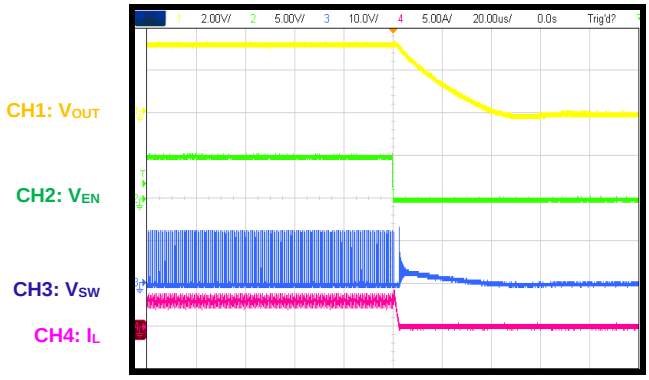
Shutdown through Enable

I_{OUT} = 0A



Shutdown through Enable

I_{OUT} = 3A

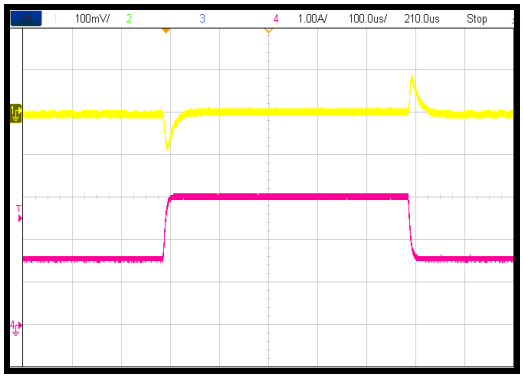


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Load Transient Response

I_{OUT} = 1.5A to 3A, slew rate = 2.5A/µs with e-load



FUNCTIONAL BLOCK DIAGRAM

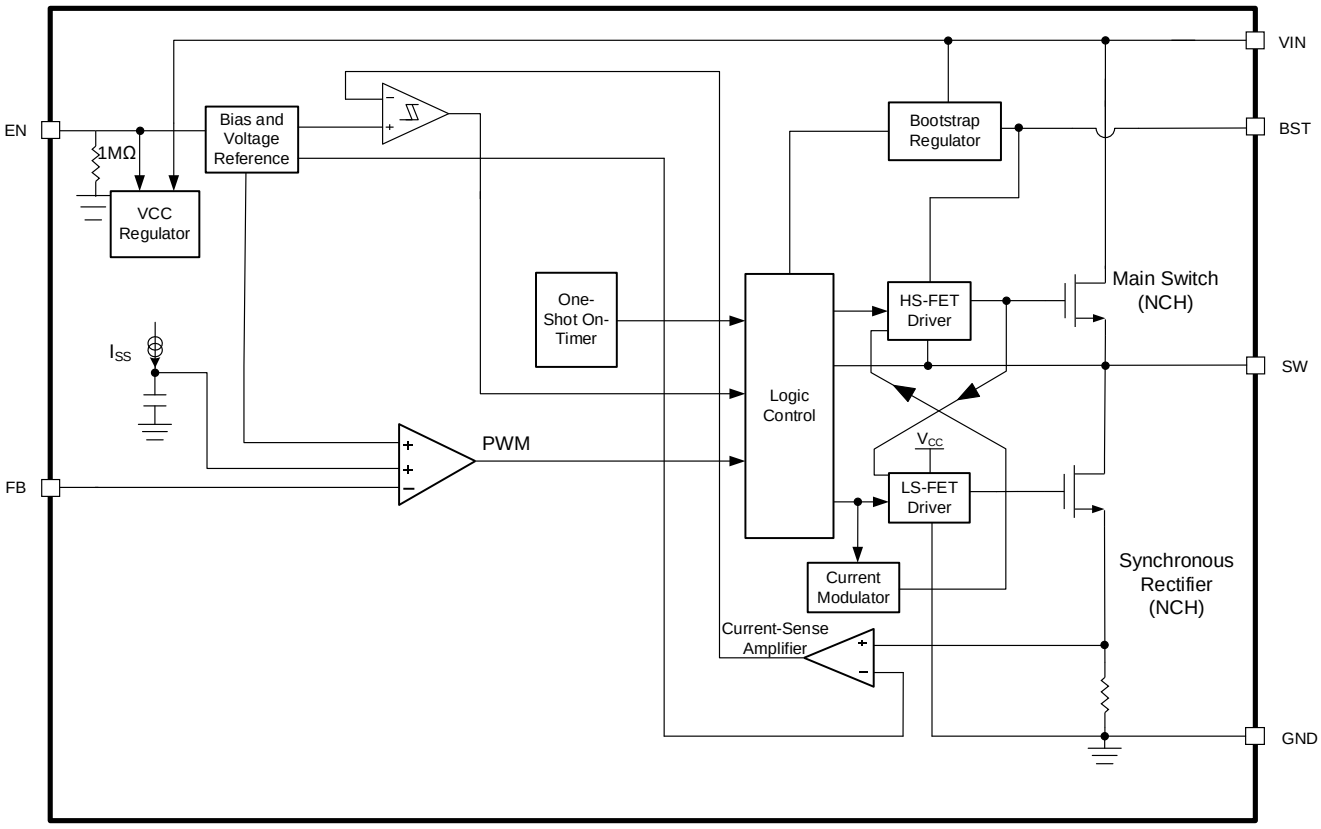


Figure 1: Functional Block Diagram

OPERATION

The MP1653A is a fully integrated, synchronous, rectified, step-down switch-mode converter. Constant-on-time (COT) control provides fast transient response and eases loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}). The HS-FET turns on for a fixed time determined by the one-shot on-timer. The on-timer is determined by both the output voltage (V_{OUT}) and input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the entire V_{IN} range.

After the on time (t_{ON}) elapses, the HS-FET turns off until the next period. The converter regulates the V_{OUT} by repeating operation this way.

The low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET turn on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is inserted internally between the HS-FET off time (t_{OFF}) and LS-FET t_{ON}, or vice versa.

Enable (EN) Control

EN is a digital control pin that turns the converter on and off. Pull EN high to turn the converter on; pull EN low to turn it off. An internal 1MΩ resistor between EN and GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to VIN limits the EN input current below 100μA to prevent damaging the Zener diode. For example, when connecting a 100kΩ pull-up resistor to 12V VIN, I_{Zener} = (12V - 2.8V) / (100kΩ + 35kΩ) = 68μA.

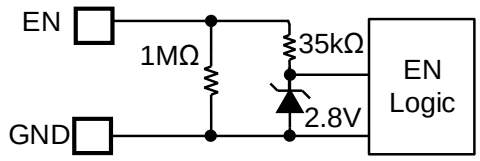


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The V_{IN} UVLO rising threshold is about 4V, while its falling threshold is 3.67V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the device starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1.2V. When V_{SS} drops below V_{REF}, V_{SS} overrides V_{REF} and the error amplifier (EA) uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference. The soft-start time (t_{SS}) is set to 2.5ms internally.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP1653A has a valley current limit (I_{LIMIT}). The inductor current (I_L) is monitored during the LS-FET t_{ON}. When the sensed I_L reaches the I_{LIMIT}, the low-side current-limit comparator turns from low to high, and over-current protection (OCP) is triggered. The HS-FET remains off until I_L drops below I_{LIMIT}. Meanwhile, V_{OUT} drops until V_{FB} is below the under-voltage protection (UVP) threshold (typically 42% of V_{REF}). Once UVP is triggered, the MP1653A enters hiccup mode to restart the part periodically.

During over-current protection (OCP), the device attempts to recover from the over-current (OC) fault with hiccup mode. In hiccup mode, the device disables the output power stage, discharges V_{SS}, and initiates an SS automatically. If the OC fault still remains after the SS is complete, the device repeats this operation until the OC fault is removed. Then the output rises back to the regulation level. OCP is a non-latch protection.

Pre-Bias Start-Up

The MP1653A is designed for monotonic start-up into a pre-biased load. If the output is pre-biased to a certain voltage during start-up, the bootstrap (BST) voltage (V_{BST}) is refreshed and charged, and V_{SS} is also charged.

If V_{BST} exceeds its rising threshold and V_{SS} exceeds the sensed V_{FB}, the MP1653A starts up and operates normally.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. Once the temperature falls below the lower threshold (typically 130°C), the device initiates an SS to resume normal operation.

Floating Driver and Bootstrap (BST) Charging

An external BST capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a 2.2V rising threshold of and 150mV hysteresis. VIN regulates V_{BST} internally via D1, M1, C3, L1, and C2 (see Figure 3). If the difference between V_{IN} and the SW voltage (V_{SW}) exceeds 3.3V, U2 regulates M1 to maintain a 3.3V V_{BST} across C3.

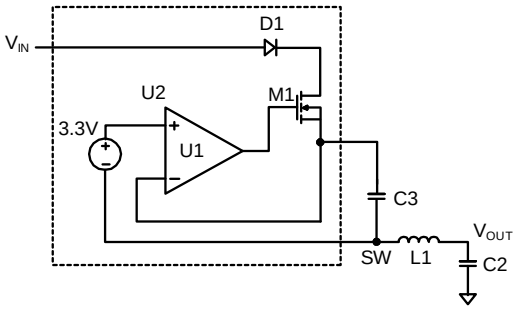


Figure 3: Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If both V_{IN} exceeds the V_{IN} UVLO rising threshold and the EN voltage (V_{EN}) exceed the EN rising threshold, the device starts up. The reference block starts up first to generate a stable V_{REF} and current, and then the internal regulator starts up to provides a stable supply for the remaining circuitry.

Three events can shut down the chip: EN pulling low, V_{IN} going low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path to avoid triggering any faults. Then the internal supply rail is pulled down.

APPLICATION INFORMATION

Setting the Output Voltage

An external resistor divider (R1 + R2) sets V_{OUT}. Choose an appropriate resistance for R2. A lower resistance causes considerable quiescent current (I_Q) loss, while a higher resistance makes FB sensitive to noise. It is recommended to choose R2 to be between 5kΩ and 100kΩ. The current flowing through R2 should be below 150μA to provide balance between system stability and no-load loss. R1 can be calculated with Equation (1):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (1)$$

Figure 4 shows the FB network.

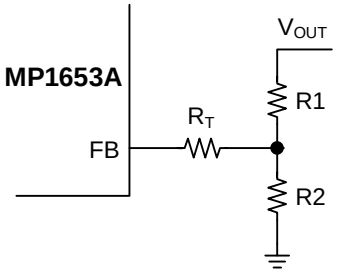


Figure 4: Feedback Network

Table 1 lists the recommended resistances for common output voltages.

Table 1: Recommended Resistances for Common Output Voltages (C_{OUT} = 22μF x 2) (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	L (μH)
5	40.2	5.49	75	2.2
3.3	40.2	8.87	75	1.5
2.5	40.2	12.7	100	1.5
1.8	40.2	20	110	1.2
1.5	40.2	26.7	249	1
1.2	40.2	40.2	249	0.68
1	20.5	30.9	348	0.68

Note:

9) For the detailed design circuit, see the Typical Application Circuits section on page 16.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the step-down converter while maintaining the DC V_{IN}. For the best results, it is recommended to use X5R or X7R ceramic capacitors due to their stability amid temperature fluctuations. Place these capacitors as close to VIN as possible.

The capacitors should have a ripple current rating greater than the converter's maximum input ripple current (I_{CIN_MAX}). The input ripple current (I_{CIN}) can be estimated with Equation (2):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (2)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (3):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (3)$$

For simplification, choose an input capacitor (C1) with an RMS current rating greater than half of the maximum load current (I_{LOAD_MAX}).

C1 determines the converter's V_{IN} ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, choose C1 to meet the specification.

ΔV_{IN} can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C1} \quad (5)$$

Selecting the Output Capacitor

An output capacitor (C_{OUT}) is required to maintain the DC V_{OUT}. Ceramic or POSCAP capacitors are recommended. The V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (6)$$

With ceramic capacitors, the capacitance dominates the impedance at f_{SW}. ΔV_{OUT} is mainly caused by the capacitance. For simplification, caused can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

ΔV_{OUT} caused by the ESR is very small.

With POSCAP capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

A larger C_{OUT} can improve load transient response, but consider the maximum C_{OUT} limitation in the application design. If design is too large, V_{OUT} cannot reach the design value during the t_{SS} and fails to regulate. The maximum C_{OUT} (C_{OUT_MAX}) can be estimated with Equation (9):

$$C_{OUT\_MAX} = (I_{LIMIT\_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \quad (9)$$

Where I_{LIMIT_AVG} is the average start-up current during the t_{SS}.

Selecting the Inductor

An inductor is required to supply constant current to the output load, while being driven by the switched V_{IN}. A larger-value inductor results in less ripple current and a lower output voltage ripple (ΔV_{OUT}); however, a larger-value inductor also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance is to design the inductor's peak-to-peak ripple current (ΔI_L) to be between 30% and 60% of the maximum I_{OUT}. The inductance (L) can be calculated with Equation (10):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The inductor should not saturate under the maximum peak I_L (I_{L_PEAK}). The peak inductor current can be calculated with Equation (11):

$$I_{L\_PEAK} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on the design requirements.

Table 2: Power Inductor Selection

Part Number	Inductance	Manufacturer
MPL-AL	0.68µH to 2.2µH	MPS
MPL-AL4020-R68	0.68µH	MPS
MPL-AL6050-1R0	1µH	MPS
MPL-AL6050-1R2	1.2µH	MPS
MPL-AL6050-1R5	1.5µH	MPS
MPL-AL6050-2R2	2.2µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Design Example

Table 3 shows a design example when ceramic capacitors are applied.

Table 3: Design Example

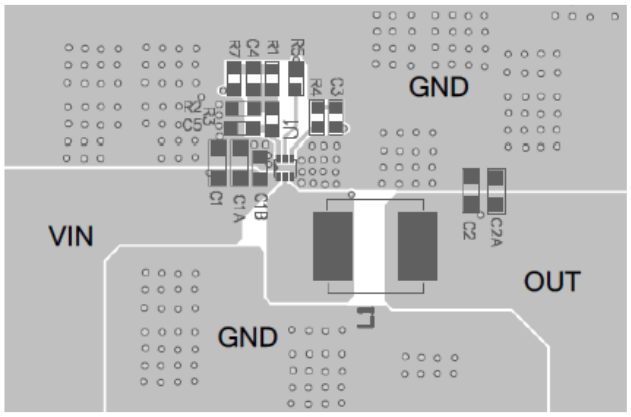
V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	3A

The detailed application schematics are shown in Figures 6–12 on page 16. The typical performance and waveforms are shown in the Typical Performance Characteristics section on page 5. For more device applications, refer to the related evaluation board datasheet.

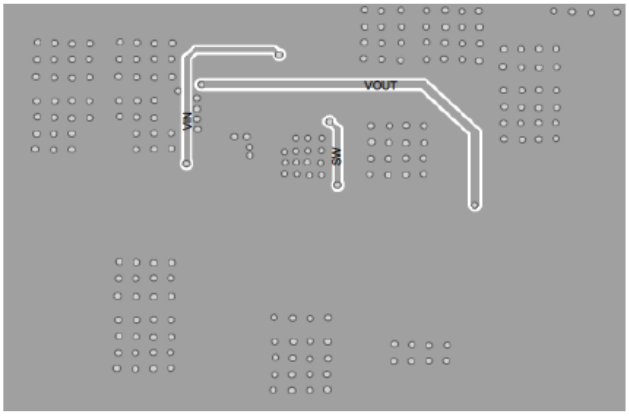
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 5 and follow the guidelines below:

1. Connect the high-current paths (GND, VIN, and SW) using short, direct, and wide traces.
2. Place the GND, VIN, and SW as close to the device as possible.
3. Place the input capacitor as close to VIN and GND as possible (recommended to be within 1mm).
4. Place the external FB resistors next to the FB pin.
5. Route the switching node (SW) away from the FB network using short traces.



Top Layer



Bottom Layer

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

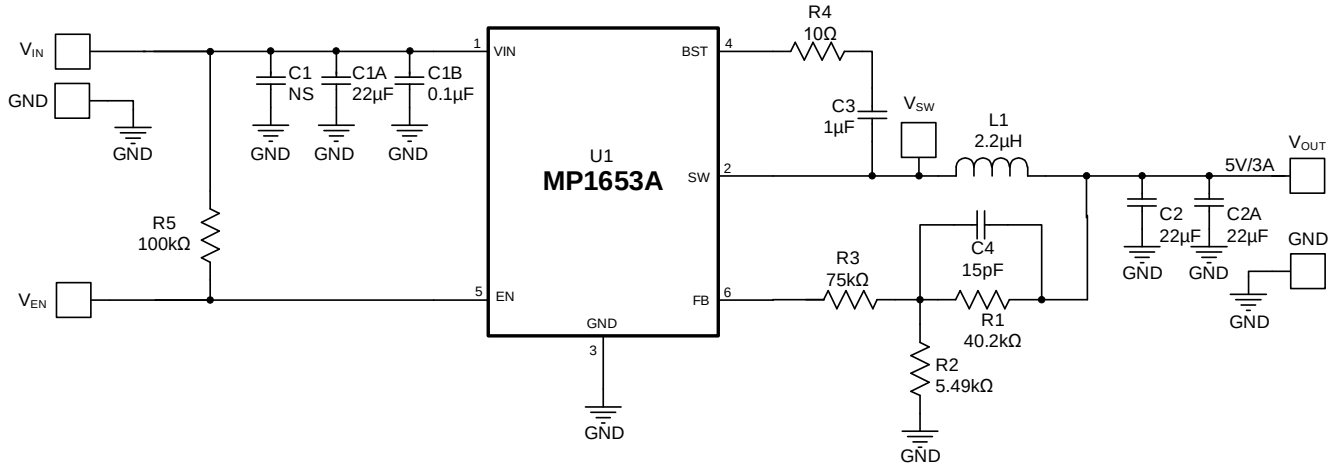


Figure 6: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 5V/3A)

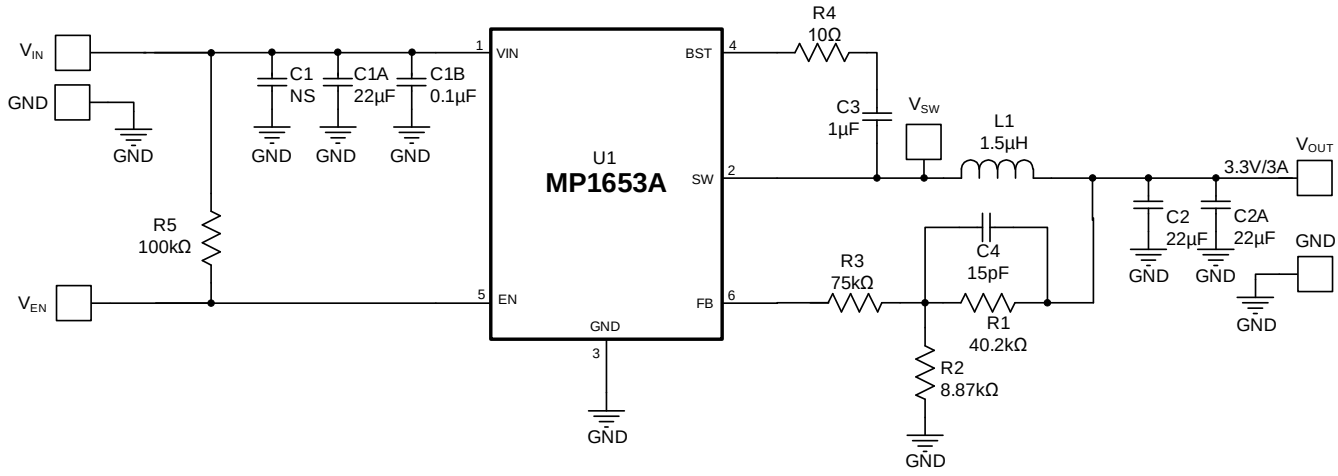


Figure 7: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 3.3V/3A)

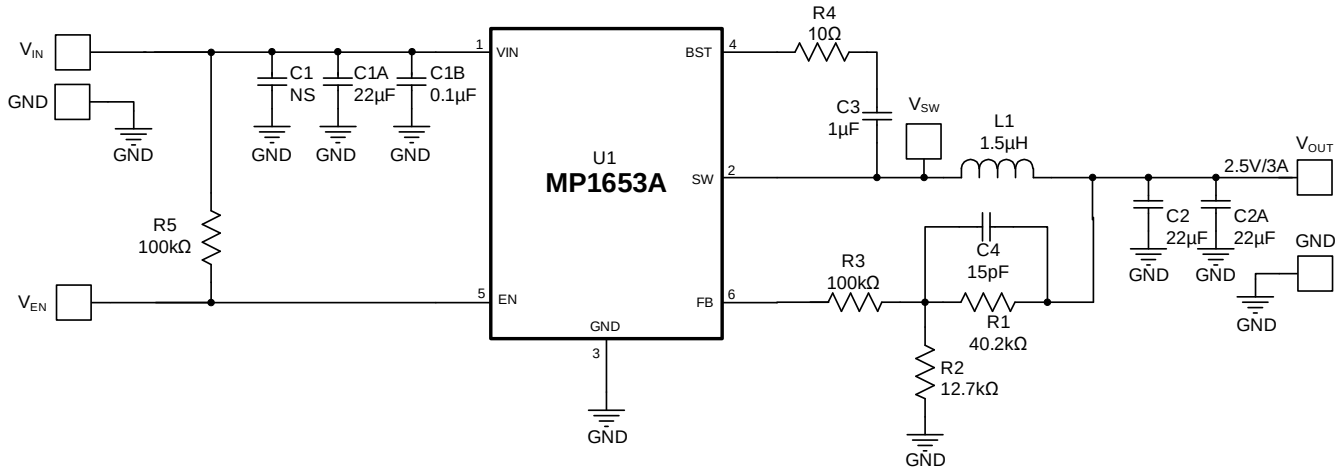


Figure 8: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 2.5V/3A)

TYPICAL APPLICATION CIRCUITS *(continued)*

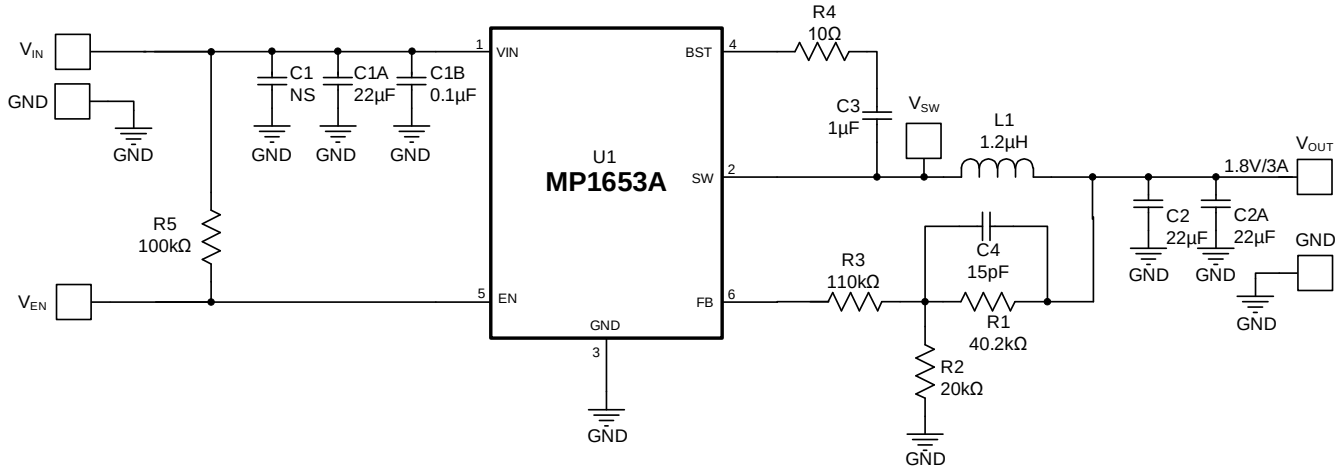


Figure 9: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.8V/3A)

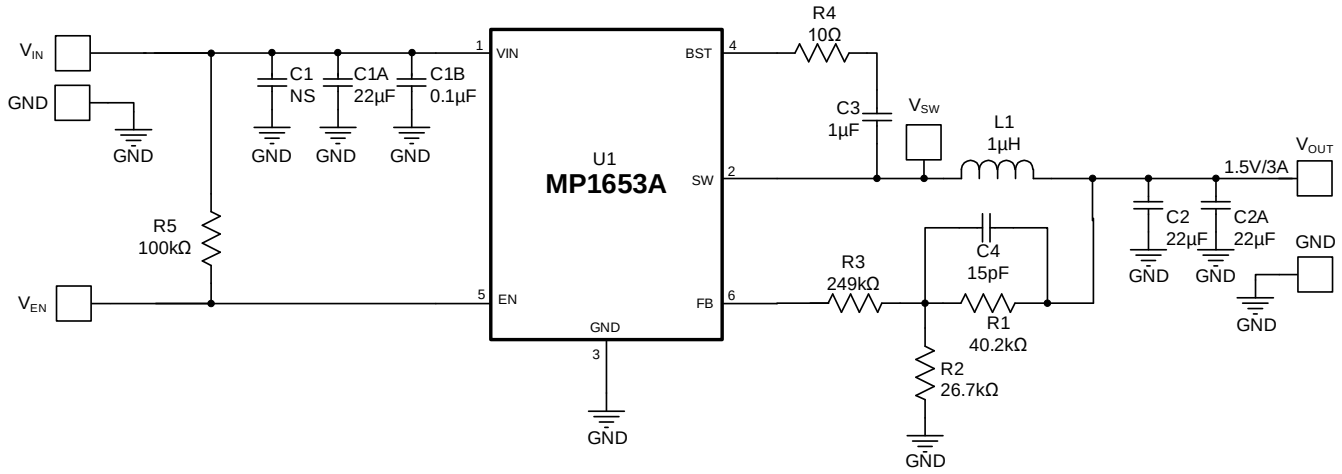


Figure 10: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.5V/3A)

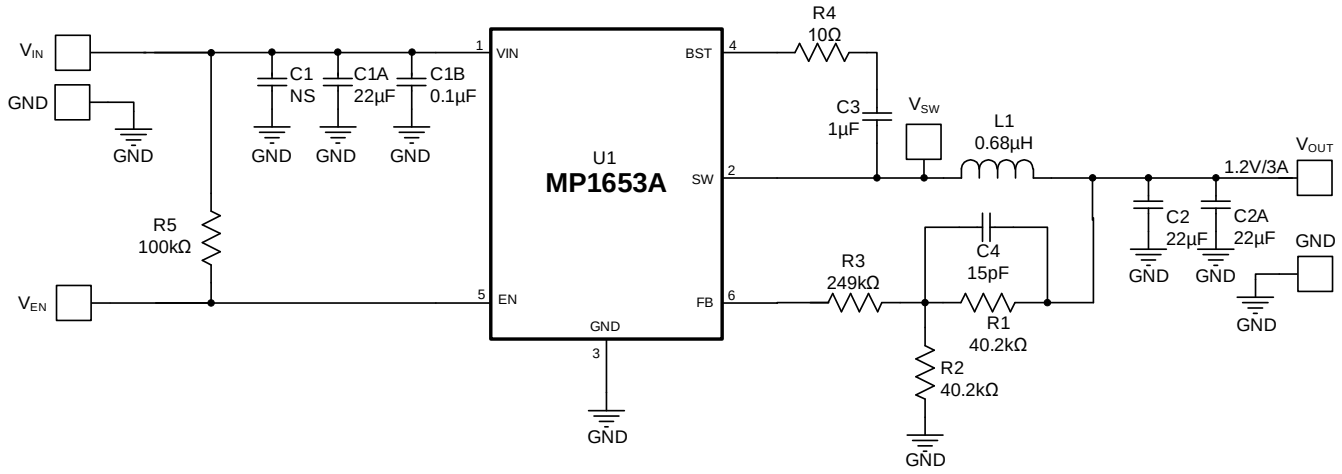


Figure 11: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.2V/3A)

TYPICAL APPLICATION CIRCUITS *(continued)*

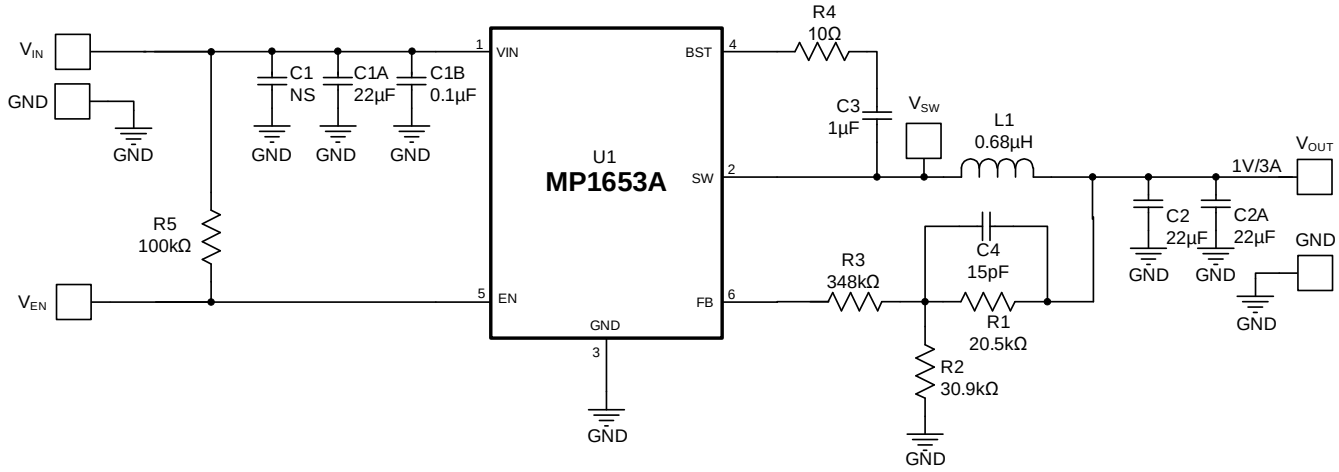
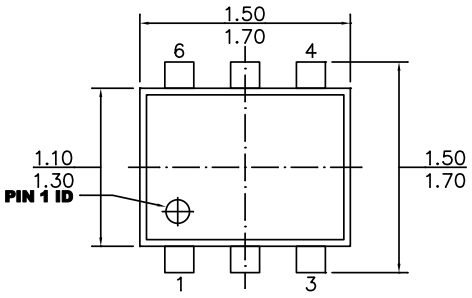


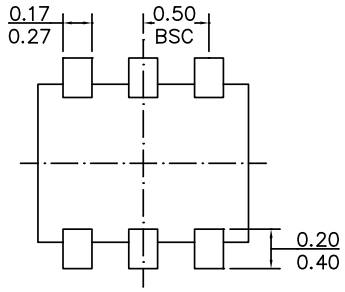
Figure 12: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1V/3A)

PACKAGE INFORMATION

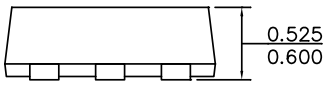
SOT563 (1.6mmx1.6mm)



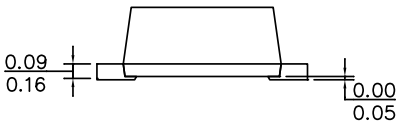
TOP VIEW



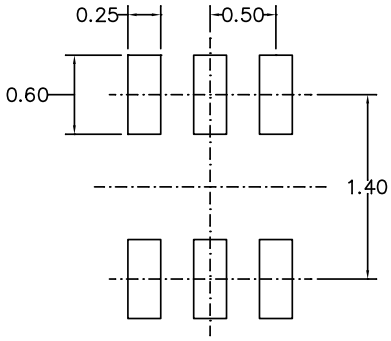
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

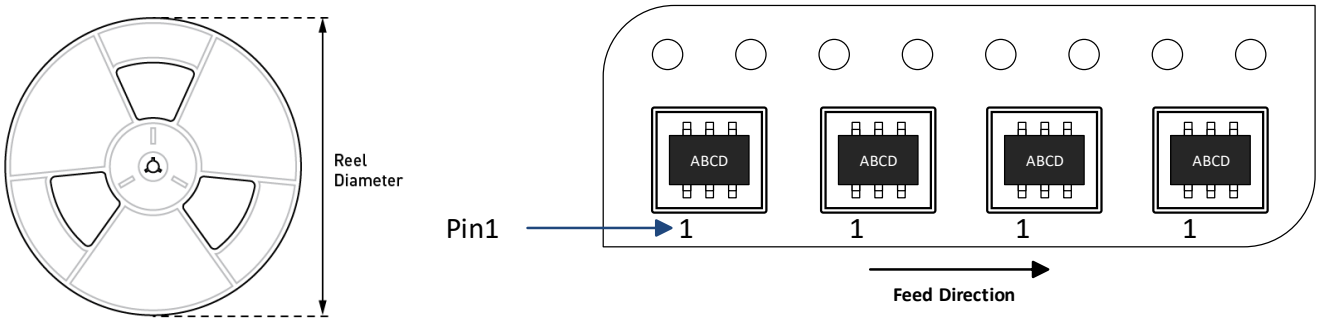


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP1653AGTF-Z	SOT563 (1.6mmx1.6mm)	5000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	06/26/2023	Initial Release	-