

AM27S02, AM27S03

64-Bit Inverting-Output Bipolar RAM

The AM27S02 and AM27S03 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active-LOW chip select (\overline{CS}) input and open-collector OR-tieable outputs (AM27S02) or three-state outputs (AM27S03). Chip selection for large memory systems can be controlled by active-LOW output decoders such as the AM74S138.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.



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Am27S02/Am27S03

64-Bit Inverting-Output Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 18 word x 4-bit low-power Schottky RAMS
- Ultra-Fast Version: Address access time 25 ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
 Available with open-collector outputs (Am27S02) or with
- three-state outputs (Am27S03)
- Pin-compatible replacements for 3101A, 74S289, (use Am27S02); for 74S189, (use Am27S03)

lines are LOW the information on the four data inputs Do to

D₃ is written into the addressed memory word and precon-

ditions the output circuitry so that correct data is present at

GENERAL DESCRIPTION

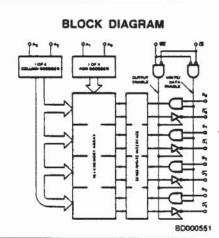
The Am27S02 and Am27S03 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active-LOW chip select (CS) input and open-collector OR-iseable outputs (Am27S02) or three-state outputs (Am27S03). Chip selection for large memory systems can be controlled by active-LOW output decoders such as the Am74S138.

An active-LOW Write line (WE) controls the writing/reading

operation of the memory. When the chip select and write

the outputs when the write cycle is complete. This preconditioning operation ensures minimum write recovery times by eliminating the "write recovery glitch." Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O_0}$ to $\overline{O_3}$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.



MODE SELECT TABLE

Input		Data Output			
CS	WE	Data Output Status Og - Og	Mode		
L	L	Output Disabled	Write		
L	н	Selected Word (Inverted)	Read		
н	X	Output Disabled	Deselect		

L=LOW

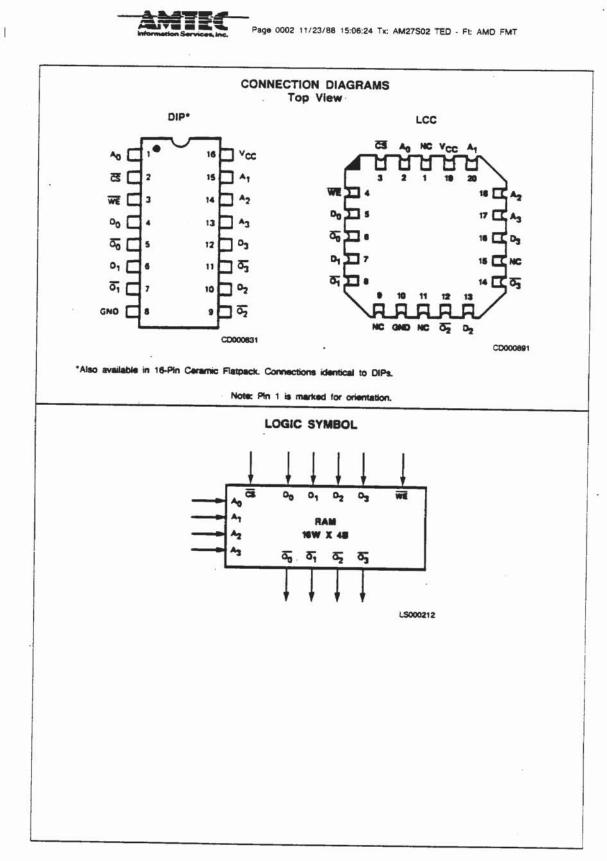
X = Don't Care

PRODUCT SELECTOR GUIDE

Access Time	25 ns	30 ns	35 ns	50 ns
lcc	70 mA	70 mA	70 mA	70 mA
Temperature Range	С	M	С	м
Open Collector	Am27S02A	Am27S02A	Am27S02	Am27502
Three State	Am27S03A	Am27S03A	Am27S03	Am27S03

Public	ation		Rev.	Amendment		
02191			F	/0		
SSUR	Date:	Ja	nuary	1989		

Am27S02/Am27S03

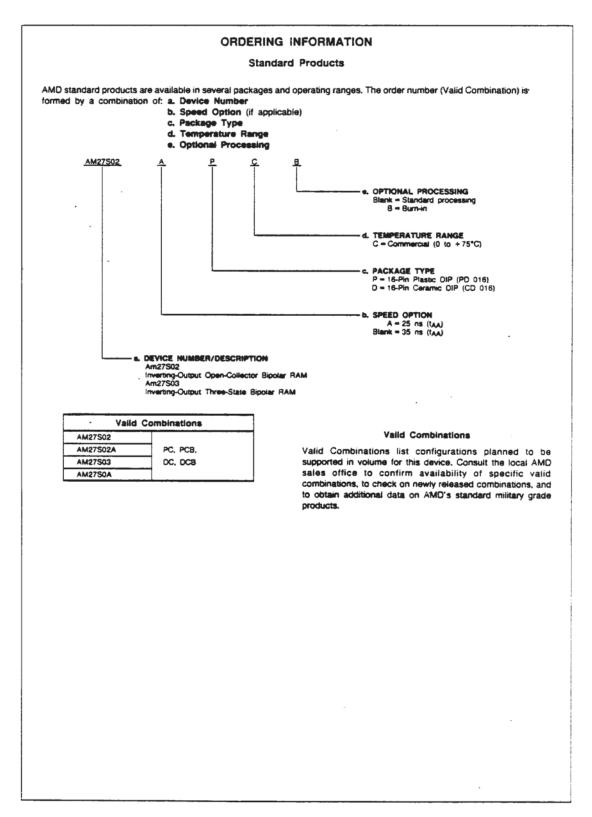


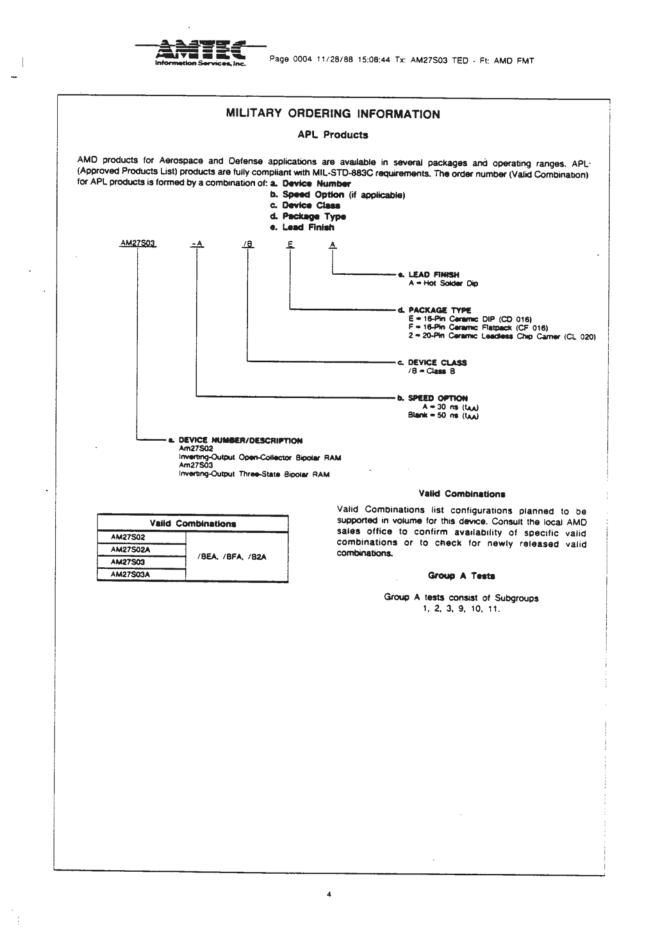
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ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C Ambient Temperature with Power Applied-55 to +125°C

Supply Voltage -0.5 V to +7.0 V DC Voltage Applied to Outputs -0.5 V to + VCC Max. DC Input Voltage -0.5 V to +5.5 V DC Input Current -30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices Temperature 0 to +75°C Supply Voltage + 4.75 V to + 5.25 V

Military" (M) Devices

Temperature -55 to +125°C Supply Voltage + 4.5 V to + 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

"Military products 100% tested at Tc = +25°C, +125°C, and -55°C. (see note 5)

DC CHARACTERISTICS over opeating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter				Am2			
	Description	Test Conditions				Typ.	Max.	Unit
VOH	Output HIGH	Vcc = Min.,	10H = -5.2 mA	COM'L	- 2.4	3.0		v
(Note 2)	Voltage	VIN = VIH OF VIL	IOH = -2.0 mA	MIL				
VOL	Output LOW	Vcc = Min.,	IOL = 16 mA			350	450	10.000
·u.	Voltage					-380	500	۳V
VIH	Input HIGH Level	Guaranteed Input Lo Voltage for All Input	2.0			v		
VIL	Input LOW Level	Guaranteed Input Lo Voltage for All Input			0.8			
h	Input LOW Current	Voc - Max., WE. Do-Da, Ag-Ag				-15	-250	0.00
4L		VIN = 0.40 V	CS .		- 30	-250	μA	
lu r	Input HIGH Current	Vcc = Max., Vin = 2.7 V				0	10	дĄ
ISC (Note 2)	Output Short Circuit Current	VCC - Max., VOUT = 0.0 V (Note	- 20	-45	- 90			
lcc	Power Supply Current	All Inputs = GND Outputs = Open Vcc = Max.		50	70	πA		
VCL	Input Clamp Voltage	Vcc = Min., im = - 1		-0.85	-1.2	v		
ICEX	Output Leakage Current	VCS = VIH or VWE= VOUT = 2.4 V. VCC	VR_ - Max.			0	40	
		VCS - VIH OF VWE - VOUT - 0.4 V. VCC		(Note 2)	(Note 2) -40 0			μА

Notes: 1. Typical limits are at VCC = 5.0 V and TA = 25°C.

This applies to three-state devices only.
These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

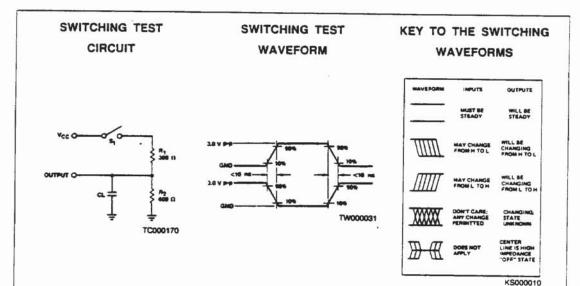
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second. 5. Operating specifications with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performance instantaneously where $T_A = T_C = T_J$.

 $\theta_{JA} \approx 50$ *C/W (with moving air) for Ceramic DIP. $\theta_{JA} \approx 10-17^{*}$ C/W for flatpack and leadless chip carrier.

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SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified*

				Am27502A/3A				Am27502/3			
			C Devices		M Devices		STD C Devices		STD M Devices		
No.	No. Parameter Symbol	Parameter Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
1	(PLH(A)										
2	tPHL(A)	Delay from Address to Output		25		30		35		50	ns
з	tPZH(CS)	Delay from Chip Select (LOW) to	_								
4	(PZL(CS)	Active Output and Correct Data		15		20		17		25	ns
5		Delay from Write Enable (HIGH) to Active Output and Correct Data									
6	PZL(WE)	(Write Recovery-See Note 1) -		20		25		35		40	ns
7	t _s (A)	Setup Time Address (Prior to Initiation of Write)	0		0		0		0		ns
8	th(A)	Hold Time Address (After Termination of Write)	0		0		0		0	-	ns
9	t _s (DI)	Setup Time Data Input (Prior to Termination of Write)	20		25		25		25		ns
10	4n(DI)	Hold Time Data Input (After Termination of Write)	0		0		0	•	0		ns
11	Low(WE)	MIN Write Enable Width Pulse to Insure Write	20		25		25		25		ns
12	PHZ(CS)	Delay from Chip Select (HIGH)									
13	tpLZ(CS)	to inactive Output (HI-Z)		15	1	20		17		25	ns
14	IPLZ(WE)	Delay from Write Enable (LOW)									
15	IPHZ(WE)	to inactive Output (HI-Z)		20		25		25		35	ns

Notes: 1. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)

recovery glitch.) 2. tpLH(A) and tpHL(A) are tested with St closed and CL = 50 pF with both input and output timing referenced to 1.5 V. 3. For open collector, all delays from Write Enable (WE) or Chip Select (CS) inputs to the Data Output (D_{OUT}), tpL_Z(WE), tpL_Z(CS), tpL_Z(WE) and tp_Z(CS) are measured with St closed and CL = 30 pF and with both the input and output timing referenced to 1.5 V. 4. For 3-state output, tp_Z(WE) and tp_Z(CS) are measured with St open, CL = 50 pF and with both the input and output timing referenced to 1.5 V. tp_Z(WE) and tp_Z(CS) are measured with St closed, CL = 50 pF and with both the input and output timing referenced to 1.5 V. tp_Z(WE) and tp_Z(CS) are measured with St closed, CL = 50 pF and are measured between the 1.5 V level on the input to the VOH = 500 mV level on the output. tpL_Z(WE) and tp_{LZ}(CS) are measured with St closed and CL ≤ 5 pF and are measured between the 1.5 V level on the input and the VOL = 500 mV level on the input and the VOL = 500 mV level on the input and the VOL = 500 mV level on the output.



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