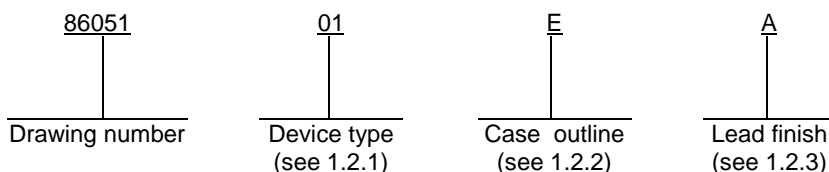|		REVISIONS		
LTR	DESCRIPTION		DATE (YR-MO-DA)	APPROVED
A	Update vendor's part number. Change to military drawing format. Editorial changes throughout.		87-07-07	M. A. Frye
B	Made technical changes to table I. Added device types 07, 08, and 09 for vendor CAGE 34335. Changes to figures 4, 5, 6. Changes to 4.3.2 and 6.4. Corrected CAGE code on front page. Editorial changes throughout.		89-06-13	M. A. Frye
C	Boilerplate update, part of 5 year review. ksr		05-08-31	Raymond Monnin
D	Updated body of drawing to reflect current requirements. - glg		11-03-08	Charles Saffle
E	Update drawing to reflect current MIL-PRF-38535 requirements. – llb		18-01-03	Charles Saffle

CURRENT CAGE CODE 67268

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED

REV															
SHEET															
REV															
SHEET															
REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Sandra Rooney	**DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990** **http://www.dla.mil/landandmaritime**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY D. A. DiCenzo	
	APPROVED BY Don Cool	MICROCIRCUIT, MEMORY, DIGITAL, BIPOLAR 64-BIT RAM, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 86-03-25	
	REVISION LEVEL E	SIZE A / CAGE CODE 14933 / 86051
		SHEET 1 OF 14

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5962-E176-18

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

```
    86051              01              E              A
      |                 |              |              |
      |                 |              |              |
 _____      _____     _____    _____
Drawing number    Device type    Case  outline   Lead finish
                  (see 1.2.1)     (see 1.2.2)     (see 1.2.3)
```

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	27S02	64-Bit Schottky bipolar RAM, open collector outputs	50
02	27S02A	64-Bit Schottky bipolar RAM, open collector outputs	30
03	27LS02	64-Bit Low power schottky bipolar RAM, open collector outputs	65
04	27S03	64-Bit Schottky bipolar RAM, three-state outputs	50
05	27S03A	64-Bit Schottky bipolar RAM, three-state outputs	30
06	27LS03	64-Bit Low power schottky bipolar RAM, three-state outputs	65
07	27S02-20	64-Bit Schottky bipolar RAM, open collector outputs	20
08	27S03-20	64-Bit Schottky bipolar RAM, three-state outputs	20
09	27LS03-30	64-Bit Low power Schottky bipolar RAM, three-state outputs	30

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line package
F	GDFP2-F16 or CDFP3-F16	16	Flat package
2	CQCC1-N20	20	Square-chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

```
Supply voltage range ...................................................-0.5 V dc to +7.0 V dc
Input voltage range ......................................................-0.5 V dc to +5.5 V dc
Storage temperature range ..........................................-65°C to +150°C
Maximum power dissipation (P_D) 1/ ............................1.6 W
Lead temperature (soldering, 10 seconds)...................+300°C
Thermal resistance, junction-to-case (θ_JC):
  Cases E, F and 2  ...................................................  See MIL-STD-1835
Junction temperature (T_J)............................................+175°C
DC input current  ........................................................-30 mA to +5 mA
```

1.4 Recommended operating conditions.

```
Supply voltage range (V_CC) .........................................4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_IH)........................2.0 V dc
Maximum low-level input voltage (V_IL)..........................0.8 V dc
Case operating temperature range (T_C) ......................-55°C to +125°C
```

1/   Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 1.

3.2.2 <u>Truth table</u>. The truth table shall be as specified on figure 2.

3.2.3 <u>Logic diagram</u>. The logic diagram shall be as specified on figure 3.

3.2.4 <u>Case outlines</u>. The case outlines shall be in accordance with 1.2.2 herein.

3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. <u>Electrical performance characteristics.</u>

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ $4.5 \text{ V dc} \leq V_{CC} \leq 5.5 \text{ V dc}$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output high voltage	V_{OH}	V_{CC} = min. $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -2.0 mA	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = min. $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 16 mA	1,2,3	01,02, 04,05, 07,08		450	mV
			I_{OL} = 20 mA		01,02, 04,05, 07,08		500	
			I_{OL} = 10 mA		03,06,09		500	
			I_{OL} = 8 mA		03,06,09		450	
Input high level voltage	V_{IH}	Guaranteed input logical high 1/ voltage for all inputs		1,2,3	All	2.0		V
Input low level voltage	V_{IL}	Guaranteed input logical low 1/ voltage for all inputs		1,2,3	All		0.8	V
Input low current	I_{IL}	V_{CC} = max V_{IN} = 0.40 V	$\overline{WE}$, D_0-D_3, A_0-A_3, $\overline{CS}$					
Input high current	I_{IH}	V_{CC} = max, V_{IN} = 2.7 V		1,2,3	All		10	µA
Output short circuit current	I_{OS}	V_{CC} = max V_{OUT} = 0.0 V 2/		1,2,3	All	-20	-90	mA
Power supply current	I_{CC}	All inputs = GND V_{CC} = max		1,2,3	01,02,04, 05,07,08		105	mA
					03,06,09		38	
Input clamp voltage	V_{CL}	V_{CC} = min, I_{IN} = -18 mA		1,2,3	All		-1.2	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V dc ≤ V_{CC} ≤ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output leakage current	I_{CEX}	$V_{\overline{CS}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$ V_{OUT} = 2.4 V	1,2,3	All		40	μA
		$V_{\overline{CS}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$ V_{OUT} = 0.4 V		All		-40	
Delay from address to output	$t_{PLH(A)}$ $t_{PHL(A)}$	See figures 4 and 6 3/	9,10,11	01,04		50	ns
				02,05,09		30	
				03,06		65	
				07,08		20	
Delay from chip select (LOW) to active output and correct data	$t_{PZH(\overline{CS})}$ $t_{PZL(\overline{CS})}$	See figures 4 and 6 4/ 5/	9,10,11	01,04		25	ns
				02,05,07, 08,09		20	
				03,06		35	
Delay from write enable (HIGH) to active output and correct data (write recovery) 6/	$t_{PZH(\overline{WE})}$ $t_{PZL(\overline{WE})}$	See figures 4 and 5 4/ 5/	9,10,11	01,04		40	ns
				02,05		25	
				03,06		35	
				07,08,09		15	
Setup time address (prior to initiation of write)	$t_{s(A)}$	See figures 4 and 5	9,10,11	All	0		ns
Hold time address (after termination of write)	$t_{h(A)}$	See figures 4 and 5	9,10,11	All	0		ns
Setup time data input (prior to termination of write)	$t_{s(DI)}$	See figures 4 and 5	9,10,11	09	30		ns
				01,02,04, 05	25		
				03,06	55		
				07,08	20		
Hold time data input (after termination of write)	$t_{h(DI)}$	See figures 4 and 5	9,10,11	All	0		ns

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> – Continued.

Test	Symbol	Conditions -55°C $\leq$ T$_C$ $\leq$ +125°C 4.5 V dc $\leq$ V$_{CC}$ $\leq$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Min write enable pulse width to insure write	t$_{pw(\overline{WE})}$	See figures 4 and 5	9,10,11	09	30		ns
				01,02, 04,05	25		
				03,06	55		
				07,08	20		
Delay from chip select HIGH) to inactive output (HI-Z)	t$_{PHZ(\overline{CS})}$ t$_{PLZ(\overline{CS})}$	See figures 4 and 6 <u>4</u>/ <u>5</u>/	9,10,11	01,04, 09		25	ns
				02,05, 07,08		20	
				03,06		35	
Delay from write enable (LOW) to inactive output (HI-Z)	t$_{PLZ(\overline{WE})}$ t$_{PHZ(\overline{WE})}$	See figures 4 and 5 <u>4</u>/ <u>5</u>/	9,10,11	01,03, 04,06		35	ns
				02,05, 09		25	
				07,08		20	

<u>1</u>/ These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

<u>2</u>/ Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

<u>3</u>/ Parameters t$_{PLH(A)}$ and t$_{PHL(A)}$ are tested with S1 closed and CL = 30 pF with both input and output timing referenced to 1.5 V.

<u>4</u>/ For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D$_{OUT}$), t$_{PLZ(\overline{WE})}$, t$_{PLZ(\overline{CS})}$, t$_{PZL(\overline{WE})}$, and t$_{PZL(\overline{CS})}$ are measured with S1 closed and C1 = 30 pF; and with both the input and output timing referenced to 1.5 V.

<u>5</u>/ For 3-state output, t$_{PZH(\overline{WE})}$ and t$_{PZH(\overline{CS})}$ are measured with S1 open, CL = 30 pF and with both the input and output timing referenced to 1.5 V. Parameters t$_{PZL(\overline{WE})}$ and t$_{PZL(\overline{CS})}$ are measured with S1 closed, CL = 30 pF and with both the input and output timing referenced to 1.5 V. Parameters t$_{PHZ(\overline{WE})}$ and t$_{PHZ(\overline{CS})}$ are measured with S1 open and CL < 5 pF and are measured between the 1.5 V level on the input and the V$_{OH}$ = -500 mV level on the output. Parameters t$_{PLZ(\overline{WE})}$ and t$_{PLZ(\overline{CS})}$ are measured with S1 closed CL $\leq$ 5 pF and are measured between the 1.5 V level on the input and the V$_{OL}$ = +500 mV level on the output.

<u>6</u>/ Output is preconditioned to data in (inverted) during write to ensure correct data is present on all outputs when write is terminated. (No write recovery glitch).
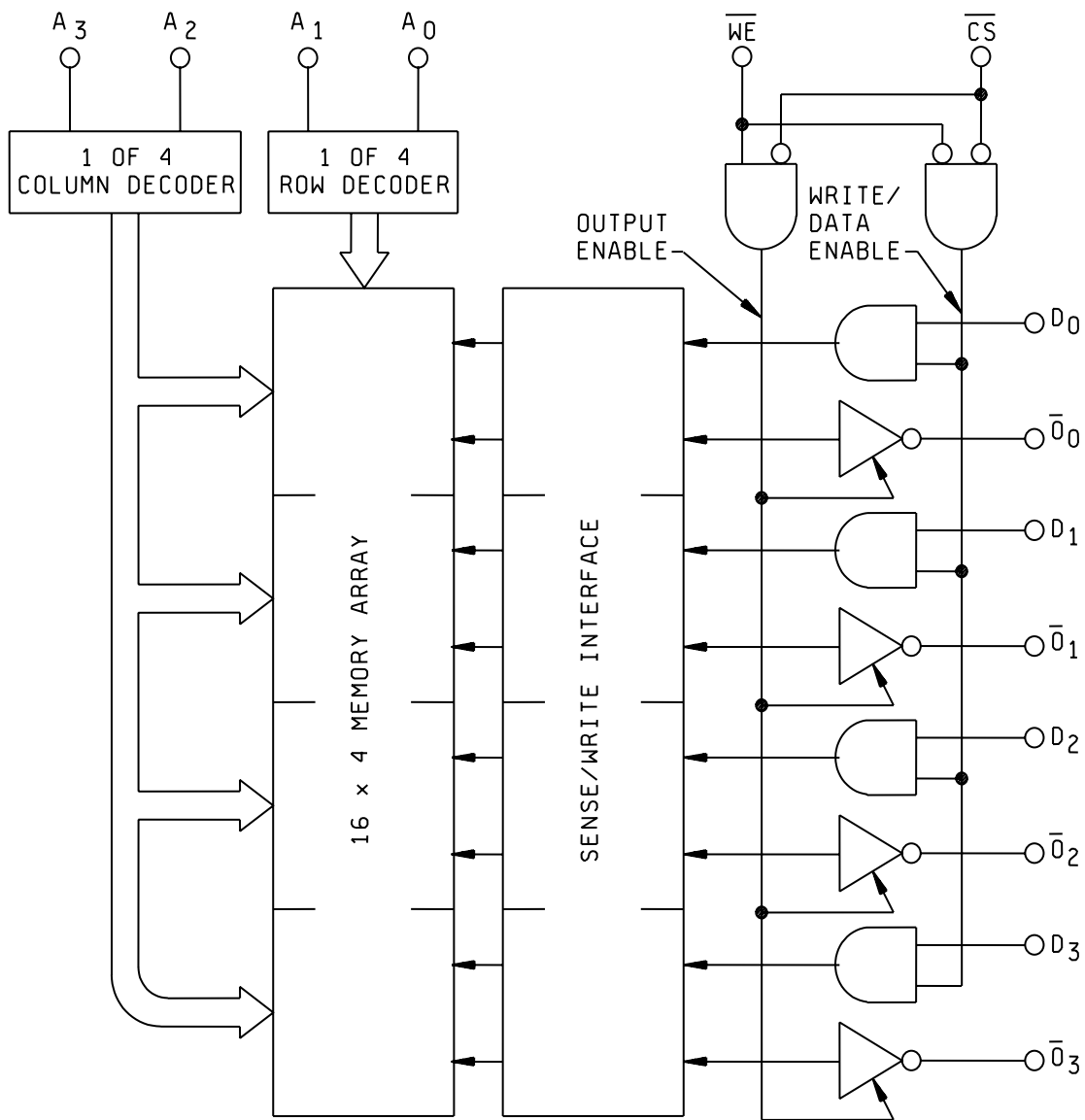
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Device Types	All	
Case Outlines	E and F	2
Terminal Number	Terminal Symbol	
1	A_0	NC
2	$\overline{CS}$	A_0
3	$\overline{WE}$	$\overline{CS}$
4	D_0	$\overline{WE}$
5	$\overline{O}_0$	D_0
6	D_1	$\overline{O}_0$
7	$\overline{O}_1$	D_1
8	GND	$\overline{O}_1$
9	$\overline{O}_2$	NC
10	D_2	GND
11	$\overline{O}_3$	NC
12	D_3	$\overline{O}_2$
13	A_3	D_2
14	A_2	$\overline{O}_3$
15	A_1	NC
16	V_{CC}	D_3
17	---	A_3
18	---	A_2
19	---	A_1
20	---	V_{CC}

FIGURE 1. Terminal connections.

Input		Data output status $\overline{O}_0$ - $\overline{O}_3$	Mode
$\overline{CS}$	$\overline{WE}$		
L	L	Output disabled	Write
L	H	Selected word (inverted)	Read
H	X	Output disabled	Deselect

H = HIGH   L = LOW   X = Don't Care

FIGURE 2. Truth table.

A₃ A₂   A₁ A₀   WE   CS

1 OF 4 COLUMN DECODER   1 OF 4 ROW DECODER

OUTPUT ENABLE

WRITE/ DATA ENABLE

16 x 4 MEMORY ARRAY

SENSE/WRITE INTERFACE

D_0
$\overline{D}_0$
D_1
$\overline{D}_1$
D_2
$\overline{D}_2$
D_3
$\overline{D}_3$

FIGURE 3. Logic diagram.

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SWITCHING TEST
CIRCUIT
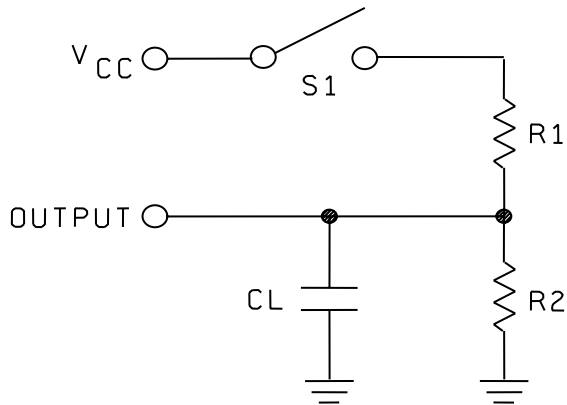
SWITCHING TEST
WAVEFORM
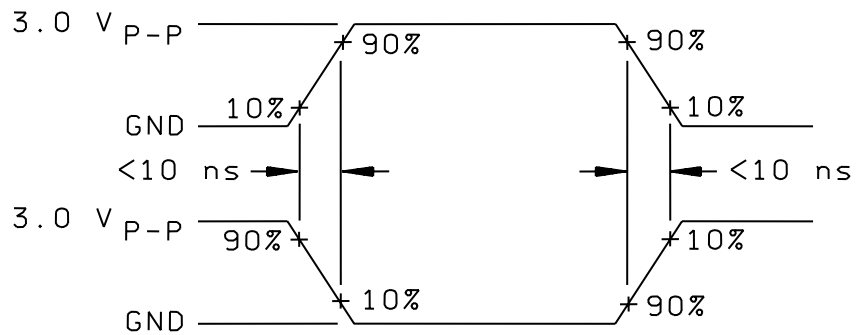
Device	R1	R2
01, 02 04, 05 07, 08	300Ω	600Ω
03, 06 09	600Ω	1200Ω

FIGURE 4. Switching test circuit and waveform.

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WRITE MODE
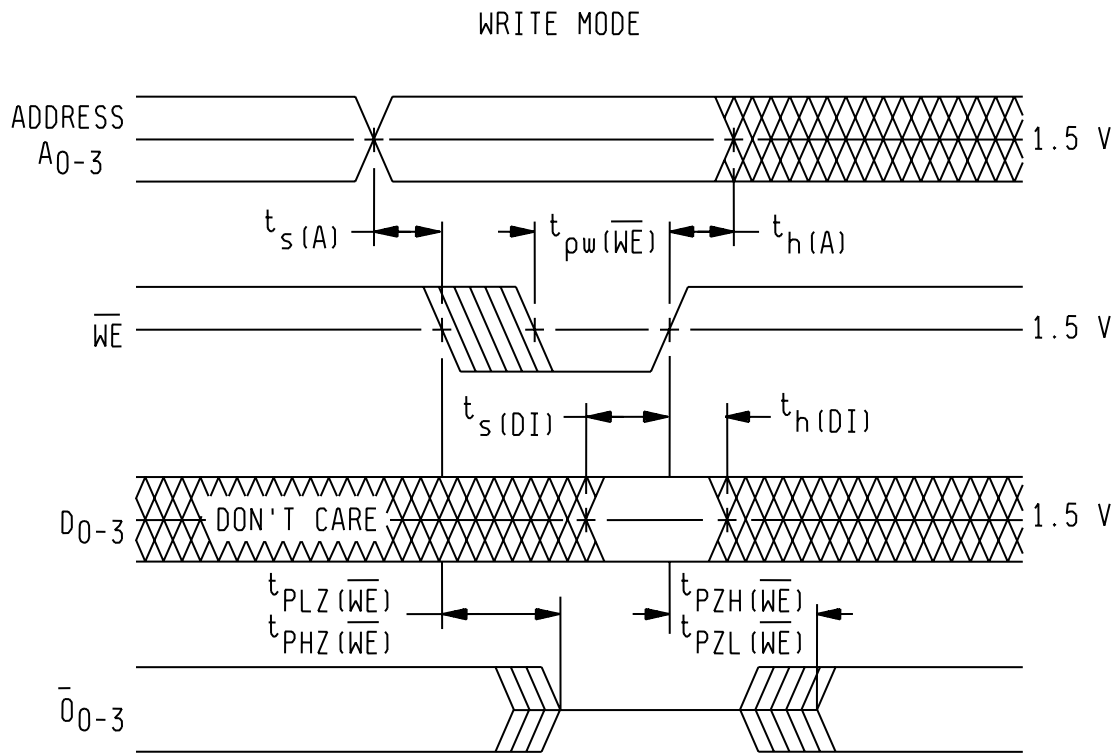
NOTE: Write cycle time. The cycle is initiated by an address change. After $t_{s(A)}$ minimum the write enable may begin.
The chip select must also be LOW for writing. Following the write pulse, $t_{h(A)}$ minimum must be allowed before the
address may be changed again. The output will be inactive (floating for the O_4, O_5, O_6, O_8, and O_9) while the write
enable is LOW.

FIGURE 5. Write mode switching waveform.
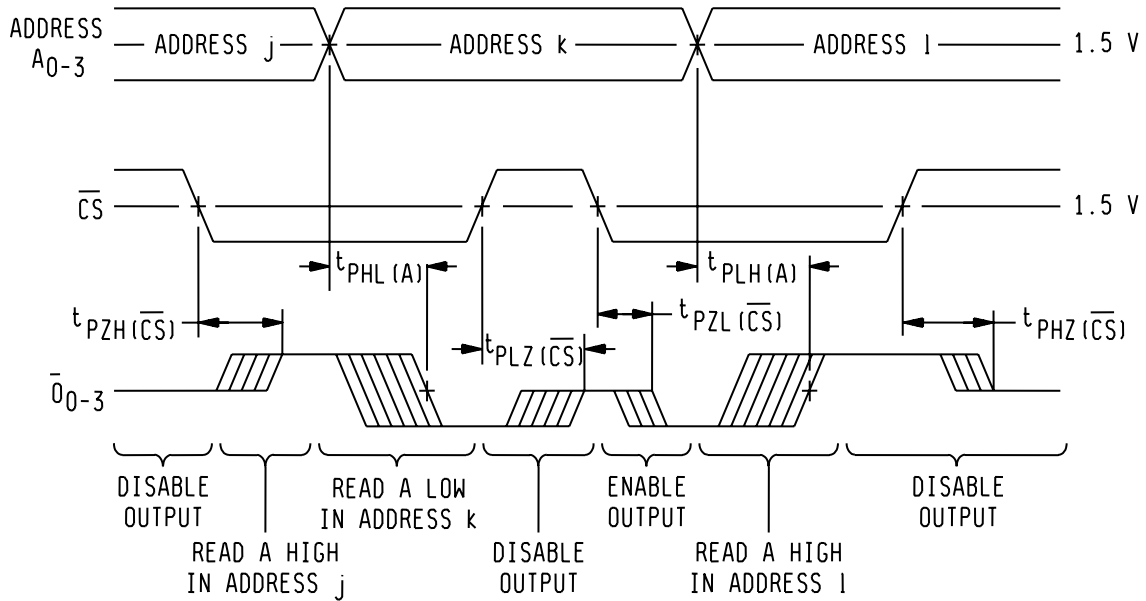
NOTE: Switching delays from address and chip select inputs to the data output. For the O_4, O_5, O_6, O_8, and O_9 device types disabled output is "OFF", represented by a single center line. For the 01, 02,03, and 07 device types a disable output is HIGH.

FIGURE 6. Read mode switching waveform.

4. VERIFICATION

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

   a. Burn-in test, method 1015 of MIL-STD-883.

     (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

     (2) T_A = +125°C, minimum.

   b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. <u>Electrical test requirements</u>.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8A, 8B, 9, 10**, 11**
Group A test requirements (method 5005)	1, 2, 3, 7***, 8A***, 8B***, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

   *   PDA applies to subgroups 1.

   **   Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

   ***   See 4.3.1c

4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 <u>Group A inspection</u>.

   a. Tests shall be as specified in table II herein.

   b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

   c. Subgroups 7 and 8 shall include verification of the truth table.

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4.3.2 <u>Groups C and D inspections</u>.

   a. End-point electrical parameters shall be as specified in table II herein.

   b. Steady-state life test conditions, method 1005 of MIL-STD-883.

      (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

      (2) T_A = +125°C, minimum.

      (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 <u>Record of users</u>. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 <u>Comments</u>. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 18-01-03

Approved sources of supply for SMD 86051 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: https://landandmaritimeapps.dla.mil/programs/smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8605101EA	3/	AM27S02/BEA
8605101FA	3/	AM27S02/BFA
86051012A	3/	AM27S02/B2A
8605102EA	3/	AM27S02A/BEA
8605102FA	3/	AM27S02A/BFA
86051022A	3/	AM27S02A/B2A
8605103EA	3/	AM27LS02/BEA
8605103FA	3/	AM27LS02/BFA
86051032A	3/	AM27LS02/B2A
8605104EA	0DKS7 3V146 3/	GEM13404QEA 27S03/BEA AM27S03/BEA
8605104EC	0DKS7	GEM13404QEC
86051042A	0DKS7 3V146 3/	GEM13404Q2A 27S03/B2A AM27S03/B2A
86051042C	0DKS7	GEM13404Q2C
8605104FA	0DKS7 3V146 3/	GEM13404QFA 27S03/BFA AM27S03/BFA
8605104FC	0DKS7	GEM13404QFC
8605105EA	3V146 3/	27S03A/BEA AM27S03A/BEA
8605105FA	3V146 3/	27S03A/BFA AM27S03A/BFA

See notes at end of table.

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8605106FA	0DKS7 3V146 3/	GEM31606QFA 27LS03/BFA AM27LS03/BFA
86051052A	3V146 3/	27S03A/B2A AM27S03A/B2A
8605106EA	0DKS7 3V146 3/	GEM31606QEA 27LS03/BEA AM27LS03/BEA
8605106EC	0DKS7	GEM31606QEC
8605106FC	0DKS7	GEM31606QFC
86051062A	3V146 3/	27LS03/B2A AM27LS03/B2A
8605107EA	3/	AM27S02-20/BEA
8605107FA	3/	AM27S02-20/BFA
86051072A	3/	AM27S02-20/B2A
8605108EA	3V146 3/	27S03-20/BEA AM27S03-20/BEA
8605108FA	3V146 3/	27S03-20/BFA AM27S03-20/BFA
86051082A	3V146 3/	27S03-20/B2A AM27S03-20/B2A
8605109EA	3V146 3/	27LS03-30/BEA AM27LS03-30/BEA
8605109FA	3V146 3/	27LS03-30/BFA AM27LS03-30/BFA
86051092A	3V146 3/	27LS03-30/B2A AM27LS03-30/B2A

See notes at end of table.

1/ The lead finish shown for each PIN representing
a hermetic package is the most readily available
from the manufacturer listed for that part. If the
desired lead finish is not listed contact the vendor
to determine its availability.

2/ Caution. Do not use this number for item
acquisition. Items acquired to this number may not
satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0DKS7	SRI International 201 Washington Road Princeton, NJ 08540-6449
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950