Product Change Notification / SYST-29LANR577

Date:

30-Jan-2024

Product Category:

32-Bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

PIC32MK General Purpose and Motor Control GPG/MCJ with CAN FD Family Silicon Errata and Data Sheet Clarifications

Affected CPNs:

SYST-29LANR577_Affected_CPN_01302024.pdf
SYST-29LANR577_Affected_CPN_01302024.csv

Notification Text:

SYST-29LANR577

Microchip has released a new Document for the PIC32MK General Purpose and Motor Control GPG/MCJ with CAN FD Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC32MK General Purpose and Motor Control GPG/MCJ with CAN FD Family Silicon Errata and Data Sheet Clarifications.

Notification Status: Final

Description of Change: The following new Data Sheet Clarification was added: • Packaging

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 30 Jan 2024

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC32MK General Purpose and Motor Control GPG/MCJ with CAN FD Family Silicon Errata and Data Sheet Clarifications

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Affected Catalog Part Numbers (CPN)

PIC32MK0512MCJ064-E/R4X
PIC32MK0512MCJ064-E/PT
PIC32MK0512MCJ064-I/R4X
PIC32MK0512MCJ064-I/PT
PIC32MK0512MCJ064T-I/R4X
PIC32MK0512MCJ064T-I/PT
PIC32MK0512MCJ064T-E/R4X
PIC32MK0512MCJ064T-E/PT
PIC32MK0512MCJ048-E/7MX
PIC32MK0512MCJ048-E/Y8X
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PIC32MK0256GPG048T-E/Y8X
PIC32MK0256MCJ064-E/R4X
PIC32MK0256MCJ064-E/PT
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PIC32MK0256MCJ064-I/PT
PIC32MK0256MCJ064T-I/R4X
PIC32MK0256MCJ064T-I/PT
PIC32MK0256MCJ064T-E/R4X
PIC32MK0256MCJ064T-E/PT

PIC32MK General Purpose and Motor Control GPG/MCJ with CAN FD Family Silicon Errata and Data Sheet Clarifications

PIC32MK (GPG/MCJ) Family Errata

The PIC32MK family of devices that you have received conform functionally to the device data sheet, PIC32MK General Purpose and Motor Control (GPG/MCJ) with CAN FD Family Data Sheet (DS60001570**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the PIC32MK family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. PIC32MK Family Silicon Device Identification

Part Number	Device Identification (DEVID[27:0])	Revision ID (DEVID[31:28])	
		A1	A2
PIC32MK0512MCJ064	0x6300053	0x1	0x2
PIC32MK0512MCJ048	0x6301053		
PIC32MK0256MCJ064	0x6304053		
PIC32MK0256MCJ048	0x6305053		
PIC32MK0512GPG064	0x6318053		
PIC32MK0512GPG048	0x6319053		
PIC32MK0256GPG064	0x631C053		
PIC32MK0256GPG048	0x631D053		

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

Table of Contents

1. Silicon Errata Issues Summary

The following errata issues are to be noted for the current device data sheet, PIC32MK General Purpose and Motor Control (GPG/MCJ) with CAN FD Family (DS60001570**C**).

Table 1-1. Silicon Errata Summary

Module	Feature	Item #	Issue Summary	Affected Revisions	
				A1	A2
Oscillator	Hardware Clock Source Selection	2.1.1	Clock source selection in hardware, that is, using the Fuse Configuration register (FNOSC <2:0> bits (DEVCFG1 <2:0>)) does not work.	X	
ADC	Scan mode	2.2.1	Shared ADC7 on high Offset and Gain Error in Scan mode.	X	
I^2C	Speed	2.3.1	I^2C Host module does not meet low period of the SCL Clock (t_{LOW}) parameter from I^2C specification for clock frequency >= 400 kHz.	X	
I^2C	Client	2.3.2	The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.	X	
FLASH	RTSP	2.4.1	RTSP of Configuration Words is not functional.	X	X

2. Silicon Errata Issues

The following issues apply to the PIC32MK GPG/MCJ family of devices.

Notes:

- An ‘X’ indicates the issue is present in this revision of silicon.
- Cells with a dash (‘-’) indicate that this silicon revision does not exist for this issue.
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

2.1 Oscillator

2.1.1 Hardware Clock Source Selection

After a Brown-out Reset (BOR), the system clock source may default to FRC instead of the clock source defined using the Fuse Configuration register (FNOSC<2:0> bits (DEVCFG1<2:0>)).

Workaround:

Upon any reset, verify if the Current Clock Source Selection register (COSC<2:0> bits (OSCCON<14:12>)) match the clock source selected using the Fuse Configuration register (FNOSC<2:0> bits (DEVCFG1<2:0>)). If the clock sources do not match, perform a software clock switch to the desired clock source. For additional information on software clock switching, refer to Section 42. *Oscillators with Enhanced PLL (DS60001250), subsection 42.3.7.2 Oscillator Switching Sequence* in the “PIC32 Family Reference Manual”.

Affected Revisions:

A1	A2						
X							

2.2 ADC

2.2.1 Scan Mode

Shared ADC 7 has high offset and gain error up to 38 LSb in ADC7 Scan mode, as defined in the ADCCSS1/ ADCCSS2 registers.

Workaround:

Increase the user-defined SMAC<9:0> bits (ADCCON2<25:16>) sample time register value by 4 T_{AD}. This will reduce the ADC7 throughput that the user must consider, but it will reduce the gain and offset to less that 4 LSb in 12-bit mode.

Affected Revisions:

A1	A2						
X							

2.3 I^2C

2.3.1 Speed

The I^2C Host module does not meet low period of the SCL clock (t_{LOW}) parameter from I^2 C specification for clock frequency >= 400 kHz.

Workaround:

None.

Affected Revisions:

A1	A2						
X							

2.3.2 Client

The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.

Workaround:

None

Affected Revisions:

A1	A2						
X							

2.4 Flash

2.4.1 RTSP

Run-Time Self Programming (RTSP) of Configuration Words is not functional.

Workaround:

None

Affected Revisions:

A1	A2						
X	X						

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the current device data sheet, PIC32MK General Purpose and Motor Control (GPG/MCJ) with CAN FD Family (DS60001570**C**), and are showed in **BOLD** type.

Currently there are no known issues to report.

4. Revision History

Revision C - July 2022
The SPI, I^2S, and I^2C standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively. These terms have been updated throughout this document for this revision.

The following silicon errata issues were added:

- FLASH: 2.4.1 RTSP

Revision B - June 2020
Addition of A1 silicon revision.

The following silicon errata issues were added:

- Oscillator: 2.1.1 Hardware Clock Source Selection
- ADC Scan Mode
- I^2C Speed Reference and I^2C Client Reference

Revision A - May 2019
This is the initial released version of this document.

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