



SH1101A

132 X 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller

Preliminary

Features

- Support maximum 132 X 64 dot matrix panel
- Embedded 132 X 64 bits SRAM
- Operating voltage:
 - Logic voltage supply: $V_{DD1} = 2.4V - 3.5V$
 - DC-DC voltage supply: $V_{DD2} = 2.4V - 3.5V$
 - OLED Operating voltage supply: $V_{PP} = 7.0V - 16.0V$
- Maximum segment output current: 320 μ A
- Maximum common sink current: 45mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial peripheral interface
- Programmable frame frequency and multiplexing ratio
- Row re-mapping and column re-mapping (ADC)
- Vertical scrolling
- On-chip oscillator
- Available internal DC-DC converter
- 256-step contrast control on monochrome passive OLED panel
- Low power consumption
 - Sleep mode: <5 μ A
- Wide range of operating temperatures: -40 to +85 $^{\circ}$ C
- Available in COG and TCP form

General Description

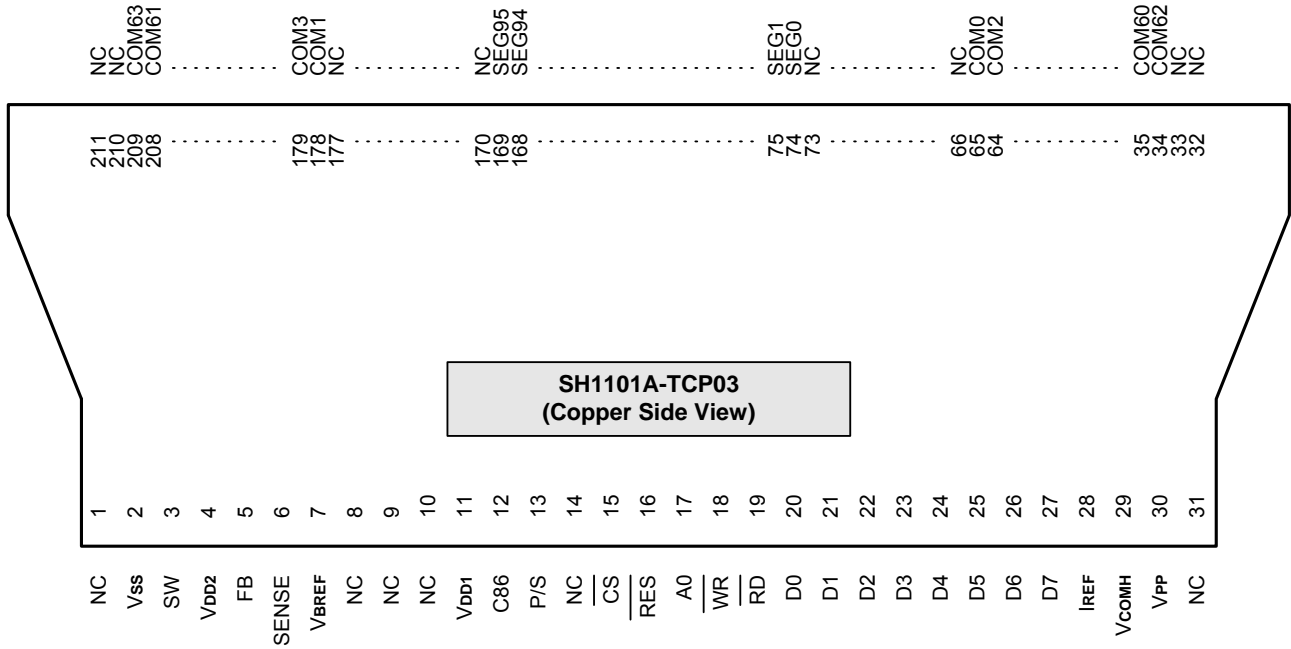
SH1101A is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SH1101A consists of 132 segments, 64 commons that can support a maximum display resolution of 132 X 64. It is designed for Common Cathode type OLED panel.

SH1101A embeds with contrast control, display RAM oscillator and efficient DC-DC converter, which reduces the number of external components and power consumption. SH1101A is suitable for a wide range of compact portable applications, such as sub-display of mobile phone, calculator and MP3 player, etc.

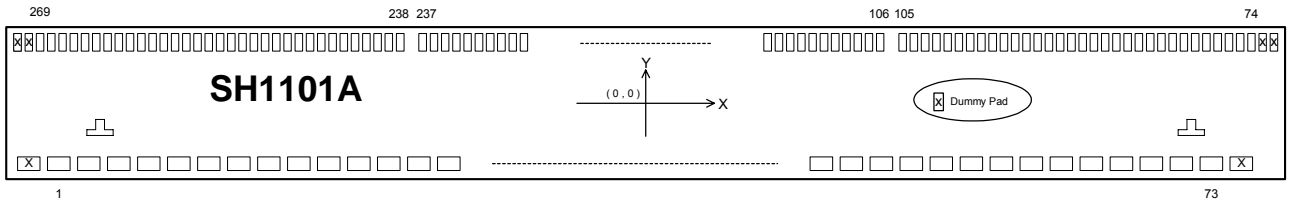


SH1101A

Pin Configuration

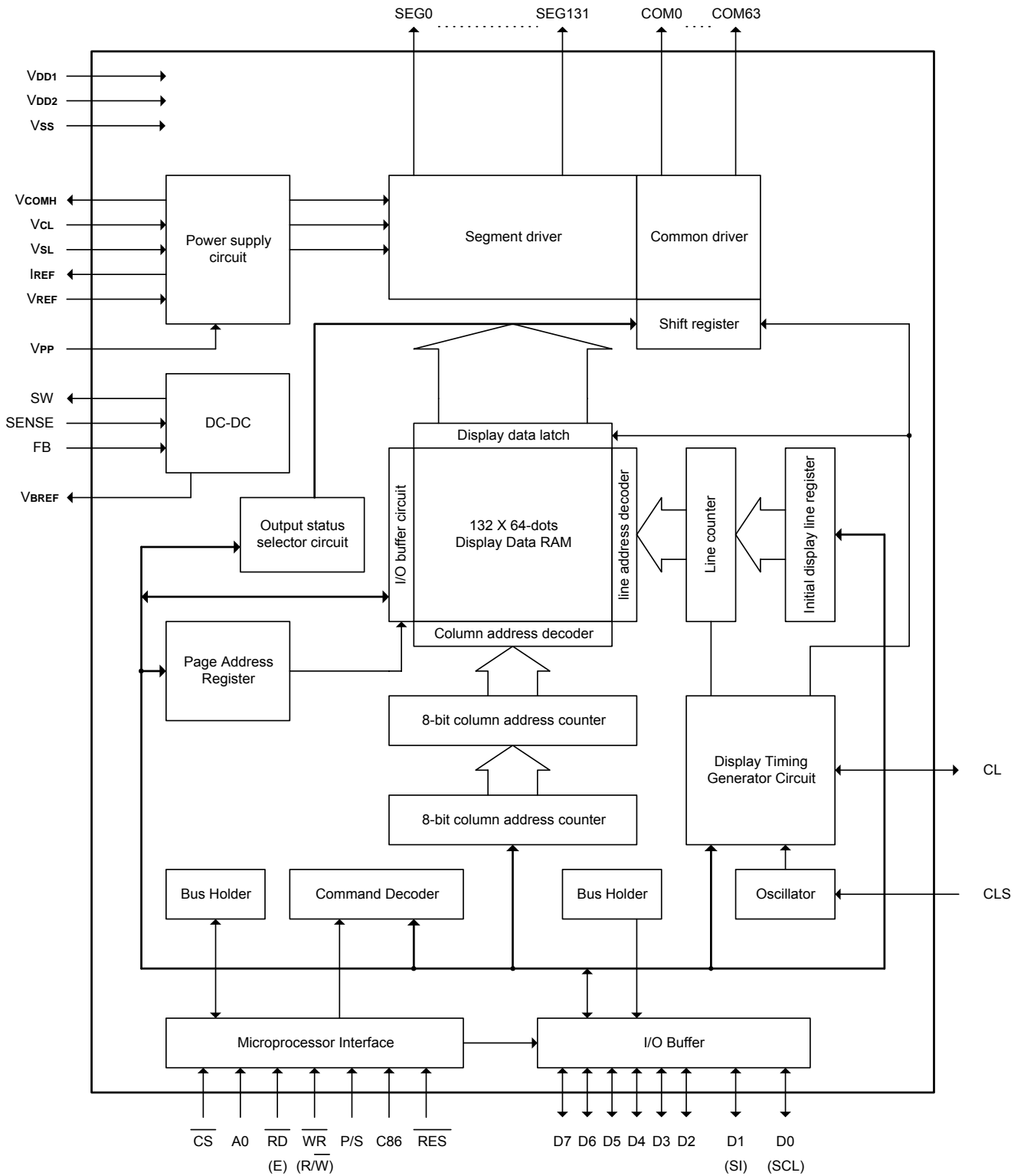


Pad Configuration





Block Diagram



**Pad Description****Power Supply**

| Pad No. | Symbol | I/O | Description |
|--------------------|--------|--------|---|
| 28 - 31 | VDD1 | Supply | 2.4 - 3.5V power supply input. |
| 34,44,62 | VDD1 | Supply | 2.4 - 3.5V power supply output for pad option. |
| 17 - 20 | VDD2 | Supply | 2.4 - 3.5V power supply pad for the internal buffer of the DC-DC voltage converter. |
| 7 - 13 | VSS | Supply | Ground. |
| 21, 32, 36, 42, 64 | VSS | Supply | Ground output for pad option. |
| 49 - 53, 71 - 73 | VPP | Supply | This is the most positive voltage supply pad of the chip. It should be supplied externally. |
| 66 | VPP | Supply | This is the most positive voltage output for pad option, which cannot be used as the most positive voltage input. |
| 4 - 6 | VSL | Supply | This is a segment voltage reference pad. This pad should be connected to VSS externally. |
| 1 - 3 | VCL | Supply | This is a common voltage reference pad. This pad should be connected to VSS externally. |

OLED Driver Supplies

| Pad No. | Symbol | I/O | Description |
|------------------|--------|-----|---|
| 70 | VREF | I | This is a voltage reference pad for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can either be supplied externally or by connecting to VPP. |
| 65 | IREF | O | This is a segment current reference pad. A resistor should be connected between this pad and VSS. Set the current at 10 μ A. |
| 45 - 48, 67 - 69 | VCOMH | O | This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and VSS. |
| 14 - 16 | SW | O | This is an output pad driving the gate of the external NMOS of the booster circuit. |
| 22 | FB | I | This is a feedback resistor input pad for the booster circuit. It is used to adjust the booster output voltage level, VPP. |
| 23 | SENSE | I | This is a source current pad of the external NMOS of the booster circuit. |
| 24 | VBREF | O | This is an internal voltage reference pad for booster circuit. A stabilization capacitor, typical 1 μ F, should be connected to VSS. |



System Bus Connection Pads

| Pad No. | Symbol | I/O | Description | | | | | | | | | | | | |
|---------|---|-------------------------|--|--|-------------------------|-------------------------|------------------|-----|---|---|---|-----|---|---|---|
| 37 | CL | I/O | This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source. | | | | | | | | | | | | |
| 63 | CLS | I | This is the internal clock enable pad. CLS = "H": Internal oscillator circuit is enabled. CLS = "L": Internal oscillator circuit is disabled (requires external input). When CLS = "L", an external clock source must be connected to the CL pad for normal operation. | | | | | | | | | | | | |
| 33 | C86 | I | This is the MPU interface switch pad. C86 = "H": 8080 series MPU interface. C86 = "L": 6800 series MPU interface. | | | | | | | | | | | | |
| 35 | P/S | I | This is the parallel data input/serial data input switch pad. P/S = "H": Parallel data input. P/S = "L": Serial data input. When P/S = "L", D2 to D7 are HZ. D2 to D7 may be "H", "L" or Open. \overline{RD} (E) and \overline{WR} (R/ \overline{W}) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported. These are MPU interface input selection pads. See the following table for selecting different interfaces: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>6800-Parallel Interface</th> <th>8080-Parallel Interface</th> <th>Serial Interface</th> </tr> </thead> <tbody> <tr> <td>C86</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>P/S</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> | | 6800-Parallel Interface | 8080-Parallel Interface | Serial Interface | C86 | 0 | 1 | 0 | P/S | 1 | 1 | 0 |
| | 6800-Parallel Interface | 8080-Parallel Interface | Serial Interface | | | | | | | | | | | | |
| C86 | 0 | 1 | 0 | | | | | | | | | | | | |
| P/S | 1 | 1 | 0 | | | | | | | | | | | | |
| 38 | \overline{CS} | I | This pad is the chip select input. When \overline{CS} = "L", then the chip select becomes active, and data/command I/O is enabled. | | | | | | | | | | | | |
| 39 | \overline{RES} | I | This is a reset signal input pad. When \overline{RES} is set to "L", the settings are initialized. The reset operation is performed by the \overline{RES} signal level. | | | | | | | | | | | | |
| 40 | A0 | I | This is the Data/Command control pad which determines whether the data bits are data or a command. A0 = "H": the inputs at D0 to D7 are treated as display data. A0 = "L": the inputs at D0 to D7 are transferred to the command registers. | | | | | | | | | | | | |
| 41 | \overline{WR} (R/ \overline{W}) | I | This is a MPU interface input pad. When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU \overline{WR} signal. The signals on the data bus are latched at the rising edge of the \overline{WR} signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/ \overline{W} = "H": Read. When R/ \overline{W} = "L": Write. | | | | | | | | | | | | |
| 43 | \overline{RD} (E) | I | This is a MPU interface input pad. When connected to an 8080 series MPU, it is active LOW. This pad is connected to the \overline{RD} signal of the 8080 series MPU, and the SH1101A data bus is in an output status when this signal is "L". When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU. | | | | | | | | | | | | |



System Bus Connection Pads (continued)

| Pad No. | Symbol | I/O | Description |
|---------------------|--------------------------|--------------|--|
| 54 – 61 54 55 | D0 - D7 (SCL) (SI) | I/O | This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance. |

OLED Drive Pads

| Pad No. | Symbol | I/O | Description |
|------------------------|------------|-----|--|
| 105 - 74, 238 - 269 | COM0 - 63 | O | These pads are Common signal output for OLED display. |
| 106 - 237 | SEG0 - 131 | O | These pads are Segment signal output for OLED display. |

Test Pads

| Pad No. | Symbol | I/O | Description |
|---------|--------|-----|---|
| 25 | TEST1 | I | Test pads, internal pull low, no connection for user. |
| 27 | TEST2 | O | Test pads, no connection for user. |
| 26 | TEST3 | I | Test pads, no connection for user. |
| - | NC | - | NC pads, no connection for user. |



Functional Description

Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface or Serial Interface (SPI) can be selected by different selections of C86, P/S as shown in Table 1.

Table. 1

| | 6800-Parallel Interface | 8080-Parallel Interface | Serial Interface |
|-----|-------------------------|-------------------------|------------------|
| C86 | 0 | 1 | 0 |
| P/S | 1 | 1 | 0 |

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), \overline{WR} (R/ \overline{W}), \overline{RD} (E), A0 and \overline{CS} . When \overline{WR} (R/ \overline{W}) = "H", read operation from the display RAM or the status register occurs. When \overline{WR} (R/ \overline{W}) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of A0 input. The \overline{RD} (E) input serves as data latch signal (clock) when it is "H", provided that \overline{CS} = "L" as shown in Table. 2.

Table. 2

| P/S | C86 | Type | \overline{CS} | A0 | \overline{RD} | \overline{WR} | D0 to D7 |
|-----|-----|-------------------------|-----------------|----|-----------------|-------------------|----------|
| 1 | 0 | 6800 microprocessor bus | \overline{CS} | A0 | E | R/ \overline{W} | D0 to D7 |

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processings are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. 1 below.

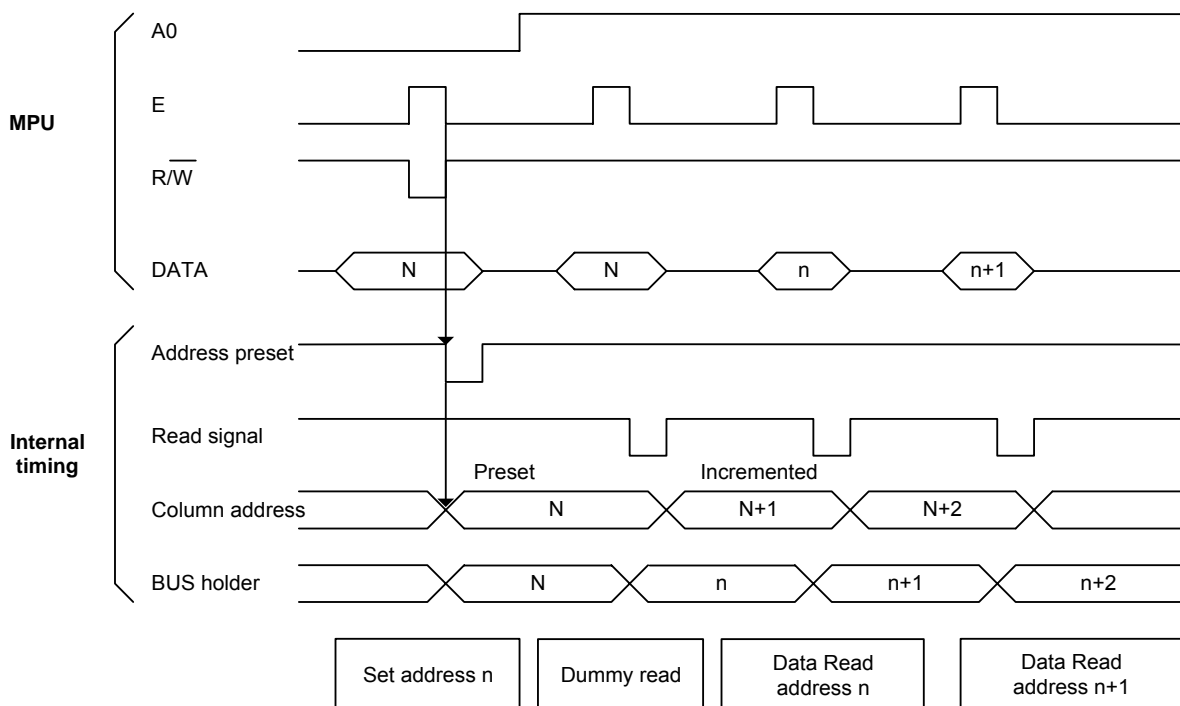


Figure. 1



8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), \overline{WR} (R/ \overline{W}), \overline{RD} (E), A0 and \overline{CS} . The \overline{RD} (E) input serves as data read latch signal (clock) when it is "L" provided that \overline{CS} = "L". Display data or status register read is controlled by A0 signal. The \overline{WR} (R/ \overline{W}) input serves as data write latch signal (clock) when it is "L" and provided that \overline{CS} = "L". Display data or command register write is controlled by A0 as shown in Table. 3.

Table. 3

| P/S | C86 | Type | \overline{CS} | A0 | \overline{RD} | \overline{WR} | D0 to D7 |
|-----|-----|-------------------------|-----------------|----|-----------------|-----------------|----------|
| 1 | 1 | 8080 microprocessor bus | \overline{CS} | A0 | \overline{RD} | \overline{WR} | D0 to D7 |

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

Data Bus Signals

The SH1101A identifies the data bus signal according to A0, \overline{RD} (E) and \overline{WR} (R/ \overline{W}) signals.

Table. 4

| Common | 6800 processor A0 | 8080 processor | | Function | |
|--------|----------------------|----------------------|-----------------|----------|---|
| | | (R/ \overline{W}) | \overline{RD} | | \overline{WR} |
| | 1 | 1 | 0 | 1 | Reads display data. |
| | 1 | 0 | 1 | 0 | Writes display data. |
| | 0 | 1 | 0 | 1 | Reads status. |
| | 0 | 0 | 1 | 0 | Writes control data in internal register. (Command) |



Serial Interface (SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and \overline{CS} . SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM or command register in the same clock. See Figure. 2.

Table. 5

| P/S | C86 | Type | \overline{CS} | A0 | \overline{RD} | \overline{WR} | D0 | D1 | D2 to D7 |
|-----|-----|------------------------|-----------------|----|-----------------|-----------------|-----|----|----------|
| 0 | 0 | Serial Interface (SPI) | \overline{CS} | A0 | - | - | SCL | SI | (HZ) |

Note: “-” Must always be HIGH or LOW.

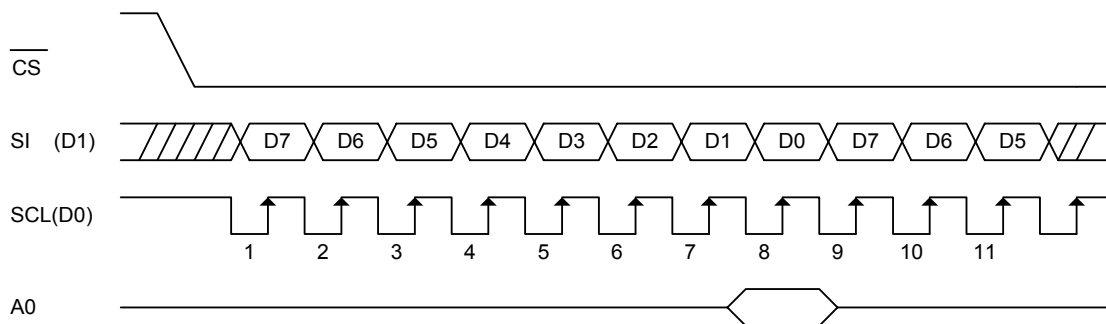


Figure. 2

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = “H”, the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = “L”, the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 X 64 bits. For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software. For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.



The Page Address Circuit

As shown in Figure. 3, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

The Column Address

As shown in Figure. 3, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Because the column address is independent of the page address, when moving, for example, from page0 column 83H to page 1 column 00H, it is necessary to re-specify both the page address and the column address.

Furthermore, as shown in Table. 6, the Column re-mapping (ADC) command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the OLED module is assembled can be minimized.

Table. 6

| Segment Output | SEG0 | SEG131 |
|----------------|----------|-------------------------|
| ADC "0" | 0 (H) → | Column Address → 83 (H) |
| ADC "1" | 83 (H) ← | Column Address ← 0 (H) |

The Line Address Circuit

The line address circuit, as shown in Figure. 3, specifies the line address relating to the common output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for SH1101A, when the common output mode is reversed. The display area is a 64-line area for the SH1101A from the display start line address.

If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. that can be performed relationship between display data RAM and address (if initial display line is 1DH).



The Oscillator Circuit

This is a RC type oscillator (Figure. 4) that produces the display clock. The oscillator circuit is only enabled when CLS = "H". When CLS = "L", the oscillation stops and the display clock is inputted through the CL terminal.

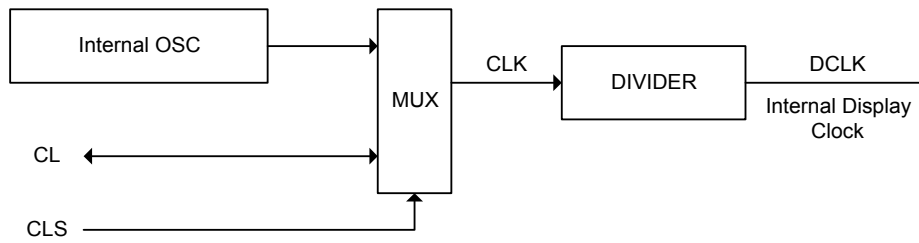


Figure. 4



DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for hand held applications. In SH1101A, built-in DC-DC voltage converter accompanied with an external application circuit (shown in Figure. 5) can generate a high voltage supply V_{PP} from a low voltage supply input V_{DD2} . V_{PP} is the voltage supply to the OLED driver block.

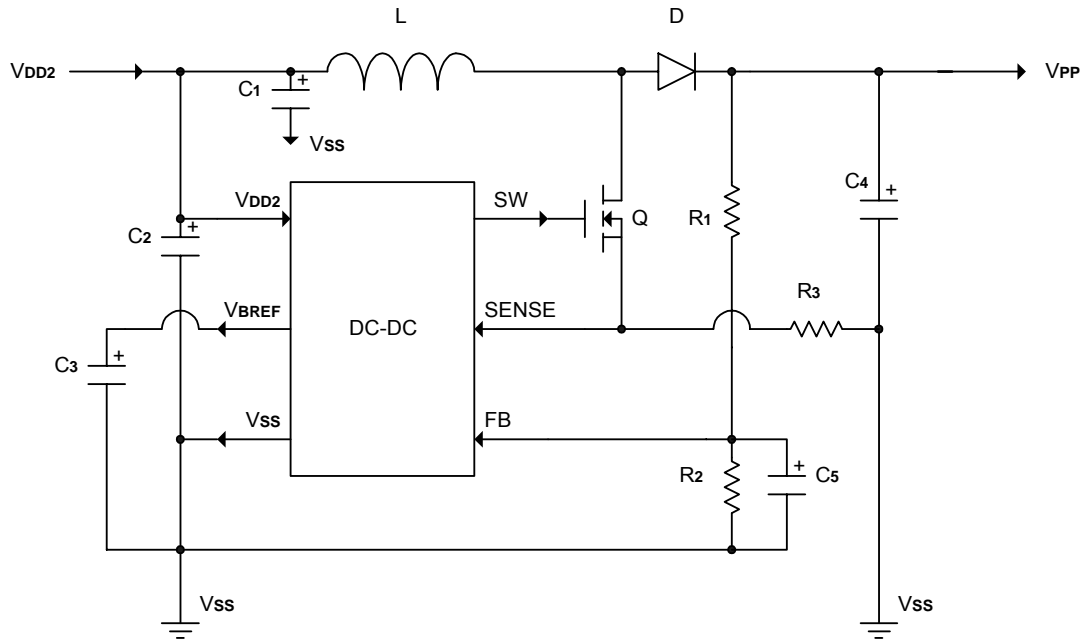


Figure. 5

$$V_{PP} = \left(1 + \frac{R1}{R2}\right) \times V_{BREF}, (R2: 80 - 120k\Omega)$$

Current Control and Voltage Control

This block is used to derive the incoming power sources into different levels of internal use voltage and current. V_{PP} and V_{DD2} are external power supplies. V_{REF} , a reference voltage, which is used to derive the driving voltage for segments and commons. I_{REF} is a reference current source for segment current drivers.

Common Drivers/Segment Drivers

Segment drivers deliver 132 current sources to drive OLED panel. The driving current can be adjusted up to 320µA with 256 steps. Common drivers generate voltage scanning pulses.



Reset Circuit

When the $\overline{\text{RES}}$ input falls to “L”, these reenter their default state. The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 132 X 64 Display mode
3. Normal segment and display data column address and row address mapping (SEG0 is mapped to column address 00H and COM0 mapped to row address 00H).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM line address 00H.
6. Column address counter is set at 0.
7. Normal scanning direction of the common outputs.
8. Contrast control register is set at 80H.
9. Internal DC-DC is selected.



Commands

The SH1101A uses a combination of A0, \overline{RD} (E) and \overline{WR} (R/ \overline{W}) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the \overline{RD} pad and a write status when a low pulse is input to the \overline{WR} pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/ \overline{W} pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, \overline{RD} (E) becomes 1(HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Set Lower Column Address: (00H - 0FH)
2. Set Higher Column Address: (10H - 1FH)

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 132 is accessed. The page address is not changed during this time.

| | A0 | E \overline{RD} | R/ \overline{W} \overline{WR} | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----|----------------------|--------------------------------------|----|----|----|----|----|----|----|----|
| Higher bits | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A7 | A6 | A5 | A4 |
| Lower bits | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A3 | A2 | A1 | A0 |

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Line address |
|----|----|----|----|----|----|----|----|--------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | : | | | | | : |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 131 |

Note: Don't use any commands not mentioned above.

3~5. Reserved Command

These three commands are reserved for user.



6. Set Display Start Line: (40H - 7FH)

Specifies line address (refer to Figure. 3) to determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{\overline{WR}}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|--|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 0 | 1 | A5 | A4 | A3 | A2 | A1 | A0 |

| A5 | A4 | A3 | A2 | A1 | A0 | Line address |
|----|----|----|----|----|----|--------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | : | | | : |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |



7. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: $I_{SEG} = \alpha/256 \times I_{REF} \times \text{scale factor}$

Where: α is contrast step; I_{REF} is reference current equals 10 μ A; Scale factor = 32.

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

■ Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | I _{SEG} |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|------------------|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Small |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | | | | | : | | | | : |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | POR |
| 0 | 1 | 0 | | | | | : | | | | : |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Large |

When the contrast control function is not used, set the D7 - D0 to 1000,0000.

8. Set Segment Re-map: (A0H - A1H)

Change the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the column address section of Figure. 3. When display data is written or read, the column address is incremented by 1 as shown in Figure. 1.

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|-----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | ADC |

When ADC = "L", the right rotates (normal direction). (POR)

When ADC = "H", the left rotates (reverse direction).

9. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D |

When D = "L", the normal display status is provided. (POR)

When D = "H", the entire display ON status is provided.



10. Set Normal/Reverse Display: (A6H -A7H)

Reverses the display ON/OFF status without rewriting the contents of the display data RAM.

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D |

When D = "L", the RAM data is high, being OLED ON potential (normal display). (POR)

When D = "H", the RAM data is low, being OLED ON potential (reverse display)

11. Set Multiplex Ratio: (Double Bytes Command)

This command switches default 64 multiplex modes to any multiplex ratio from 1 to 64. The output pads COM0-COM63 will be switched to corresponding common signal.

■ Multiplex Ratio Mode Set: (A8H)

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

■ Multiplex Ratio Data Set: (00H - 3FH)

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Multiplex Ratio |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|-----------------|
| 0 | 1 | 0 | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | * | * | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | * | * | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | | | | | : | | | | : |
| 0 | 1 | 0 | * | * | 1 | 1 | 1 | 1 | 1 | 0 | 63 |
| 0 | 1 | 0 | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 64 (POR) |

12. Set DC-DC OFF/ON: (Double Bytes Command)

This command is to control the DC-DC voltage converter. The converter will be turned on by issuing this command then display ON command. The panel display must be off while issuing this command.

■ DC-DC Control Mode Set: (ADH)

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

■ DC-DC ON/OFF Mode Set: (8AH - 8BH)

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | D |

When D = "L", DC-DC is disable.

When D = "H", DC-DC will be turned on when display on. (POR)

Table. 7

| DC-DC STATUS | DISPLAY ON/OFF STATUS | Description |
|--------------|-----------------------|--|
| 0 | 0 | Sleep mode |
| 0 | 1 | External VPP must be used. |
| 1 | 0 | Sleep mode |
| 1 | 1 | Built-in DC-DC is used, Normal Display |



13. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{\overline{WR}}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|--|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D |

When D = "L", Display OFF OLED. (POR)

When D = "H", Display ON OLED.

When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

- (1) Stops the oscillator circuit and DC-DC circuit.
- (2) Stops the OLED drive and outputs HZ as the segment/common driver output.
- (3) Holds the display data and operation mode provided before the start of the sleep mode.
- (4) The MPU can access to the built-in display RAM.

14. Set Page Address: (B0H - B7H)

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed.

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{\overline{WR}}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|--|----|----|----|----|----------------|----------------|----------------|----------------|
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | A ₃ | A ₂ | A ₁ | A ₀ |

| A ₃ | A ₂ | A ₁ | A ₀ | Page address |
|----------------|----------------|----------------|----------------|--------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |

Note: Don't use any commands not mentioned above for user.



15. Set Common Output Scan Direction: (C0H - C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | D | * | * | * |

When D = "L", Scan from COM0 to COM [N -1]. (POR)

When D = "H", Scan from COM [N -1] to COM0.

16. Set Display Offset: (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-63 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (64-16), so the second byte should be 100000.

■ Display Offset Mode Set: (D3H)

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

■ Display Offset Data Set: (00H~3FH)

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | COMx |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|---------|
| 0 | 1 | 0 | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 (POR) |
| 0 | 1 | 0 | * | * | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | * | * | 0 | 0 | 0 | 0 | 1 | 1 | 2 |
| 0 | 1 | 0 | | | | | : | | | | : |
| 0 | 1 | 0 | * | * | 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 0 | 1 | 0 | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 63 |

Note: "*" stands for "Don't care"



17. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

■ Divide Ratio/Oscillator Frequency Mode Set: (D5H)

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

■ Divide Ratio/Oscillator Frequency Data Set: (00H - 3FH)

| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------|-----------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A3 - A0 defines the divide ration of the display clocks (DCLK). Divide Ratio = A[3:0]+1.

| A3 | A2 | A1 | A0 | Divide Ratio |
|----|----|----|----|--------------|
| 0 | 0 | 0 | 0 | 1 (POR) |
| | | : | | : |
| 1 | 1 | 1 | 1 | 16 |

A7 - A4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

| A7 | A6 | A5 | A4 | Oscillator Frequency of f_{osc} |
|----|----|----|----|-----------------------------------|
| 0 | 0 | 0 | 0 | -25% |
| 0 | 0 | 0 | 1 | -20% |
| 0 | 0 | 1 | 0 | -15% |
| 0 | 0 | 1 | 1 | -10% |
| 0 | 1 | 0 | 0 | -5% |
| 0 | 1 | 0 | 1 | f_{osc} (POR) |
| 0 | 1 | 1 | 0 | +5% |
| 0 | 1 | 1 | 1 | +10% |
| 1 | 0 | 0 | 0 | +15% |
| 1 | 0 | 0 | 1 | +20% |
| 1 | 0 | 1 | 0 | +25% |
| 1 | 0 | 1 | 1 | +30% |
| 1 | 1 | 0 | 0 | +35% |
| 1 | 1 | 0 | 1 | +40% |
| 1 | 1 | 1 | 0 | +45% |
| 1 | 1 | 1 | 1 | +50% |



18. Set Dis-charge/Pre-charge Period: (Double Bytes Command)

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK. POR is 2 DCLKs.

■ Pre-charge Period Mode Set: (D9H)

| | | | | | | | | | | |
|----|----------------|--|----|----|----|----|----|----|----|----|
| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{\overline{WR}}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |

■ Dis-charge/Pre-charge Period Data Set: (00H - FFH)

| | | | | | | | | | | |
|----|----------------|--|----|----|----|----|----|----|----|----|
| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{\overline{WR}}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

Pre-charge Period Adjust: (A3 - A0)

| A3 | A2 | A1 | A0 | Pre-charge Period |
|----|----|----|----|-------------------|
| 0 | 0 | 0 | 0 | INVALID |
| 0 | 0 | 0 | 1 | 1 DCLKs |
| 0 | 0 | 1 | 0 | 2 DCLKs (POR) |
| | | : | | : |
| 1 | 1 | 1 | 0 | 14 DCLKs |
| 1 | 1 | 1 | 1 | 15 DCLKs |

Dis-charge Period Adjust: (A7 - A4)

| A7 | A6 | A5 | A4 | Dis-charge Period |
|----|----|----|----|-------------------|
| 0 | 0 | 0 | 0 | INVALID |
| 0 | 0 | 0 | 1 | 1 DCLKs |
| 0 | 0 | 1 | 0 | 2 DCLKs (POR) |
| | | : | | : |
| 1 | 1 | 1 | 0 | 14 DCLKs |
| 1 | 1 | 1 | 1 | 15 DCLKs |

19. Set Common pads hardware configuration: (Double Bytes Command)

This command is to set the common signals pad configuration (sequential or alternative) to match the OLED panel hardware layout

■ Common Pads Hardware Configuration Mode Set: (DAH)

| | | | | | | | | | | |
|----|----------------|--|----|----|----|----|----|----|----|----|
| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{\overline{WR}}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

■ Sequential/Alternative Mode Set: (02H - 12H)

| | | | | | | | | | | |
|----|----------------|--|----|----|----|----|----|----|----|----|
| A0 | $\frac{E}{RD}$ | $\frac{R/\overline{W}}{\overline{WR}}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 0 | 0 | D | 0 | 0 | 1 | 0 |

When D = "L", Sequential.

| | | |
|------------------|--------------------|--------------------|
| COM31, 30 - 1, 0 | SEG0, 1 - 130, 131 | COM32, 33 - 62, 63 |
|------------------|--------------------|--------------------|

When D = "H", Alternative. (POR)

| | | |
|------------------|--------------------|------------------|
| COM62, 60 - 2, 0 | SEG0, 1 - 130, 131 | COM1, 3 - 61, 63 |
|------------------|--------------------|------------------|



20. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

■ VCOM Deselect Level Mode Set: (DBH)

| | | | | | | | | | | |
|----|-----------------------------------|-------------------------------------|----|----|----|----|----|----|----|----|
| A0 | \overline{E} \overline{RD} | $\overline{R/W}$ \overline{WR} | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |

■ VCOM Deselect Level Data Set: (00H - FFH)

| | | | | | | | | | | |
|----|-----------------------------------|-------------------------------------|----|----|----|----|----|----|----|----|
| A0 | \overline{E} \overline{RD} | $\overline{R/W}$ \overline{WR} | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

$$V_{COM} = \beta \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$$

| A[7:0] | β | A[7:0] | β |
|-----------|-------------|--------|-------------|
| 00H | 0.430 | 20H | 0.770 (POR) |
| 01H | | | |
| 02H | | | |
| 03H | | | |
| 04H | | | |
| 05H | | | |
| 06H | | | |
| 07H | | | |
| 08H | | | |
| 09H | | | |
| 0AH | | | |
| 0BH | | | |
| 0CH | | | |
| 0DH | | | |
| 0EH | | | |
| 0FH | | | |
| 10H | 0.770 (POR) | 30H | |
| 11H | | | |
| 12H | | | |
| 13H | | | |
| 14H | | | |
| 15H | | | |
| 16H | | | |
| 17H | | | |
| 18H | | | |
| 19H | | | |
| 1AH | | | |
| 1BH | | | |
| 1CH | | | |
| 1DH | | | |
| 1EH | | | |
| 1FH | | | |
| 40H - FFH | 1 | | |



21. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. Once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

| A0 | \overline{E} RD | $\overline{R/W}$ WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------------|------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

Cursor display sequence:

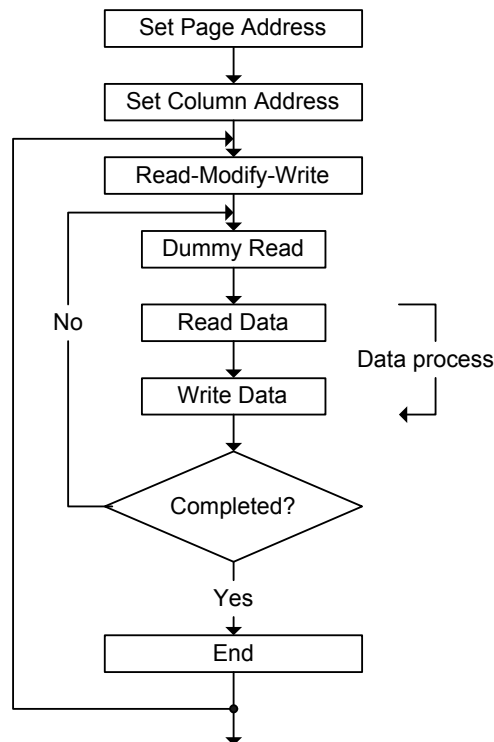


Figure. 6

22. End: (EEH)

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued.)

| A0 | \overline{E} RD | $\overline{R/W}$ WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------------|------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

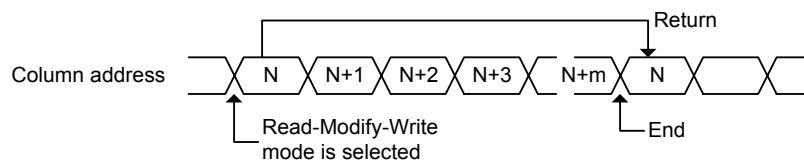


Figure. 7



23. NOP: (E3H)

Non-Operation Command.

| A0 | \overline{E} RD | $\overline{R/W}$ WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------------|------------------------|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

24. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

| A0 | \overline{E} RD | $\overline{R/W}$ WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------------|------------------------|----------------|----|----|----|----|----|----|----|
| 1 | 1 | 0 | Write RAM data | | | | | | | |

25. Read Status

| A0 | \overline{E} RD | $\overline{R/W}$ WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------------|------------------------|------|--------|----|----|----|----|----|----|
| 0 | 0 | 1 | BUSY | ON/OFF | * | * | * | 0 | 0 | 0 |

BUSY: When high, the SH1101A is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ON/OFF: Indicates whether the display is on or off. When goes low the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

26. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

| A0 | \overline{E} RD | $\overline{R/W}$ WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------------------|------------------------|---------------|----|----|----|----|----|----|----|
| 1 | 0 | 1 | Read RAM data | | | | | | | |



Command Table

| Command | Code | | | | | | | | | | | Function | |
|--|------|----|----|---------------|----|-----------------|----|-----------------------|----|----|----|----------|--|
| | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 1. Set Column Address 4 lower bits | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Lower column address | | | | 0 | Sets 4 lower bits of column address of display RAM in register. (POR = 00H) |
| 2. Set Column Address 4 higher bits | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Higher column address | | | | 0 | Sets 4 higher bits of column address of display RAM in register. (POR = 10H) |
| 3. Reserved Command | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Reserved |
| 4. Reserved Command | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | Reserved |
| 5. Reserved Command | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | D | 0 | Reserved |
| 6. Set Display Start Line | 0 | 1 | 0 | 0 | 1 | Line address | | | | | 0 | 0 | Specifies RAM display line for COM0. (POR = 40H) |
| 7. The Contrast Control Mode Set | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H) |
| Contrast Data Register Set | 0 | 1 | 0 | Contrast Data | | | | | | | 0 | 0 | |
| 8. Set Segment Re-map (ADC) | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | ADC | The right (0) or left (1) rotation. (POR = A0H) |
| 9. Set Entire Display OFF/ON | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | D | Selects normal display (0) or Entire Display ON (1). (POR = A4H) |
| 10. Set Normal/Reverse Display | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | D | Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H) |
| 11. Multiplex Ration Mode Set | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | This command switches default 63 multiplex mode to any multiplex ratio from 1 to 64. (POR = 3FH) |
| Multiplex Ration Data Set | 0 | 1 | 0 | * | * | Multiplex Ratio | | | | | 0 | 0 | |
| 12. DC-DC Control Mode Set | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 8BH) |
| DC-DC ON/OFF Mode Set | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | D | 0 | |



Command Table (Continued)

| Command | Code | | | | | | | | | | | Function |
|--|------|----|----|---------------------------------|--------|------|----|-------------------|----|----|----|--|
| | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 13. Display OFF/ON | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D | Turns on OLED panel (1) or turns off (0). (POR = AEH) |
| 14. Set Page Address | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Page Address | | | | Specifies page address to load display RAM data to page address register. (POR = B0H) |
| 15. Set Common Output Scan Direction | 0 | 1 | 0 | 1 | 1 | 0 | 0 | D | * | * | * | Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H) |
| 16. Display Offset Mode Set | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | This is a double byte command which specifies the mapping of display start line to one of COM0-63. (POR = 00H) |
| Display Offset Data Set | 0 | 1 | 0 | * | * | COMx | | | | | | |
| 17. Set Display Divide Ratio/Oscillator Frequency Mode Set | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | This command is used to set the frequency of the internal display clocks. (POR = 50H) |
| Divide Ratio/Oscillator Frequency Data Set | 0 | 1 | 0 | Oscillator Frequency | | | | Divide Ratio | | | | |
| 18. Dis-charge / Pre-charge Period Mode Set | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H) |
| Dis-charge /Pre-charge Period Data Set | 0 | 1 | 0 | Dis-charge Period | | | | Pre-charge Period | | | | |
| 19. Common Pads Hardware Configuration Mode Set | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | This command is to set the common signals pad configuration. (POR = 12H) |
| Sequential/Alternative Mode Set | 0 | 1 | 0 | 0 | 0 | 0 | D | 0 | 0 | 1 | 0 | |
| 20. VCOM Deselect Level Mode Set | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | This command is to set the common pad output voltage level at deselect stage. (POR = 35H) |
| VCOM Deselect Level Data Set | 0 | 1 | 0 | VCOM ($\beta \times V_{REF}$) | | | | | | | | |
| 21. Read-Modify-Write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Read-Modify-Write start. |
| 22. End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Read-Modify-Write end. |
| 23. NOP | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Non-Operation Command |
| 24. Write Display Data | 1 | 1 | 0 | Write RAM data | | | | | | | | |
| 25. Read Status | 0 | 0 | 1 | BUSY | ON/OFF | * | * | * | 0 | 0 | 0 | |
| 26. Read Display Data | 1 | 0 | 1 | Read RAM data | | | | | | | | |

Note: Do not use any other command, or the system malfunction may result.

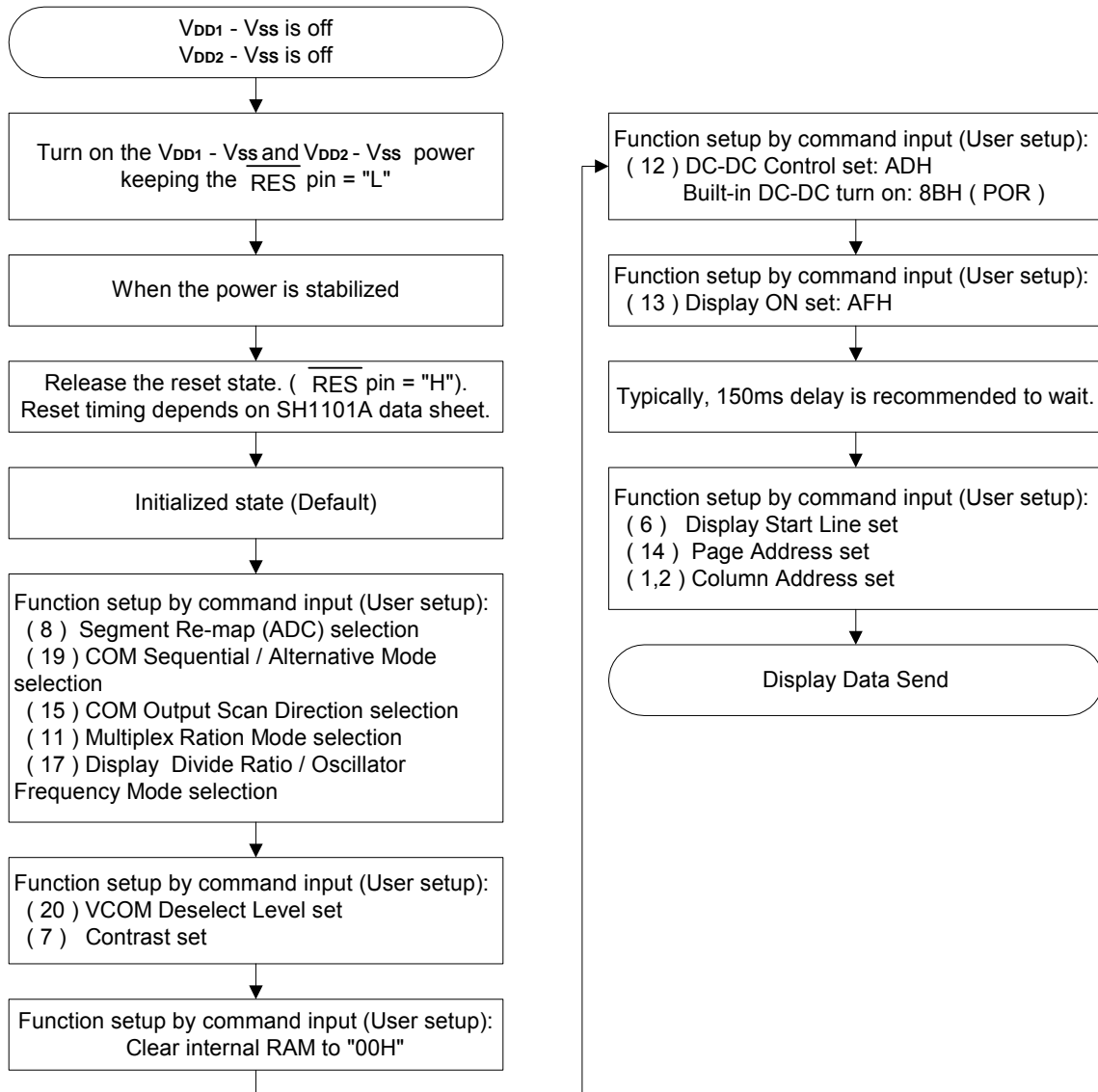


Command Description

Instruction Setup: Reference

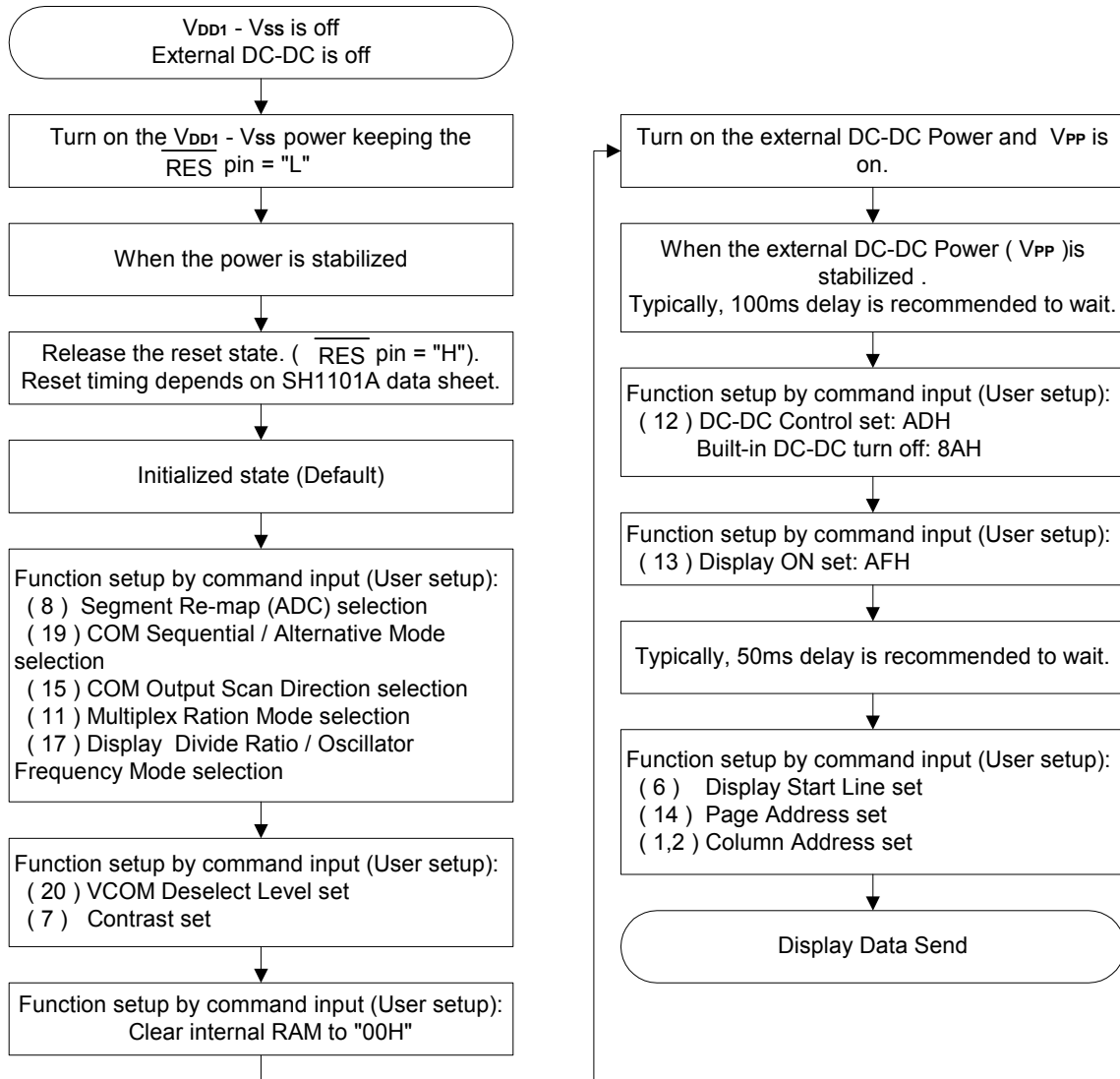
1. Power On and Initialization

1.1. When the built-in DC-DC pump power is being used immediately after turning on the power:



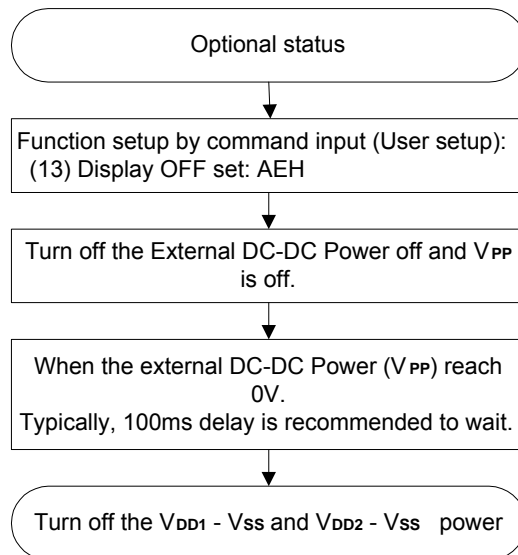


1.2. When the external DC-DC pump power is being used immediately after turning on the power:





2. Power Off





Absolute Maximum Rating*

DC Supply Voltage (VDD1, VDD2) -0.3V to +3.6V
 DC Supply Voltage (VPP) -0.3V to +18V
 Input Voltage -0.3V to VDD1 + 0.3V
 Operating Ambient Temperature -40°C to +85°C
 Storage Temperature -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (VSS = 0V, VDD1 = 2.4 - 3.5V TA = +25°C, unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|---|------|------|------|------|---|
| VDD1 | Operating voltage | 2.4 | - | 3.5 | V | |
| VDD2 | Operating voltage | 2.4 | - | 3.5 | V | |
| VPP | OLED Operating voltage | 7.0 | - | 16.0 | V | |
| VBREF | Internal voltage reference | 1.20 | 1.26 | 1.32 | V | With one 1μF capacitor |
| IDD1 | Dynamic current consumption 1 | - | 110 | 160 | μA | VDD1 = 3V, VDD2 = 3V, IREF = 10μA, Contrast α = 256, Bulid-in DC-DC OFF, Display ON, display data = All ON, No panel attached. |
| IDD2 | Dynamic current consumption 2 | - | 190 | 285 | μA | VDD1 = 3V, VDD2 = 3V, VPP = 12V, IREF = -10μA, Contrast α = 256, Bulid-in DC-DC ON, Display ON, Display data = All ON, No panel attached. |
| IPP | OLED dynamic current consumption | - | 550 | 825 | μA | VDD1 = 3V, VDD2 = 3V, VPP = 12V, IREF = -10μA, Contrast α = 256, Display ON, All ON, No panel attached. |
| ISP | Sleep mode current consumption in VDD1 & VDD2 | - | 0.01 | 5 | μA | During sleep, TA = +25°C, VDD1 = 3V, VDD2 = 3V. |
| | Sleep mode current consumption in VPP | - | 0.01 | 5 | μA | During sleep, TA = +25°C, VPP = 12V. |
| ISEG | Segment output current | -308 | -320 | -342 | μA | VDD1 = 3V, VPP = 12V, IREF = -10μA, RLOAD = 20kΩ, Display ON. Contrast α = 256. |
| | | - | -220 | - | μA | VDD1 = 3V, VPP = 12V, IREF = -10μA, RLOAD = 20kΩ, Display ON. Contrast α = 176. |
| | | - | -120 | - | μA | VDD1 = 3V, VPP = 12V, IREF = -10μA, RLOAD = 20kΩ, Display ON. Contrast α = 96. |
| | | - | -20 | - | μA | VDD1 = 3V, VPP = 12V, IREF = -10μA, RLOAD = 20kΩ, Display ON. Contrast α = 16. |
| ΔISEG1 | Segment output current uniformity | - | - | ±3 | % | ΔISEG1 = (ISEG - IMID)/IMID X 100% IMID = (IMAX + IMIN)/2 ISEG [0:131] at contrast α = 256. |
| ΔISEG2 | Adjacent segment output current uniformity | - | - | ±2 | % | ΔISEG2 = (ISEG [N] - ISEG [N+1])/(ISEG [N] + ISEG [N+1]) X 100% ISEG [0:131] at contrast α = 256. |



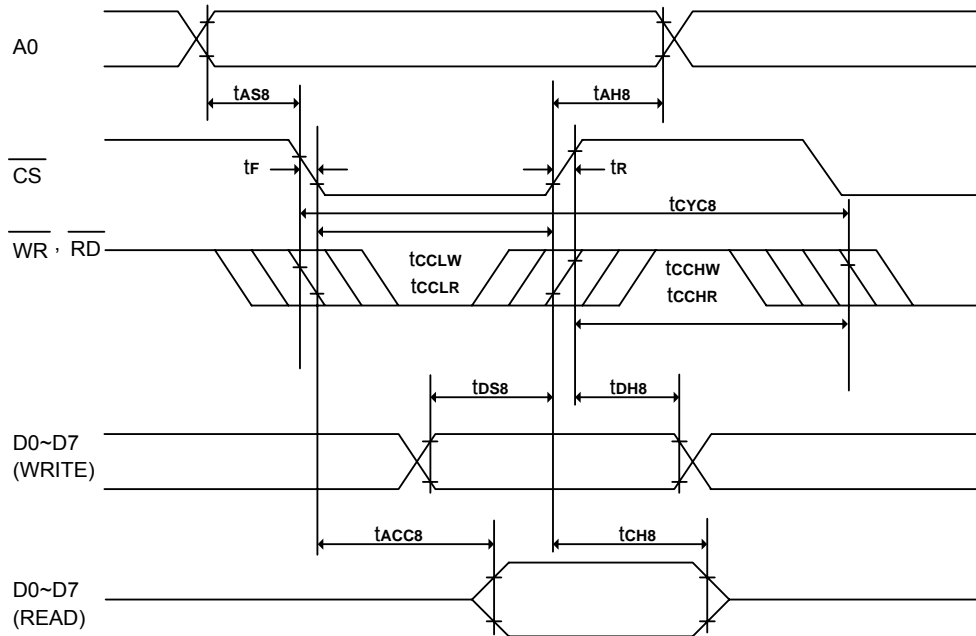
DC Characteristics (Continued)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|------------------|--------------------------------|------------------------|------|------------------------|------|---|
| V _{IHC} | High-level input voltage | 0.8 X V _{DD1} | - | V _{DD1} | V | A0, D0 - D7, \overline{RD} (E), \overline{WR} (R/ \overline{W}), \overline{CS} , CLS, CL, C86, P/S and \overline{RES} . |
| V _{ILC} | Low-level input voltage | V _{SS} | - | 0.2 X V _{DD1} | V | |
| V _{OHC} | High-level output voltage | 0.8 X V _{DD1} | - | V _{DD1} | V | I _{OH} = -0.5mA (D0 - D7, and CL). |
| V _{OLC} | Low-level output voltage | V _{SS} | - | 0.2 X V _{DD1} | V | I _{OL} = 0.5mA (D0 - D7, and CL). |
| I _{LI} | Input leakage current | -1.0 | - | 1.0 | μA | V _{IN} = V _{DD1} or V _{SS} (A0, \overline{RD} (E), \overline{WR} (R/ \overline{W}), \overline{CS} , CLS, C86, P/S and \overline{RES}). |
| I _{HZ} | HZ leakage current | -1.0 | - | 1.0 | μA | When the D0 - D7, and CL are in high impedance. |
| f _{osc} | Oscillation frequency | 315 | 360 | 420 | kHz | T _A = +25°C. |
| f _{FRM} | Frame frequency for 64 Commons | - | 104 | - | Hz | When f _{osc} = 360kHz, Divide ratio = 1, common width = 54 DCLKs. |



AC Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)

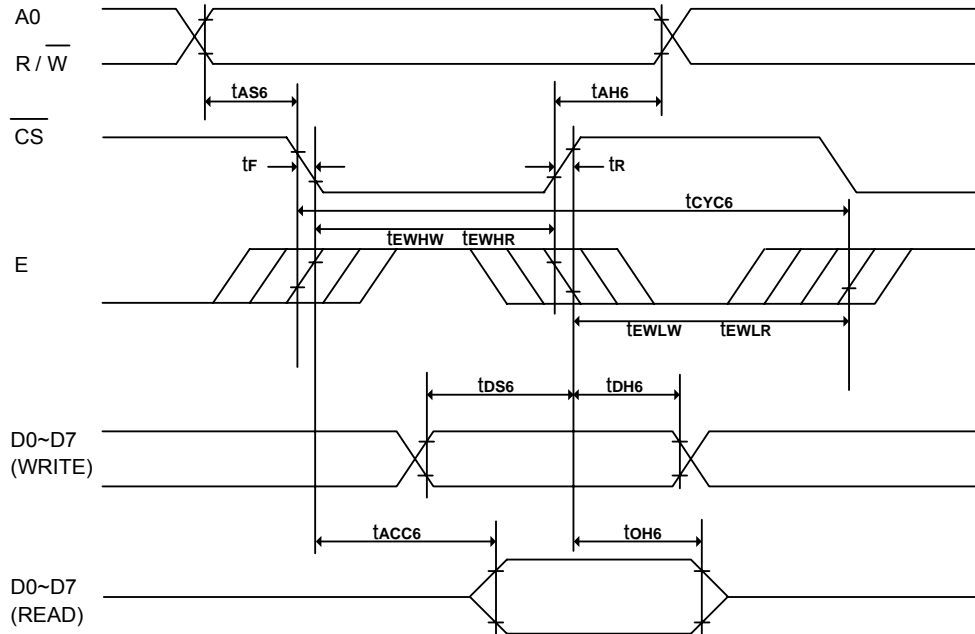


(VDD1 = 2.4 - 3.5V, TA = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|-----------------------------|------|------|------|------|------------|
| tCYC8 | System cycle time | 300 | - | - | ns | |
| tAS8 | Address setup time | 0 | - | - | ns | |
| tAH8 | Address hold time | 0 | - | - | ns | |
| tDS8 | Data setup time | 40 | - | - | ns | |
| tDH8 | Data hold time | 15 | - | - | ns | |
| tCH8 | Output disable time | 10 | - | 70 | ns | CL = 100pF |
| tACC8 | \overline{RD} access time | - | - | 140 | ns | CL = 100pF |
| tCCLW | Control L pulse width (WR) | 100 | - | - | ns | |
| tCCLR | Control L pulse width (RD) | 120 | - | - | ns | |
| tCCHW | Control H pulse width (WR) | 100 | - | - | ns | |
| tCCHR | Control H pulse width (RD) | 100 | - | - | ns | |
| tR | Rise time | - | - | 15 | ns | |
| tF | Fall time | - | - | 15 | ns | |



(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)

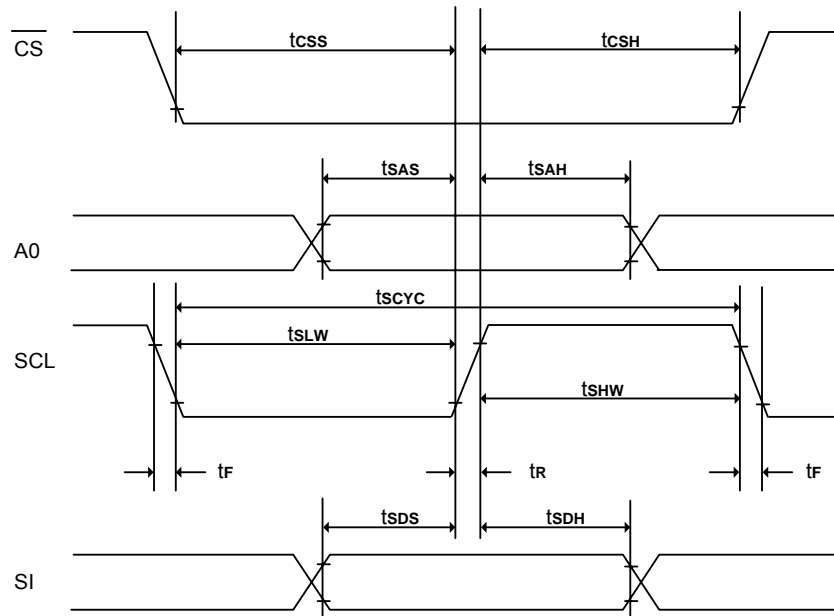


(VDD1 = 2.4 - 3.5V, TA = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|------------------------------|------|------|------|------|------------|
| tCYC6 | System cycle time | 300 | - | - | ns | |
| tAS6 | Address setup time | 0 | - | - | ns | |
| tAH6 | Address hold time | 0 | - | - | ns | |
| tDS6 | Data setup time | 40 | - | - | ns | |
| tDH6 | Data hold time | 15 | - | - | ns | |
| tOH6 | Output disable time | 10 | - | 70 | ns | CL = 100pF |
| tACC6 | Access time | - | - | 140 | ns | CL = 100pF |
| tEWHW | Enable H pulse width (Write) | 100 | - | - | ns | |
| tEWHR | Enable H pulse width (Read) | 120 | - | - | ns | |
| tEWLW | Enable L pulse width (Write) | 100 | - | - | ns | |
| tEWLR | Enable L pulse width (Read) | 100 | - | - | ns | |
| tR | Rise time | - | - | 15 | ns | |
| tF | Fall time | - | - | 15 | ns | |



(3) System buses Write characteristics 3(For the Serial Interface MPU)

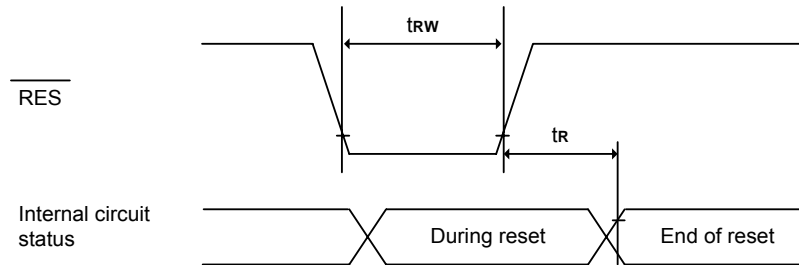


(VDD1 = 2.4 - 3.5V, TA = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|----------------------------|------|------|------|------|-----------|
| tscyc | Serial clock cycle | 250 | - | - | ns | |
| tsAS | Address setup time | 150 | - | - | ns | |
| tsAH | Address hold time | 150 | - | - | ns | |
| tsds | Data setup time | 100 | - | - | ns | |
| tsdH | Data hold time | 100 | - | - | ns | |
| tcss | \overline{CS} setup time | 120 | - | - | ns | |
| tcsH | \overline{CS} hold time | 60 | - | - | ns | |
| tshw | Serial clock H pulse width | 100 | - | - | ns | |
| tslw | Serial clock L pulse width | 100 | - | - | ns | |
| tr | Rise time | - | - | 15 | ns | |
| tf | Fall time | - | - | 15 | ns | |



(4) Reset Timing



(VDD1 = 2.4 - 3.5V, TA = +25°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|--------|-----------------------|------|------|------|------|-----------|
| tR | Reset time | - | - | 1.0 | μs | |
| tRW | Reset low pulse width | 5.0 | - | - | μs | |



Application Circuit (for reference only)

Reference Connection to MPU:

1. 8080 series interface: (Internal oscillator, External VPP)

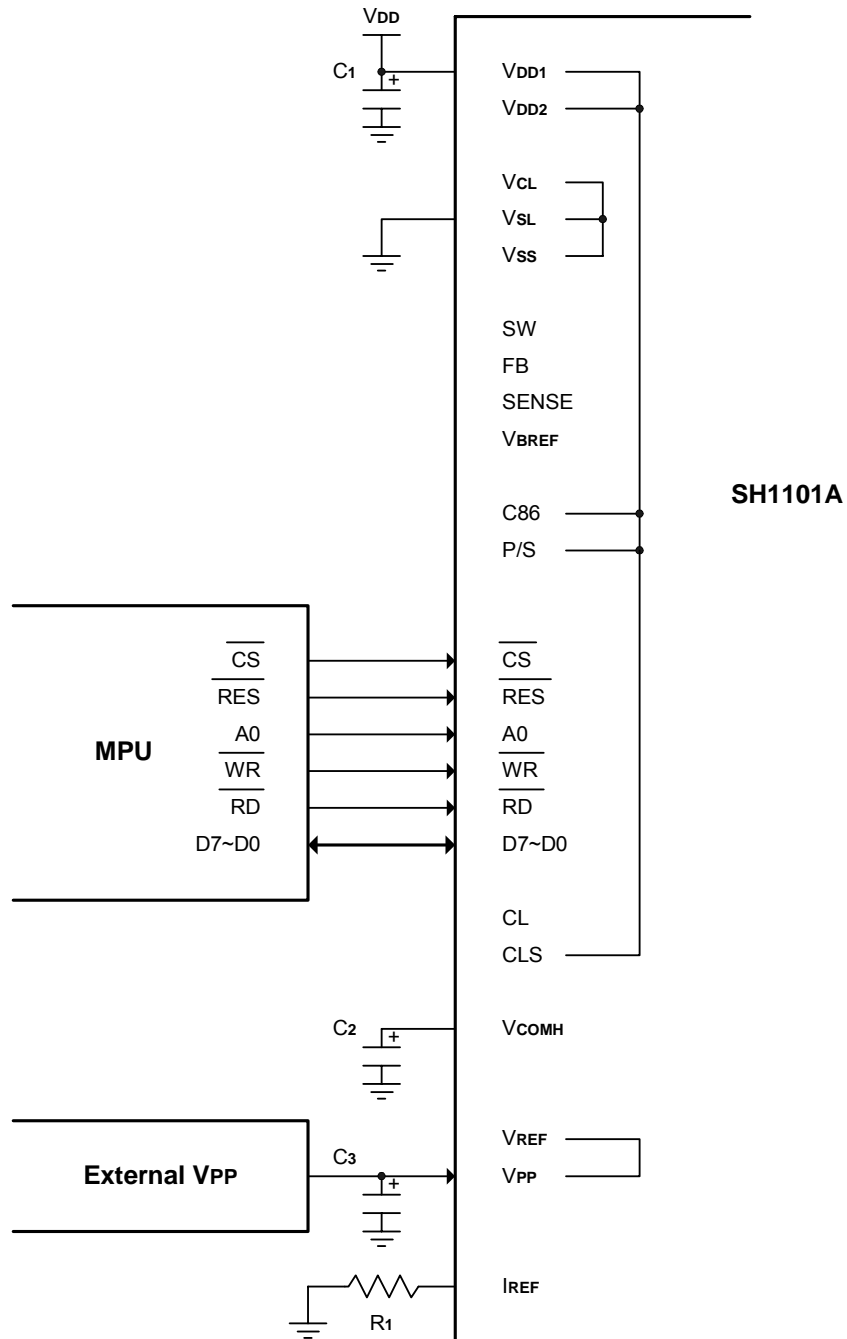


Figure. 8

Note:

C1 - C3: 4.7μF.

R1: about 910kΩ, $R1 = (\text{Voltage at IREF} - V_{SS})/I_{REF}$



2. 6800 Series Interface: (Internal oscillator, Built-in DC-DC)

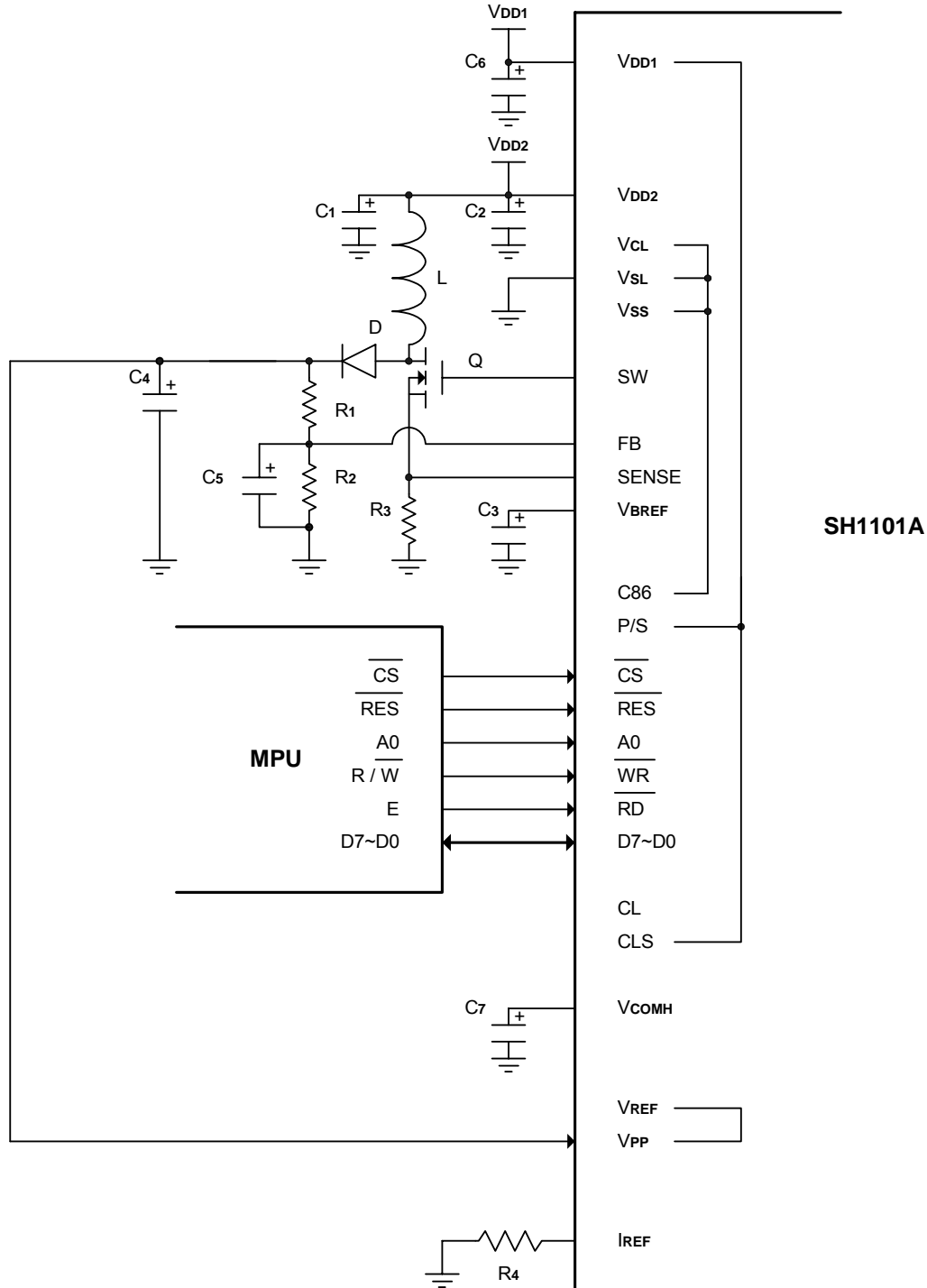


Figure. 9

Note:

L, D, Q, R1, R2, R3, C1 - C6: Please refer to following description of DC-DC module.

C6, C7: 4.7μF

R3: about 910kΩ, R4 = (Voltage at IREF - Vss)/IREF



3. Serial Interface: (External oscillator, External VPP)

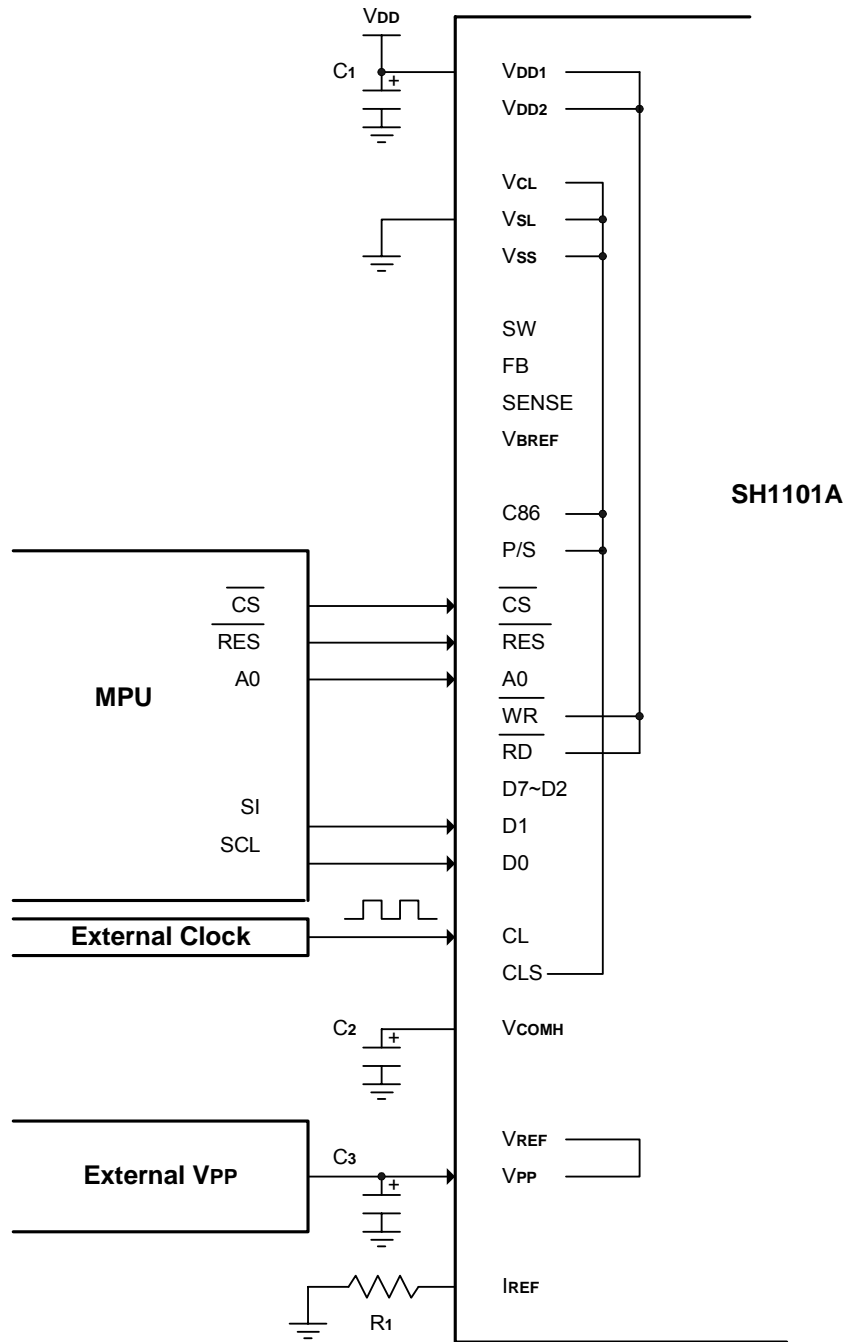


Figure. 10

Note:

C1 - C3: 4.7μF

R1: about 910kΩ, $R1 = (\text{Voltage at IREF} - V_{SS})/I_{REF}$



DC-DC:

Below application circuit is an example for the input voltage of 3V V_{DD2} to generate V_{PP} of about 12V@10mA-25mA application.

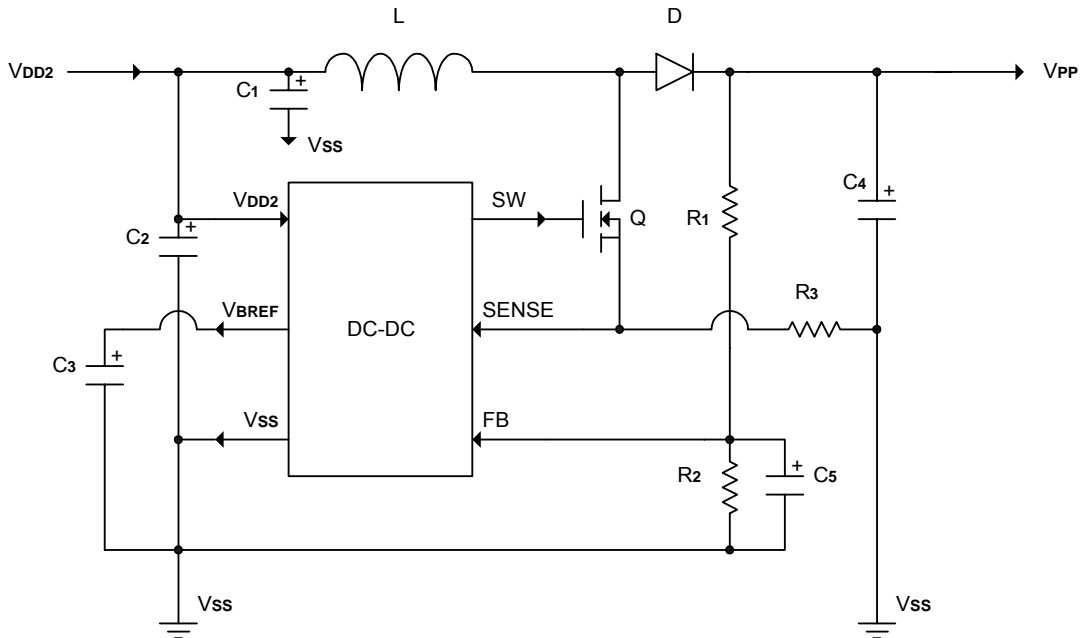
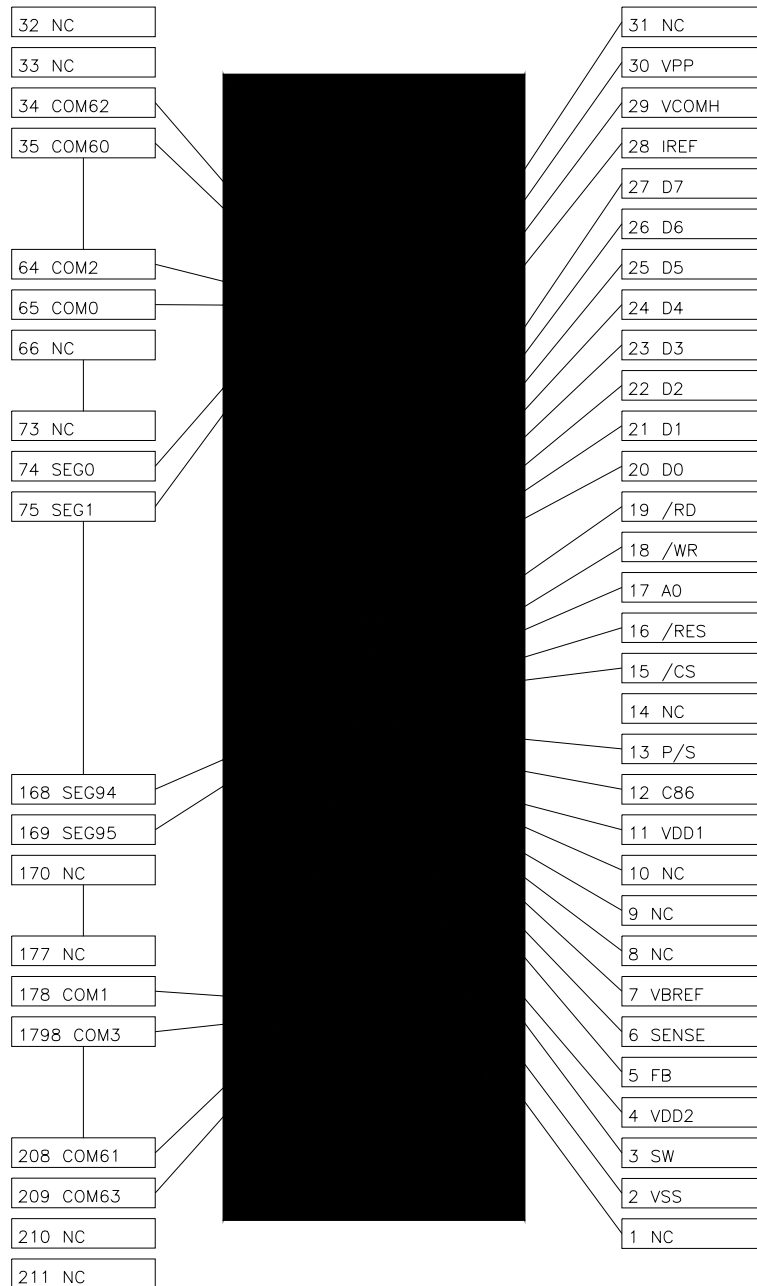


Figure. 11

| Symbol | Value | Recommendation |
|--------|-----------------|--|
| L | 10 μ H | LQH3C100K24 |
| D | SCHOTTKY DIODE | 20V@0.5A, MBR0520 |
| Q | MOSFET | N-FET with low $R_{DS(ON)}$ and low V_{TH} , MGSF1N02LT1 |
| R1 | 930k Ω | 1%, 1/8W |
| R2 | 110k Ω | 1%, 1/8W |
| R3 | 0.12 Ω | 1%, 1/2W |
| C1 | 1 - 10 μ F | Ceramic/16V |
| C2 | 0.1 - 1 μ F | Ceramic/16V |
| C3 | 1 μ F | Ceramic/16V |
| C4 | 6.8 μ F | Low ESR/25V |
| C5 | 1000pF | Ceramic/16V |



TCP Pin Layout



(Copper Side View)



TCP Pin Assignment (Total: 211 pins)

| Pin No. | Designation | Pin No. | Designation | Pin No. | Designation | Pin No. | Designation |
|---------|------------------|---------|-------------|---------|-------------|---------|-------------|
| 1 | NC | 41 | COM48 | 81 | SEG7 | 121 | SEG47 |
| 2 | Vss | 42 | COM46 | 82 | SEG8 | 122 | SEG48 |
| 3 | SW | 43 | COM44 | 83 | SEG9 | 123 | SEG49 |
| 4 | VDD2 | 44 | COM42 | 84 | SEG10 | 124 | SEG50 |
| 5 | FB | 45 | COM40 | 85 | SEG11 | 125 | SEG51 |
| 6 | SENSE | 46 | COM38 | 86 | SEG12 | 126 | SEG52 |
| 7 | VBREF | 47 | COM36 | 87 | SEG13 | 127 | SEG53 |
| 8 | NC | 48 | COM34 | 88 | SEG14 | 128 | SEG54 |
| 9 | NC | 49 | COM32 | 89 | SEG15 | 129 | SEG55 |
| 10 | NC | 50 | COM30 | 90 | SEG16 | 130 | SEG56 |
| 11 | VDD1 | 51 | COM28 | 91 | SEG17 | 131 | SEG57 |
| 12 | C86 | 52 | COM26 | 92 | SEG18 | 132 | SEG58 |
| 13 | P/S | 53 | COM24 | 93 | SEG19 | 133 | SEG59 |
| 14 | NC | 54 | COM22 | 94 | SEG20 | 134 | SEG60 |
| 15 | \overline{CS} | 55 | COM20 | 95 | SEG21 | 135 | SEG61 |
| 16 | \overline{RES} | 56 | COM18 | 96 | SEG22 | 136 | SEG62 |
| 17 | A0 | 57 | COM16 | 97 | SEG23 | 137 | SEG63 |
| 18 | \overline{WR} | 58 | COM14 | 98 | SEG24 | 139 | SEG64 |
| 19 | \overline{RD} | 59 | COM12 | 99 | SEG25 | 139 | SEG65 |
| 20 | D0 | 60 | COM10 | 100 | SEG26 | 140 | SEG66 |
| 21 | D1 | 61 | COM8 | 101 | SEG27 | 141 | SEG67 |
| 22 | D2 | 62 | COM6 | 102 | SEG28 | 142 | SEG68 |
| 23 | D3 | 63 | COM4 | 103 | SEG29 | 143 | SEG69 |
| 24 | D4 | 64 | COM2 | 104 | SEG30 | 144 | SEG70 |
| 25 | D5 | 65 | COM0 | 105 | SEG31 | 145 | SEG71 |
| 26 | D6 | 66 | NC | 106 | SEG32 | 146 | SEG72 |
| 27 | D7 | 67 | NC | 107 | SEG33 | 147 | SEG73 |
| 28 | IREF | 68 | NC | 108 | SEG34 | 148 | SEG74 |
| 29 | VCOMH | 69 | NC | 109 | SEG35 | 149 | SEG75 |
| 30 | VPP | 70 | NC | 110 | SEG36 | 150 | SEG76 |
| 31 | NC | 71 | NC | 111 | SEG37 | 151 | SEG77 |
| 32 | NC | 72 | NC | 112 | SEG38 | 152 | SEG78 |
| 33 | NC | 73 | NC | 113 | SEG39 | 153 | SEG79 |
| 34 | COM62 | 74 | SEG0 | 114 | SEG40 | 154 | SEG80 |
| 35 | COM60 | 75 | SEG1 | 115 | SEG41 | 155 | SEG81 |
| 36 | COM58 | 76 | SEG2 | 116 | SEG42 | 156 | SEG82 |
| 37 | COM56 | 77 | SEG3 | 117 | SEG43 | 157 | SEG83 |
| 38 | COM54 | 78 | SEG4 | 118 | SEG44 | 158 | SEG84 |
| 39 | COM52 | 79 | SEG5 | 119 | SEG45 | 159 | SEG85 |
| 40 | COM50 | 80 | SEG6 | 120 | SEG46 | 160 | SEG86 |

**TCP Pin Assignment (continued)**

| Pin No. | Designation | Pin No. | Designation | Pin No. | Designation | Pin No. | Designation |
|---------|-------------|---------|-------------|---------|-------------|---------|-------------|
| 161 | SEG87 | 176 | NC | 191 | COM27 | 206 | COM57 |
| 162 | SEG88 | 177 | NC | 192 | COM29 | 207 | COM59 |
| 163 | SEG89 | 178 | COM1 | 193 | COM31 | 208 | COM61 |
| 164 | SEG90 | 179 | COM3 | 194 | COM33 | 209 | COM63 |
| 165 | SEG91 | 180 | COM5 | 195 | COM35 | 210 | NC |
| 166 | SEG92 | 181 | COM7 | 196 | COM37 | 211 | NC |
| 167 | SEG93 | 182 | COM9 | 197 | COM39 | | |
| 168 | SEG94 | 183 | COM11 | 198 | COM41 | | |
| 169 | SEG95 | 184 | COM13 | 199 | COM43 | | |
| 170 | NC | 185 | COM15 | 200 | COM45 | | |
| 171 | NC | 186 | COM17 | 201 | COM47 | | |
| 172 | NC | 187 | COM19 | 202 | COM49 | | |
| 173 | NC | 188 | COM21 | 203 | COM51 | | |
| 174 | NC | 189 | COM23 | 204 | COM53 | | |
| 175 | NC | 190 | COM25 | 205 | COM55 | | |

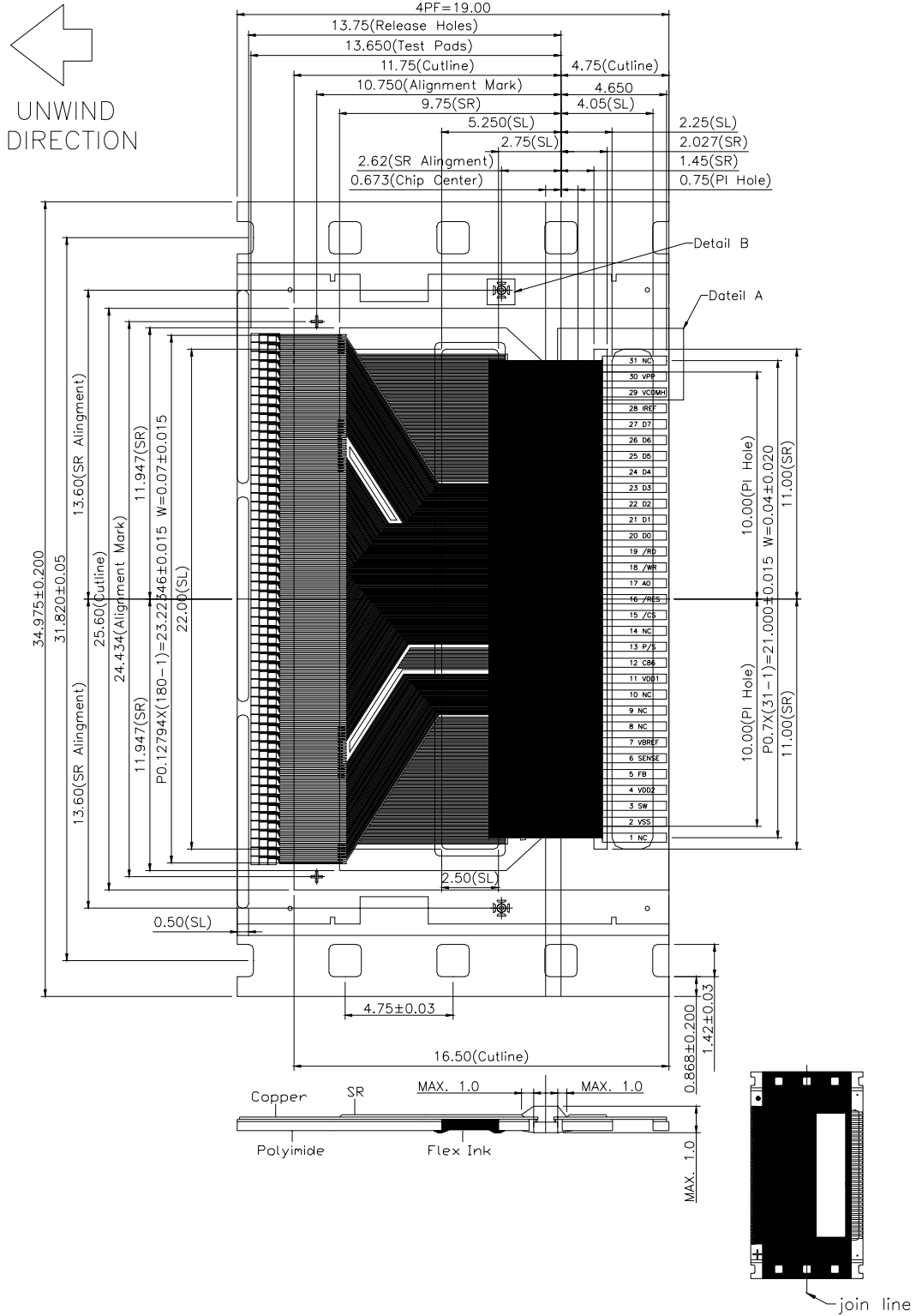
Note:

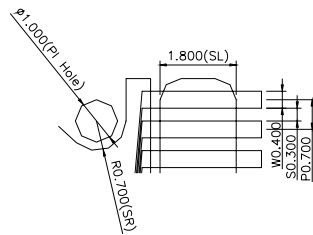
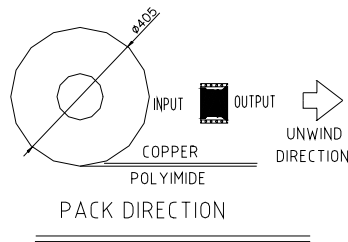
Following is the details of pad connection in SH1101A-TCP03 (TCP Form).

- "CLS" pad connects to "VDD1" pad, Internal oscillator circuit is enabled.
- "VREF" pad connects to "VPP" pad.
- "VCL" & "VSL" pad connects to "VSS" pad.
- "C86" & "P/S" pad options can be selected by user. So SH1101A-TCP03 (TCP Form) supports 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface or serial peripheral interface.
- SH1101A-TCP03 (TCP Form) supports internal DC-DC converter function.

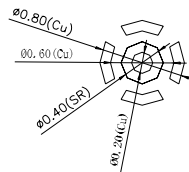


External View of TCP Pins

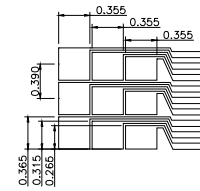




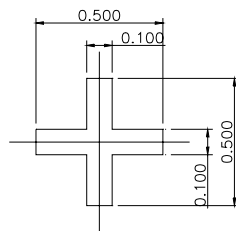
Detail A
Scale 2:1



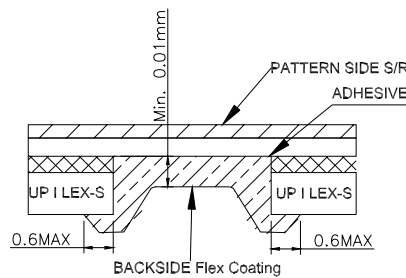
Detail B
Scale 5:1



Detail of Test Pads
Scale 5:1



Detail of Alignment Mark
Scale 10:1



NOTES:

1. All SR Dimension Tolerance ± 0.200 mm if not specified
2. All SL Dimension Tolerance ± 0.05 mm if not specified
3. Corner radiuses unless otherwise specified is 0.20 mm
4. PKG Reel Size : $\phi 4.05$ mm
5. Input IL total pitch from left 2nd to right 2nd
6. Output IL total pitch from left 2nd to right 2nd
7. IL Pitch=45um ; Min Pitch=45um||IL/TraceL

Cautions Concerning Storage:

1. When storing the product, it is recommended that it be left in its shipping package.
After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions:

| Storage state | Storage conditions |
|---|---|
| unopened (less than 90 days) | Temperature: 5 to 30 ; humidity: 80%RH or less. |
| After seal of broken (less than 30 days) | Room temperature, dry nitrogen atmosphere |

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
5. Don't store the product such that it subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
It is recommended that the products be inspected before use.



SH1101A

Ordering Information

| Part No. | Package |
|-----------------|------------------------|
| SH1101A-COG01 | Gold bump on chip tray |
| SH1101A-TCP03 | TCP Form |



Data Sheet Revision History

| Version | Content | Date |
|----------------|--|-------------|
| 0.13 | Ordering Information: 1, SH1101AG changed to SH1101A-COG01 2, SH1101AB1 changed to SH1101A-TCP03 (Page 46) | July. 2005 |
| 0.1 | 1. "Pin Configuration", "Pad Configuration" addition. (Page2) 2. "TAB Pin Layout", "TAB Pin Assignment" addition. (Page 41~45) 3. "Ordering Information" addition. (Page 46) | May. 2005 |
| 0.0 | Original | Mar. 2005 |