

## 650V SuperGaN® FET in TOLL (source tab)

### Description

The TP65H050G4QS 650V, 50 mΩ gallium nitride (GaN) FET is a normally-off device using Transphorm's Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

### Related Literature

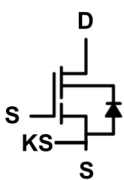
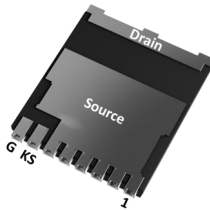
- [AN0009](#): Recommended External Circuitry for GaN FETs
- [AN0003](#): Printed Circuit Board Layout and Probing
- [AN0014](#): Low cost driver solution

### Ordering Information

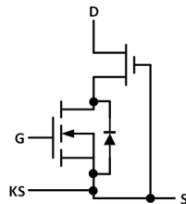
Part Number	Package	Package Configuration
TP65H050G4QS-TR	10x12mm TOLL	Source

\* "-TR" suffix refers to tape and reel. Refer to AN0012 for details.

**TP65H050G4QS  
TOLL**  
(bottom view)



Cascode Schematic Symbol



Cascode Device Structure

### Features

- JEDEC qualified GaN technology
- Dynamic  $R_{DS(on)eff}$  production tested
- Robust design, defined by
  - Wide gate safety margin
  - Transient over-voltage capability
- Enhanced inrush current capability
- Very low  $Q_{RR}$
- Reduced crossover loss
- Kelvin source for low inductance gate return path

### Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- Pin-to-pin drop-in with e-mode GaN

### Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor



### Key Specifications

$V_{DSS}$ (V)	650
$V_{DSS(TR)}$ (V)	800
$R_{DS(on)eff}$ (mΩ) max*	60
$Q_{OSS}$ (nC) typ	120
$Q_G$ (nC) typ	16

\* Dynamic on-resistance; see Figures 19 and 20

# TP65H050G4QS

## Absolute Maximum Ratings (T<sub>c</sub>=25 °C unless otherwise stated.)

Symbol	Parameter	Limit Value	Unit	
V <sub>DSS</sub>	Drain to source voltage (T <sub>J</sub> = -55 °C to 150 °C)	650	V	
V <sub>DSS(TR)</sub>	Transient drain to source voltage <sup>(a)</sup>	800		
V <sub>GSS</sub>	Gate to source voltage	±20		
P <sub>D</sub>	Maximum power dissipation @T <sub>c</sub> =25 °C	119	W	
I <sub>D</sub>	Continuous drain current @T <sub>c</sub> =25 °C <sup>(b)</sup>	34	A	
	Continuous drain current @T <sub>c</sub> =100 °C <sup>(b)</sup>	22	A	
I <sub>DM</sub>	Pulsed drain current (pulse width: 10µs)	150	A	
T <sub>C</sub>	Operating temperature	Case	-55 to +150	°C
T <sub>J</sub>		Junction	-55 to +150	°C
T <sub>S</sub>	Storage temperature	-55 to +150	°C	
T <sub>SOLD</sub>	Soldering peak temperature <sup>(c)</sup>	260	°C	
-	Mounting Torque	80	N cm	

Notes:

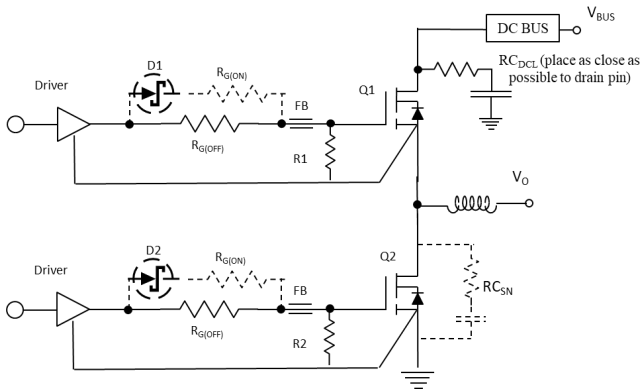
- In off-state, spike duty cycle D<0.01, spike duration <30µs, non repetitive
- For increased stability at high current operation, see Circuit Implementation on page 3
- For 10 sec., 1.6mm from the case

## Thermal Resistance

Symbol	Parameter	Typical	Unit
R <sub>θJC</sub>	Junction-to-case	1.05	°C/W
R <sub>θJA</sub>	Junction-to-ambient	45	°C/W

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## Circuit Implementation



For additional gate driver options/configurations, please see Application Note [AN0009](#)

### Layout Recommendations

#### Gate Loop:

- Gate Driver: SiLab Si823x/Si827x
- Keep gate loop compact
- Minimize coupling with power loop

#### Power loop: ( For reference see page 12 )

- Minimize power loop path inductance
- Minimize switching node coupling with high and low power plane
- Add DC bus snubber to reduce to voltage ringing
- Add Switching node snubber for high current operation

**Simplified Half-bridge Schematic ( See also on Figure 15 )**

Parameter	Symbol	Value
Single Gate Resistor <sup>(d)</sup>	R <sub>G</sub> (R <sub>G(OFF)</sub> only)	40 Ω ( D1/D2/R <sub>G(ON)</sub> : NS)
Dual Gate Resistor <sup>(d)</sup>	R <sub>G(ON)</sub> / R <sub>G(OFF)</sub>	30 Ω / 40 Ω
Dual Gate Resistor <sup>(d)</sup>	Effective R <sub>G(ON)</sub> / R <sub>G(OFF)</sub>	17 Ω / 40 Ω
Operating frequency	F <sub>sw</sub>	≤200 kHz
Steering Diode	D1/D2	Schottky diode ( V <sub>r</sub> ≥20V, V <sub>f</sub> ≤0.5V, I <sub>o</sub> ≥1A)
Gate Ferrite Bead	FB	180 – 330 Ω at 100MHz <sup>(d)</sup>
Gate-to-source Resistor	R1/R2	10 kΩ
DC Link RC Noise Filter	RC <sub>DCL</sub>	4.7nF + 5Ω
Switching Node RC Snubber	RC <sub>SN</sub>	Not Necessary <sup>(e)</sup>
Gate Driver	Driver	Si823x/Si827x or similar
<p>Note:</p> <p>d. For every design and layout, a range of ferrite beads (FB), R<sub>G</sub> and DC link RC filter should be evaluated to help suppress any high frequency ringing and optimize performance</p> <p>e. RC<sub>SN</sub> (47pF + 15Ω) is needed if</p> <ul style="list-style-type: none"> <li>• R<sub>G</sub> is smaller than recommendations</li> <li>• Layout is not optimized</li> <li>• Requires high current operation</li> </ul>		

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## Electrical Parameters (T<sub>J</sub>=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Forward Device Characteristics</b>						
V <sub>DSS(BL)</sub>	Drain-source voltage	650	—	—	V	V <sub>GS</sub> =0V
V <sub>GS(th)</sub>	Gate threshold voltage	3.3	4	4.8	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =0.7mA
ΔV <sub>GS(th)/T<sub>J</sub></sub>	Gate threshold voltage temperature coefficient	—	-6.2	—	mV/°C	
R <sub>DS(on)eff</sub>	Drain-source on-resistance <sup>(g)</sup>	—	50	60	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =22A
		—	105	—		V <sub>GS</sub> =10V, I <sub>D</sub> =22A, T <sub>J</sub> =150 °C
I <sub>DSS</sub>	Drain-to-source leakage current	—	4	40	μA	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V
		—	15	—		V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>J</sub> =150 °C
I <sub>GSS</sub>	Gate-to-source forward leakage current	—	—	100	nA	V <sub>GS</sub> =20V
		—	—	-100		V <sub>GS</sub> =-20V
C <sub>ISS</sub>	Input capacitance	—	1000	—	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =400V, f=1MHz
C <sub>OSS</sub>	Output capacitance	—	110	—		
C <sub>RSS</sub>	Reverse transfer capacitance	—	6	—		
C <sub>O(er)</sub>	Output capacitance, energy related <sup>(h)</sup>	—	164	—	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V to 400V
C <sub>O(tr)</sub>	Output capacitance, time related <sup>(i)</sup>	—	280	—		
Q <sub>G</sub>	Total gate charge	—	16	24	nC	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V to 10V, I <sub>D</sub> =22A
Q <sub>GS</sub>	Gate-source charge	—	6	—		
Q <sub>GD</sub>	Gate-drain charge	—	5	—		
Q <sub>OSS</sub>	Output charge	—	120	—	nC	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V to 400V
t <sub>D(on)</sub>	Turn-on delay	—	49.2	—	ns	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V to 10V, I <sub>D</sub> =22A, R <sub>g</sub> =45Ω, Z <sub>FB</sub> =240Ω at 100MHz (See Figure 14)
t <sub>R</sub>	Rise time	—	11.3	—		
t <sub>D(off)</sub>	Turn-off delay	—	88.3	—		
t <sub>F</sub>	Fall time	—	10.9	—		

Notes:

- g. Dynamic on-resistance; see Figures 19 and 20 for test circuit and conditions
- h. Equivalent capacitance to give same stored energy as V<sub>DS</sub> rises from 0V to 400V
- i. Equivalent capacitance to give same charging time as V<sub>DS</sub> rises from 0V to 400V

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## Electrical Parameters (T<sub>J</sub>=25 °C unless otherwise stated)

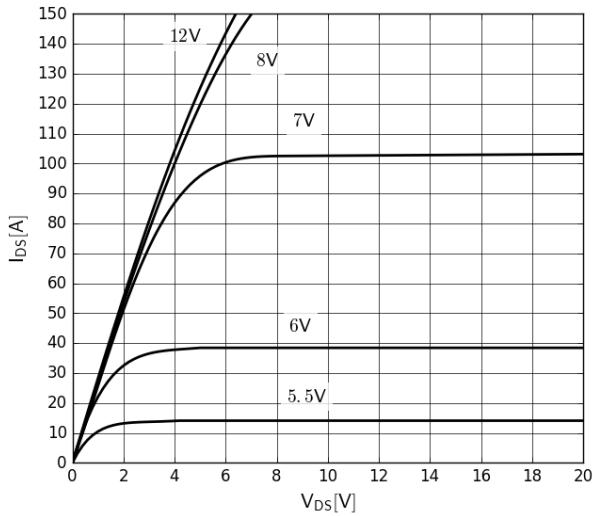
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Reverse Device Characteristics</b>						
I <sub>S</sub>	Reverse current	—	—	22	A	V <sub>GS</sub> =0V, T <sub>C</sub> =100 °C, ≤25% duty cycle
V <sub>SD</sub>	Reverse voltage <sup>(i)</sup>	—	2.2	2.6	V	V <sub>GS</sub> =0V, I <sub>S</sub> =22A
		—	1.6	1.9		V <sub>GS</sub> =0V, I <sub>S</sub> =11A
t <sub>RR</sub>	Reverse recovery time	—	50	—	ns	I <sub>S</sub> =22A, V <sub>DD</sub> =400V
Q <sub>RR</sub>	Reverse recovery charge <sup>(i)</sup>	—	0	—	nC	

Notes:

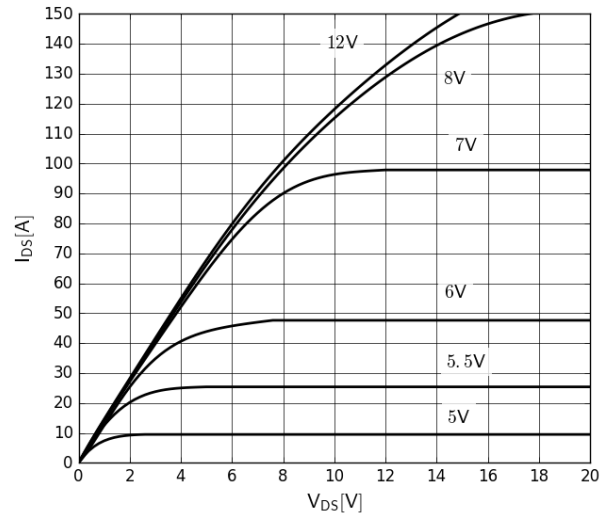
- i. Includes dynamic R<sub>DS(on)</sub> effect
- j. Excludes Q<sub>oss</sub>

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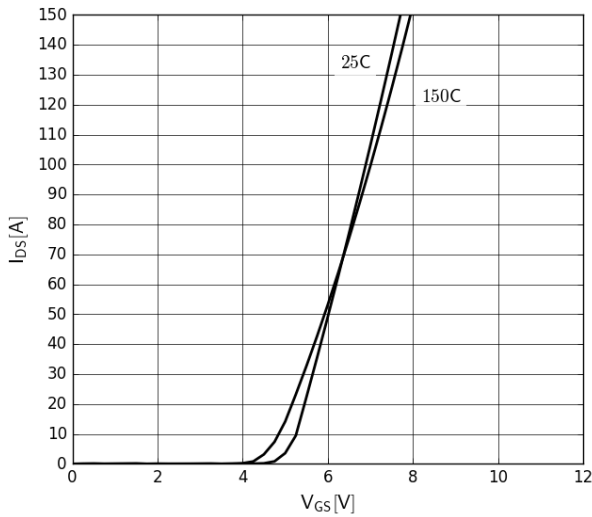
Typical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise stated)



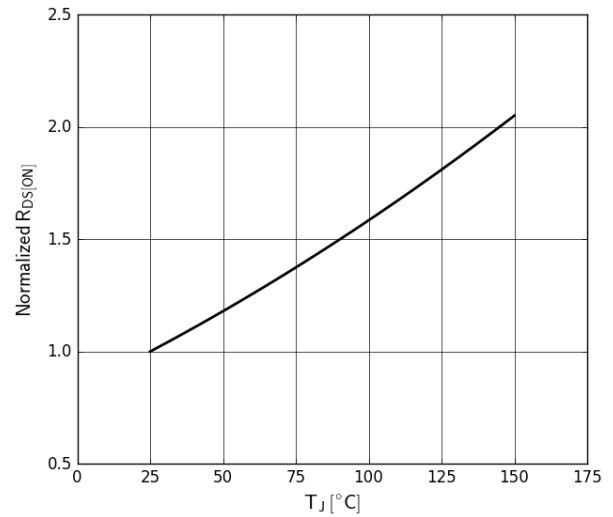
**Figure 1. Typical Output Characteristics  $T_J=25^\circ\text{C}$**   
Parameter:  $V_{GS}$



**Figure 2. Typical Output Characteristics  $T_J=150^\circ\text{C}$**   
Parameter:  $V_{GS}$



**Figure 3. Typical Transfer Characteristics**  
 $V_{DS}=20\text{V}$ , parameter:  $T_J$



**Figure 4. Normalized On-resistance**  
 $I_D=30\text{A}$ ,  $V_{GS}=8\text{V}$

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Typical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise stated)

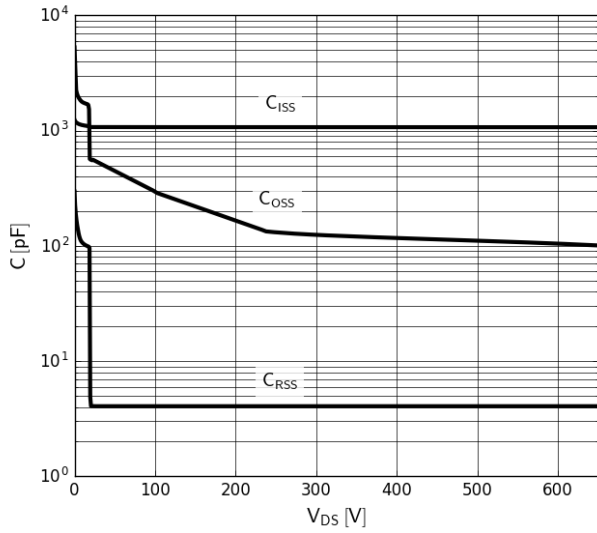


Figure 5. Typical Capacitance

$V_{GS}=0V$ ,  $f=1MHz$

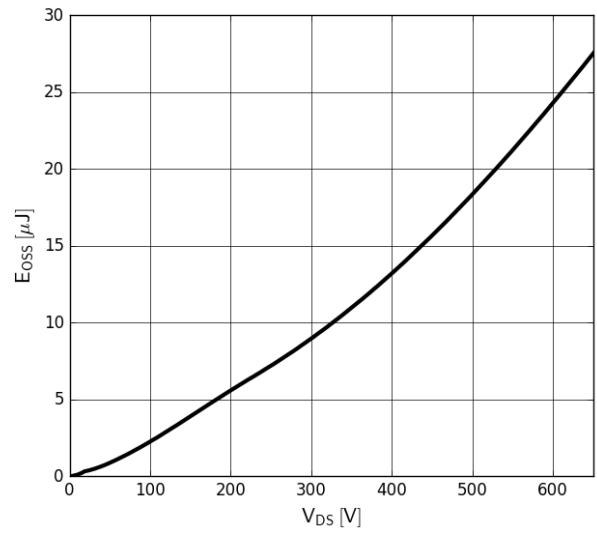


Figure 6. Typical  $C_{oss}$  Stored Energy

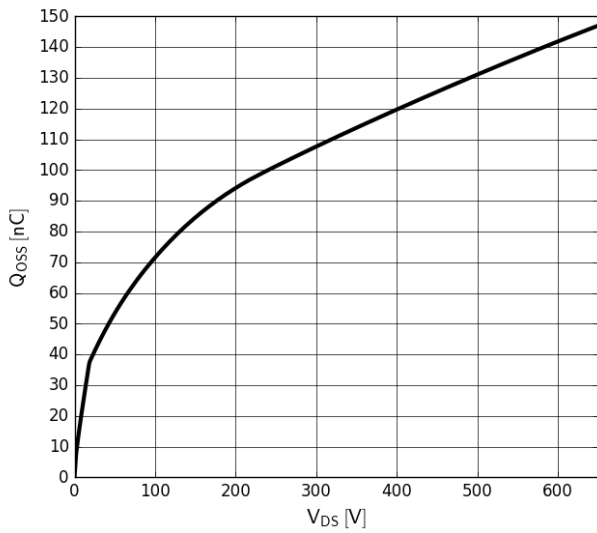


Figure 7. Typical  $Q_{oss}$

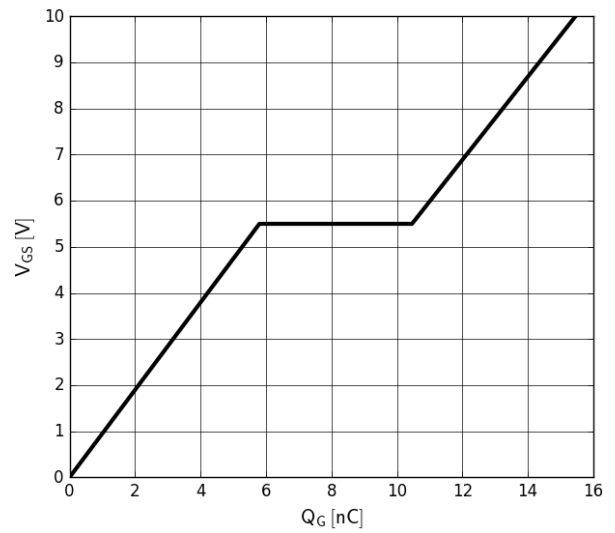
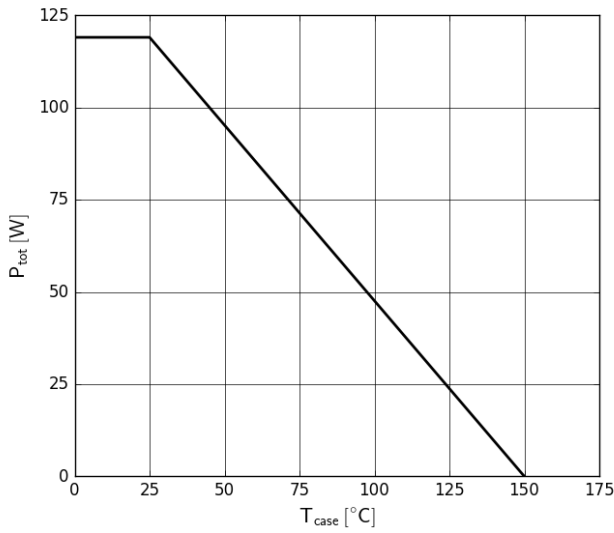


Figure 8. Typical Gate Charge

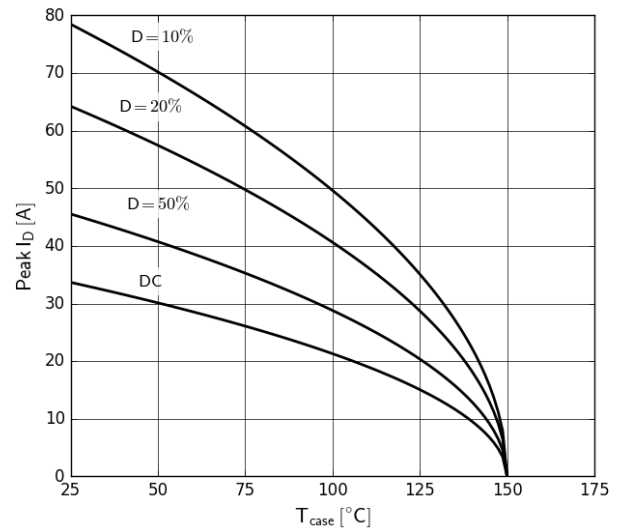
$I_{DS}=32A$ ,  $V_{DS}=400V$

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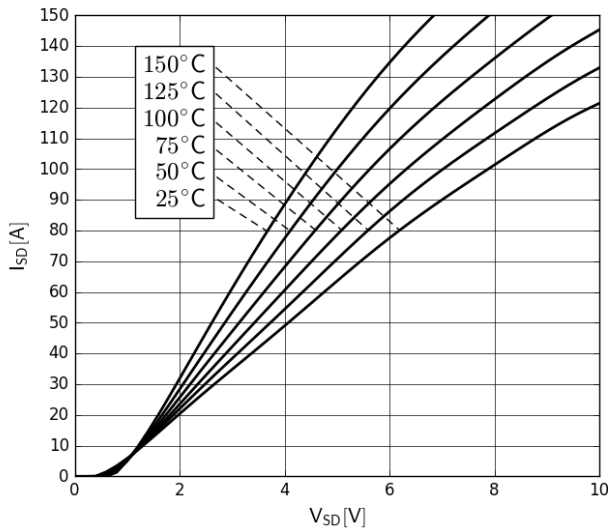
## Typical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise stated)



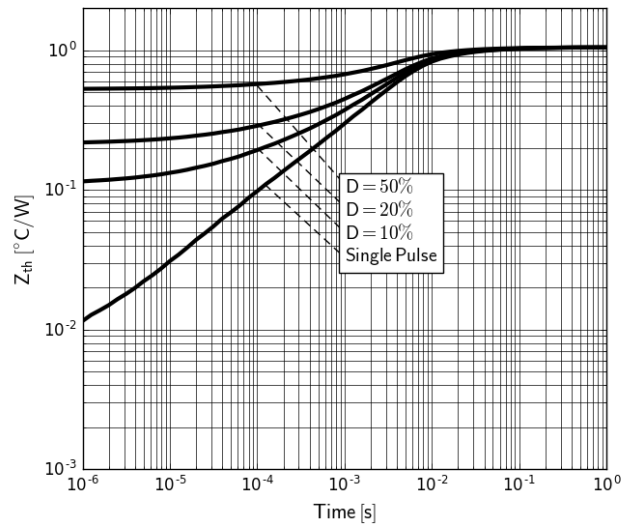
**Figure 9. Power Dissipation**



**Figure 10. Current Derating**  
Pulse width  $\leq 10\mu\text{s}$ ,  $V_{GS} \geq 10\text{V}$



**Figure 11. Forward Characteristics of Rev. Diode**  
 $I_S=f(V_{SD})$ , parameter:  $T_J$



**Figure 12. Transient Thermal Resistance**



# TP65H050G4QS

Typical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise stated)

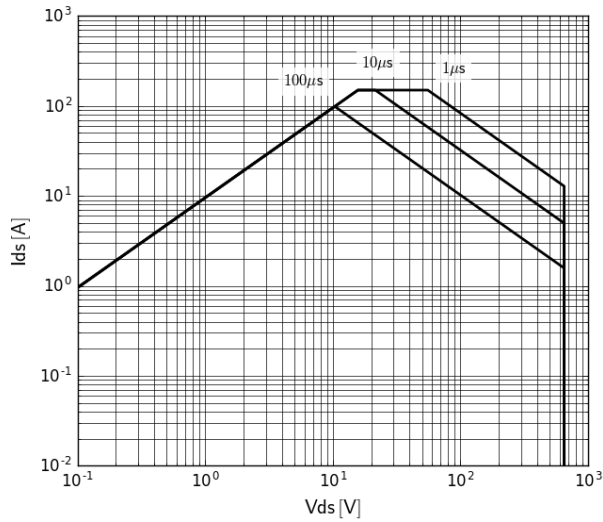


Figure 13. Safe Operating Area  $T_C=25^\circ\text{C}$

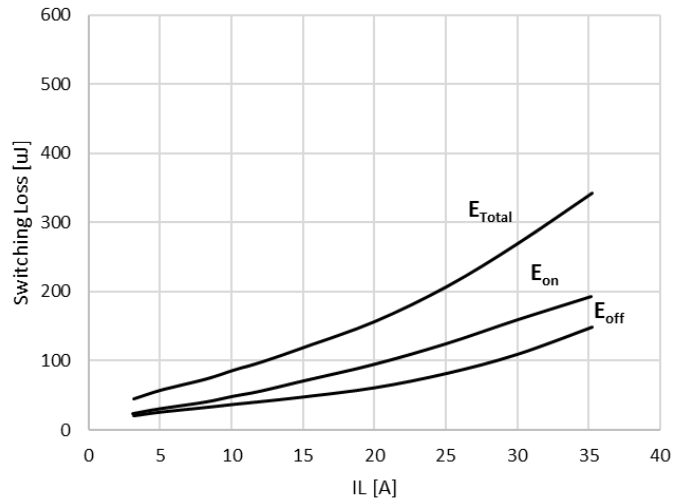
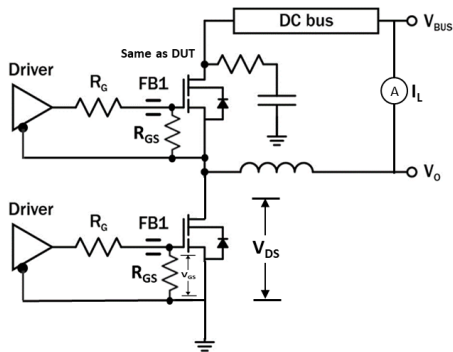


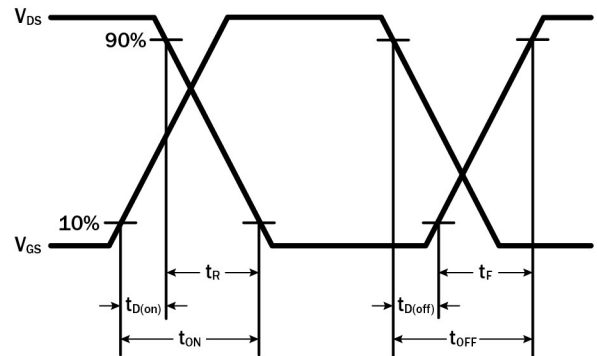
Figure 14. Inductive Switching Loss  $T_C=25^\circ\text{C}$   
 $R_g=45\Omega$ ,  $V_{DS}=400\text{V}$

# TP65H050G4QS

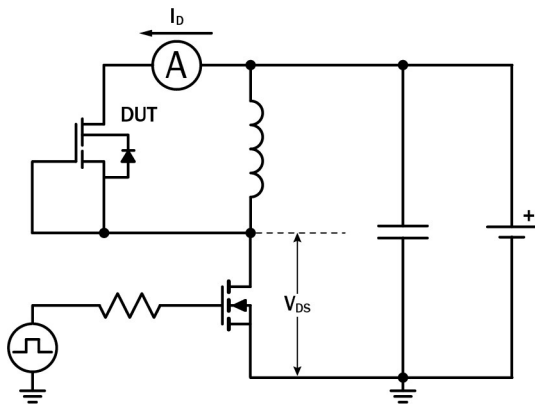
## Test Circuits and Waveforms



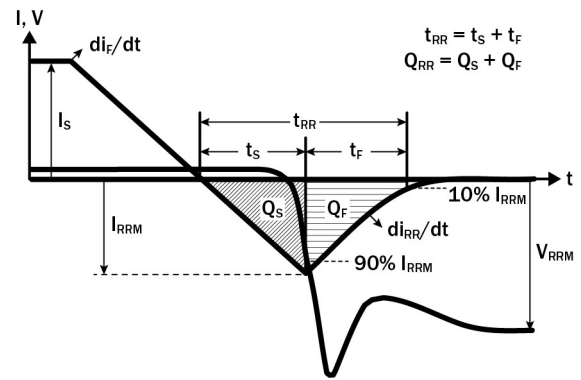
**Figure 15. Switching Time Test Circuit**  
(see circuit implementation on page 3 for methods to ensure clean switching)



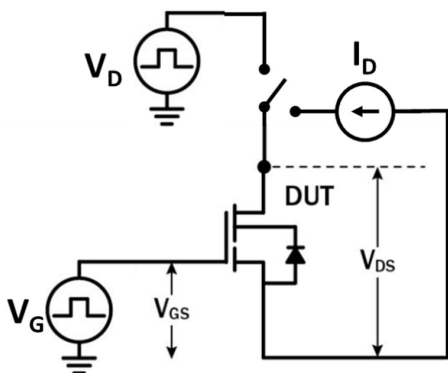
**Figure 16. Switching Time Waveform**



**Figure 17. Diode Characteristics Test Circuit**

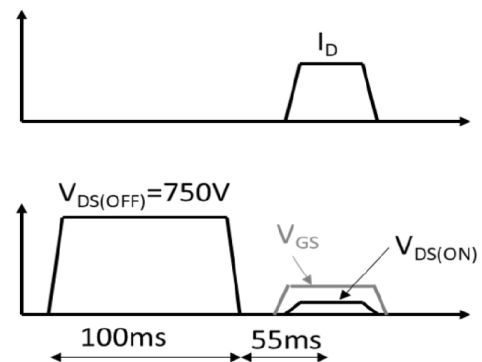


**Figure 18. Diode Recovery Waveform**



**Figure 19. Dynamic  $R_{DS(on)eff}$  Test Circuit**

**Figure 19. Dynamic  $R_{DS(on)eff}$  Test Circuit**



$$R_{DS(ON) Eff} = V_{DS(ON)} / I_D$$

**Figure 20. Dynamic  $R_{DS(on)eff}$  Waveform**

# TP65H050G4QS

## Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

### When Evaluating Transphorm GaN Devices:

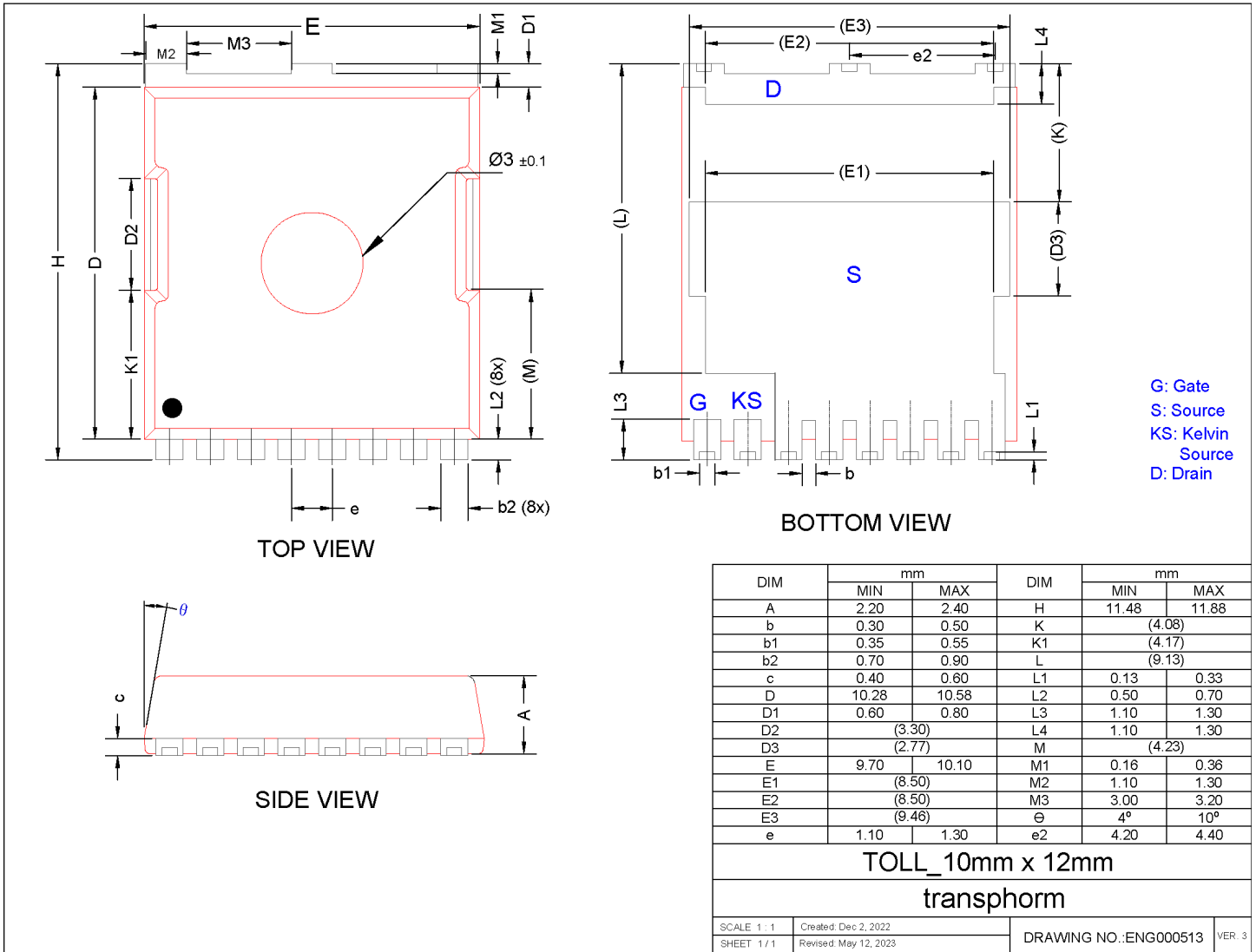
DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See <a href="#">AN0003</a> : Printed Circuit Board Layout and Probing	

## GaN Design Resources

The complete technical library of GaN design tools can be found at [transphormusa.com/design](https://transphormusa.com/design):

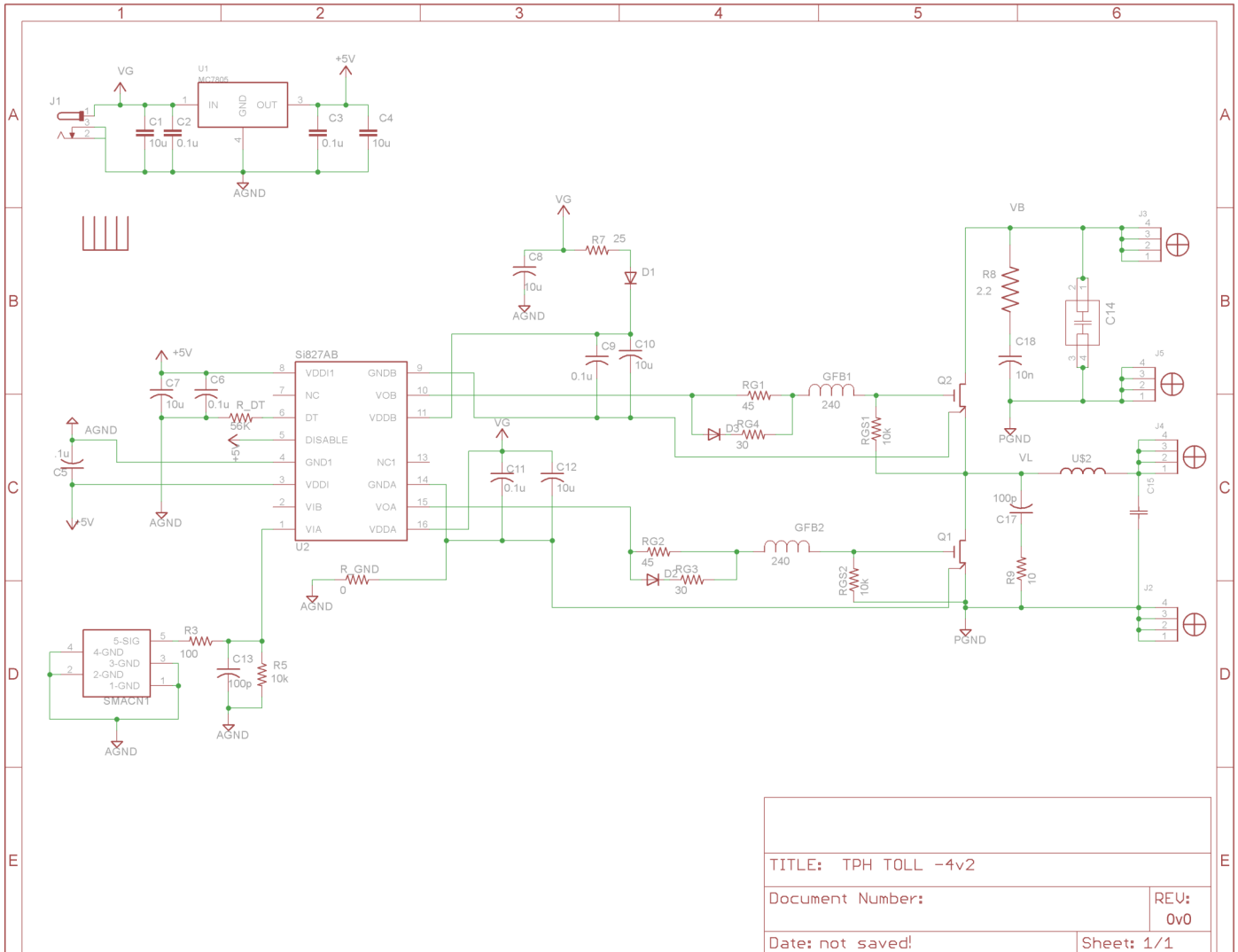
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

# TP65H050G4QS



# TP65H050G4QS

## Half-bridge Reference Schematic



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