Industrial SD 6.1
X-Mask Series (3D TLC)

Version 1.0

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1. GENERAL DESCRIPTION

1.1 Introduction

FLEXXON X-Mask SD Card is compliant with SD 6.1 specification and provides excellent performance, good reliability and wide compatibility. User could mask the entire SD card by special AP to prevent unauthorized access.

FLEXXON X-Mask SD Card provides security function to prevent the stored data from being stolen, tampered or modified by others. The stored data can only be access if the legitimate user can authenticate using the correct password.

FLEXXON X-Mask SD Card is suitable for users who want to store their private and valuable data in a flash storage without the risk of having it being read by unintended people.

The mask function is an additional feature, which will not affect the standard product specification.

1.2 Product Overview

◆ **Flash** 3D TLC	◆ **Support SD System Specification 6.1**
◆ **Capacity** 32GB to 512GB	◆ **Support SD SPI Mode**
◆ **Support Data Crypto**	◆ **Support Auto Read Refreshment**
◆ **Read disturbance management**	◆ **Adaptive wear leveling**
◆ **Support management of sudden power fails**	◆ **SMART function support**
◆ **Temperature Range** Operation (Gold): -25°C ~ 85°C Operation (Diamond): -40°C ~ 85°C ◆ Storage: -40°C ~ 85°C	

1.3 Workflow

FLEXXON X-Mask SD Card is a normal mode by default. User could set the password to enable mask mode. User is required to eject and re-insert the after set the password.

User could access the data by the legal host with security tool and enter correct password. When user power off the host or reinsert the card, the card will return to masked mode.

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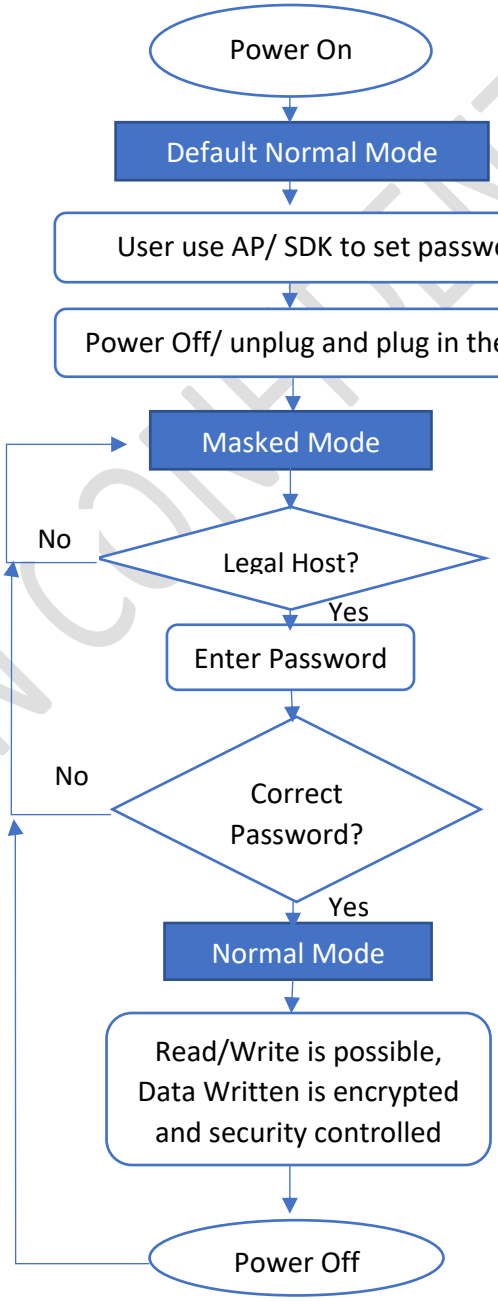


2. PRODUCT SPECIFICATIONS

2.1 Performance

Capacity	Sequential	
	Read (MB/s)	Write (MB/s)
32GB	85	25
64GB	85	25
128GB	85	48
256GB	85	50
512GB	85	50

Table 2-1 Performance of X-Mask SD Card

NOTES:

1. The performance is obtained from TestMetrix
2. Performance may vary from flash configuration and platform.

2.2 Power

Capacity	Read (mA)	Write (mA)	Standby (uA)
32GB	55	42	220
64GB	62	49	200
128GB	63	73	200
256GB	64	75	220
512GB	60	75	340

Table 2-2 Typical Power Consumption of X-Mask SD Card

2.3 MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The higher the MTBF value, the higher the reliability of the device. The predicted result of X-Mask SD Card is more than 3,000,000 hours.

3. ENVIRONMENTAL SPECIFICATIONS

Test Items	Test Conditions
Storage Temperature	-40°C ~ 85°C
Operating Temperature	Gold: -25°C ~ 85°C Diamond: -40°C ~ 85°C
Storage Humidity	40°C, 93% RH
Operating Humidity	25°C, 95% RH
Shock	1500G, Half Sin Pulse Duration 0.5ms
Vibration	80Hz ~ 2000Hz/20G, 20Hz ~ 80Hz/1.52mm, 3 axis/30min
Drop	150cm free fall, 6 face of each unit
Bending	≥ 10N, Hold 1 min/5 times
Torque	0.1N-m or +/-2.5 deg, Hold 30 seconds/5 times
ESD	Contact: +/- 4KV each item 25 times Air: +/- 8KV 10 times

Table 3-1 Environmental Specification

4. ELECTRICAL SPECIFICATIONS

4.1 DC Characteristics

4.1.1 Bus Operation Conditions for 3.3V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Table 4-1 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	

Table 4-2 Threshold Level for 1.8V Signaling

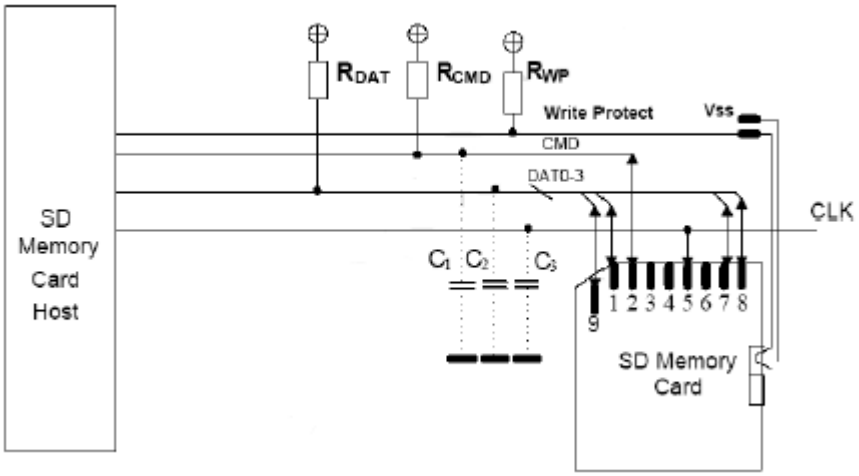
Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

Table 4-3 Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 4-4 Peak Voltage and Leakage Current

4.1.2 Bus Signal Line Load



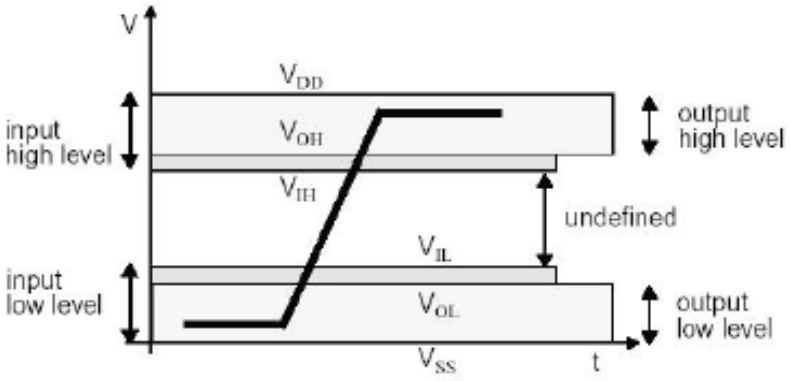
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

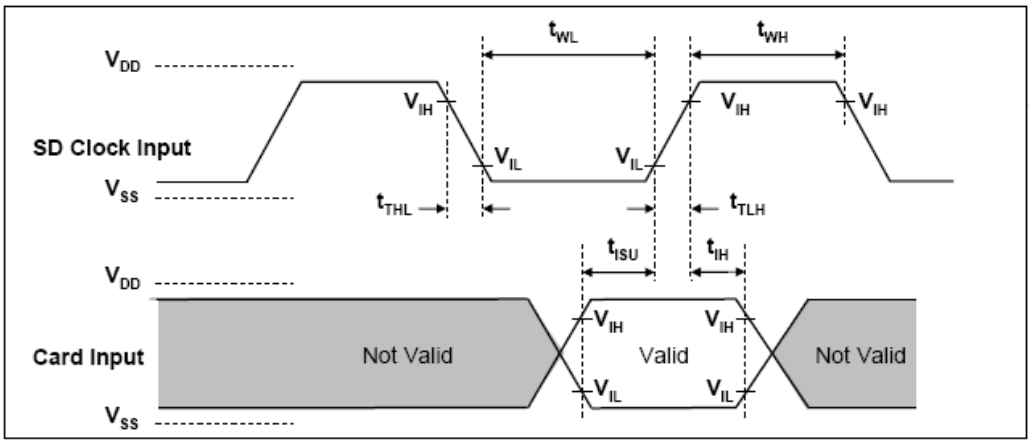
Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10[1]	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

Table 4-5 Peak Voltage and Leakage Current

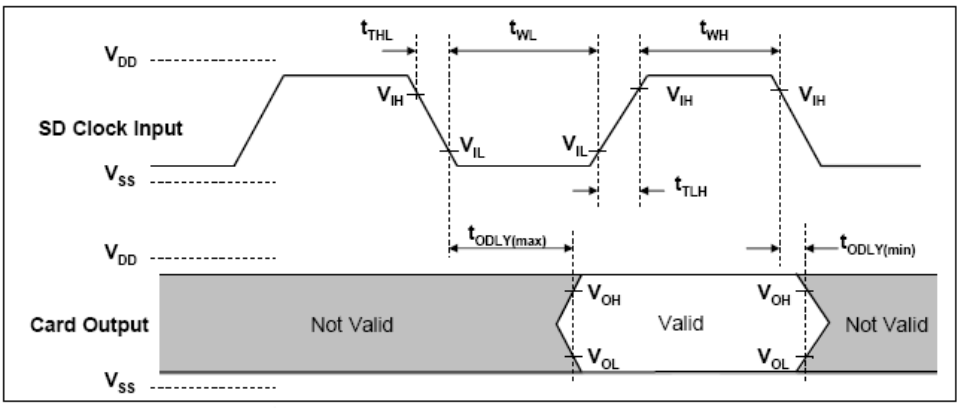
4.2 AC Characteristic



4.2.1 SD Interface timing (Default)



Card Input Timing (Default Speed Card)

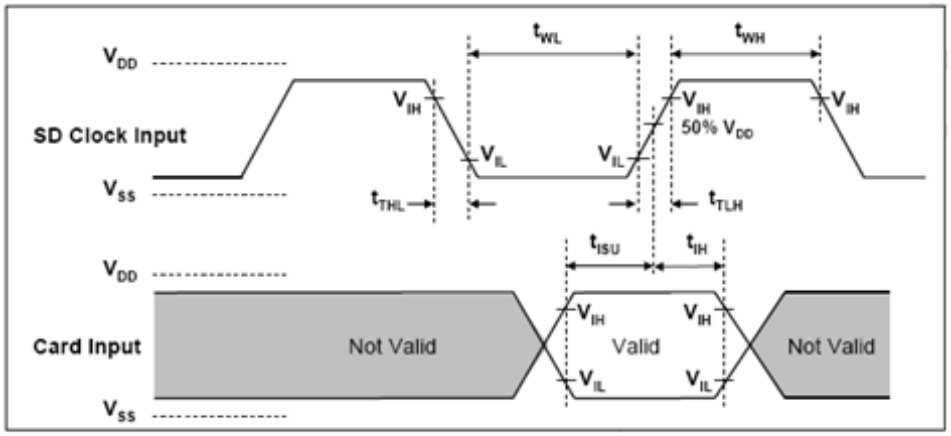


Card Output Timing (Default Speed Mode)

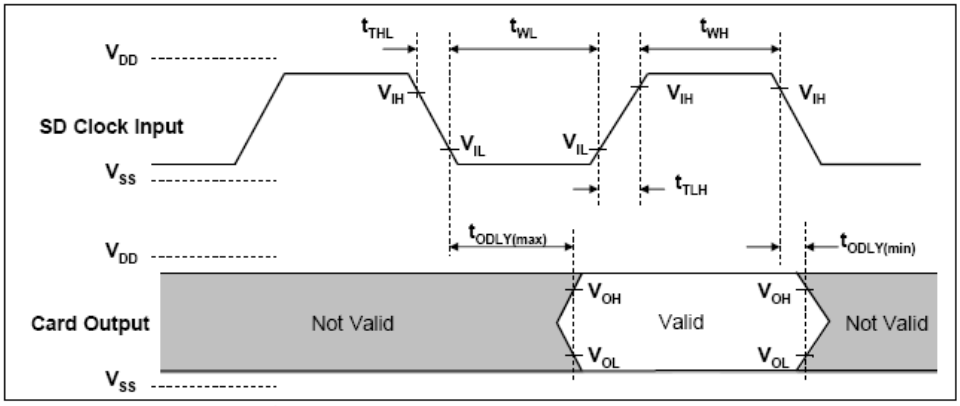
Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	KHz	C_{card}≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤ 40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L≤ 40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continues clock is required.

4.2.2 SD Interface Timing (High-Speed Mode)



Card Input Timing (High Speed Card)



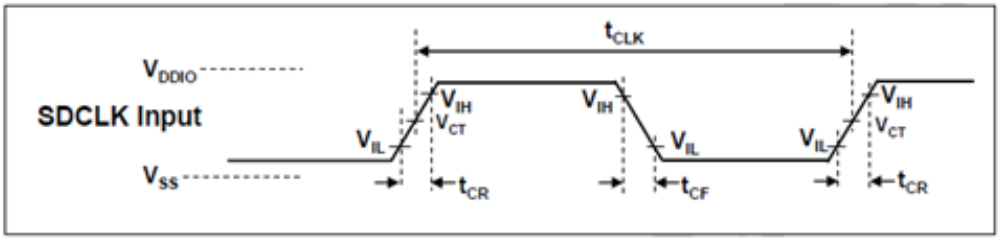
Card Output Timing (Default Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	$C_{card} \leq 10$ pF (1 card)
Clock low time	t_{WL}	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock high time	t_{WH}	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{card} \leq 10$ pF (1 card)
Clock fall time	t_{THL}		3	ns	$C_{card} \leq 10$ pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	2		ns	$C_{card} \leq 10$ pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	$C_L \leq 40$ pF (1 card)
Output Hold time	T_{OH}	2.5		ns	$C_L \leq 15$ pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

4.2.3 SD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes)

Input:

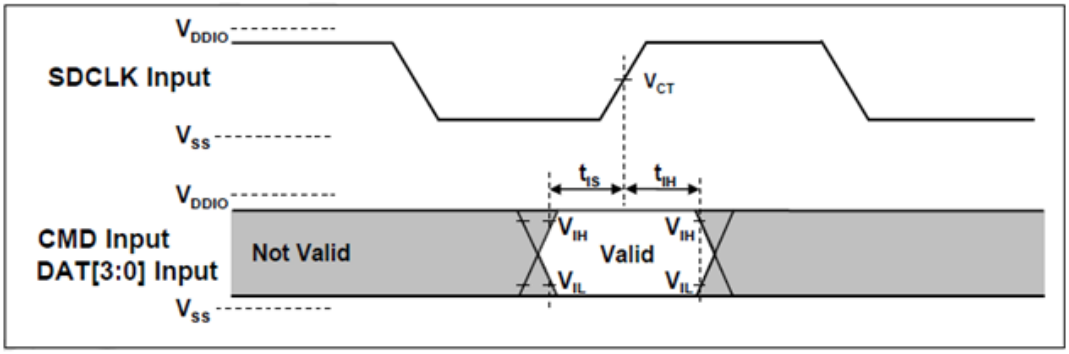


Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Clock Signal Timing

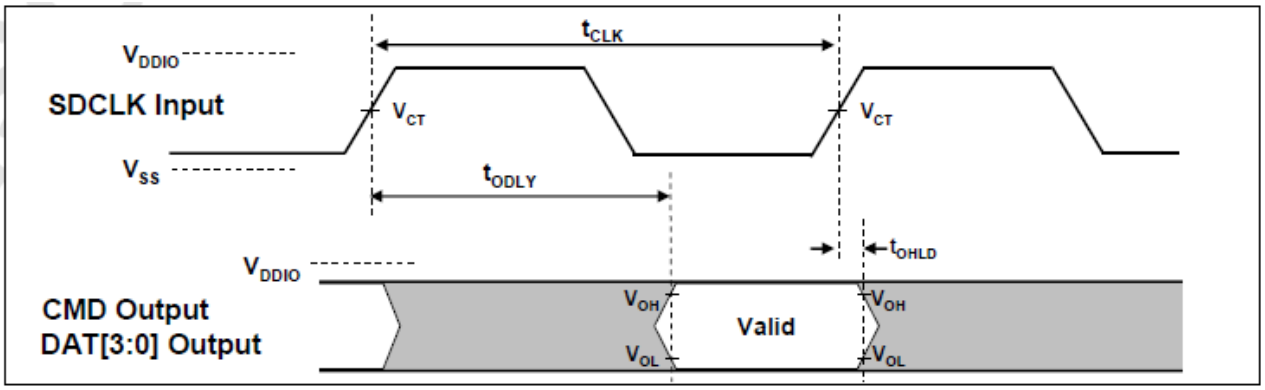
SDR50 and SDR104 Input Timing:



Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V

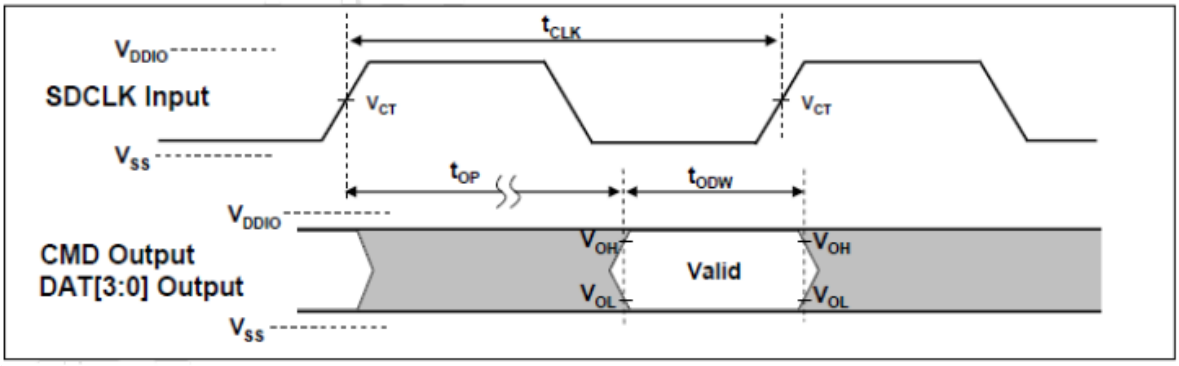
***Output* (SDR12, SDR25, SDR50):**



Output Timing of Fixed Data Window

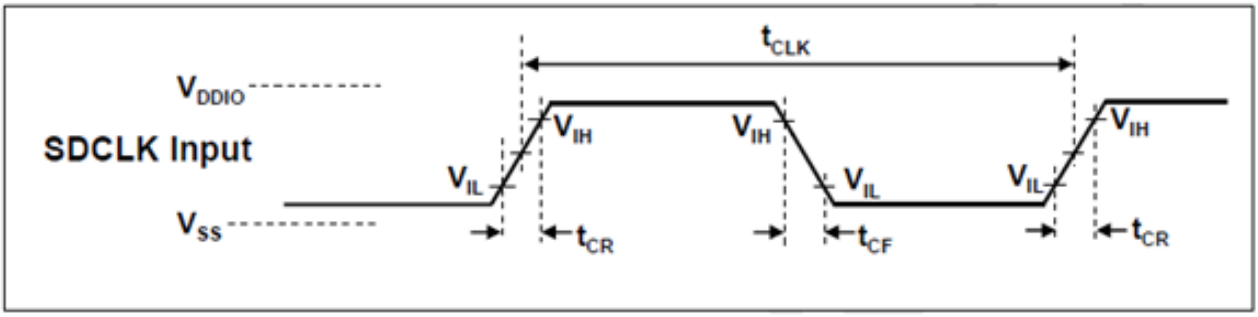
Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12,
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

Output (SDR104 Mode):



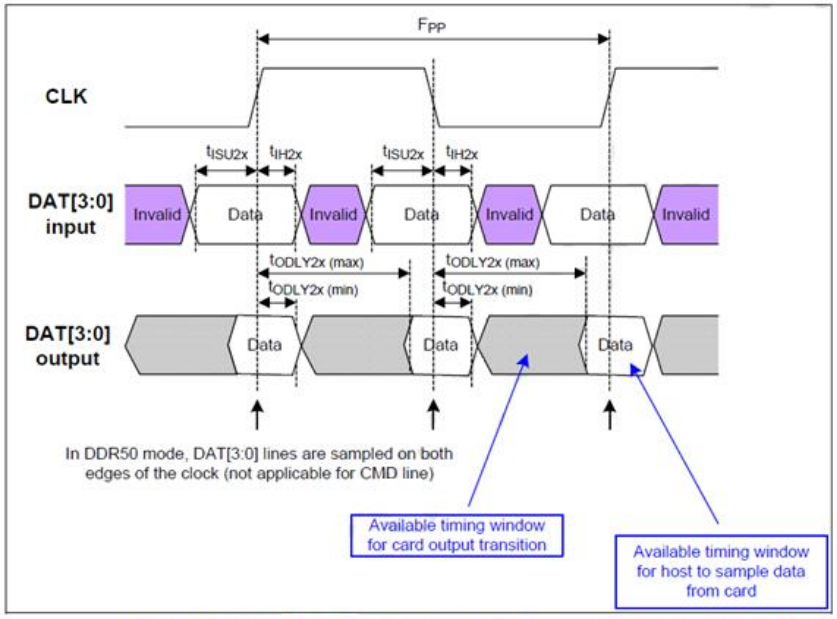
Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

4.2.4 SD Interface timing (DDR50 Modes)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	



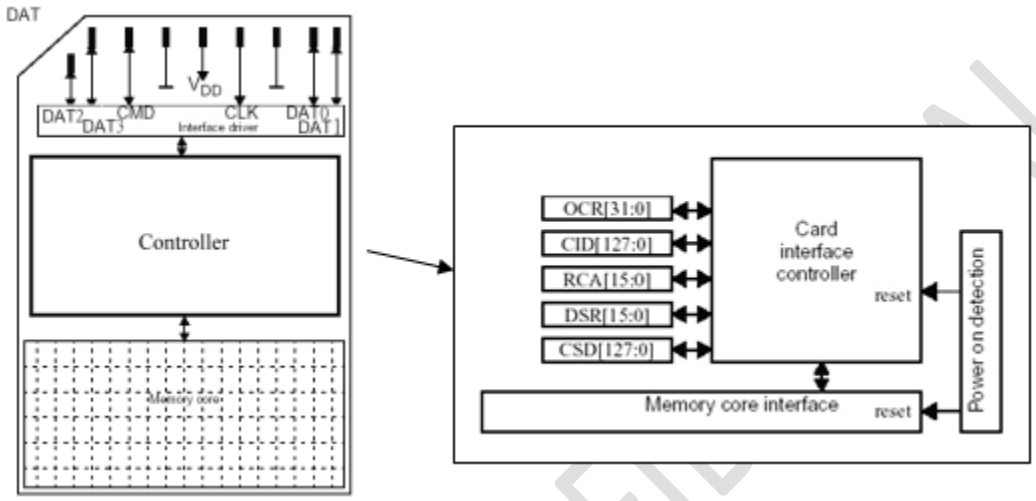
Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤ 30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥ 15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤ 25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥ 15 pF (1 card)

Table 4-6 Bus Timings – Parameters Values (DDR50 Mode)

5. PAD ASSIGNMENT

5.1 Pad Assignment and Descriptions



pin	SD Mode			SPI Mode		
	Name	**Type[1]**	**Description**	**Name**	**Type**	**Description**
1	CD/DAT3 [2]	I/O/PP [3]	Card Detect/ Data Line[bit3]	CS	I [3]	Chip Select (net true)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	VSS	S	Supply voltage ground
4	V_{DD}	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		
9	DAT2	I/O/PP	Data Line[bit2]	RSV		

Table 5-1 SD Memory Card Pad Assignment

(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode as well while they are not used. It is defined so in order to keep compatibility to MultiMedia Cards.

(3) At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

SET_CLR_CARD_DETECT (ACMD42) command.

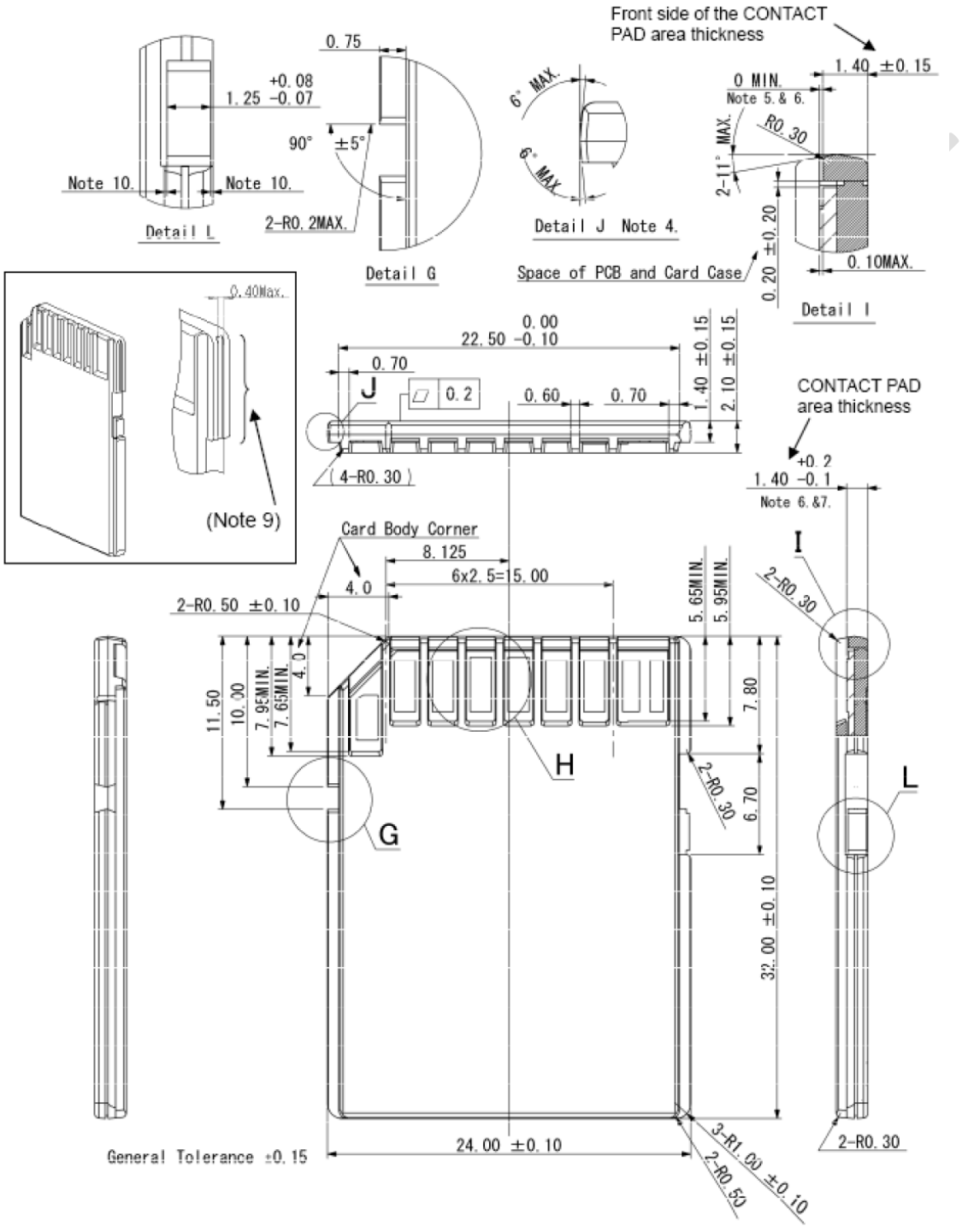
6. REGISTERS

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification.
RCA	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization.
DSR	16bit	Driver Stage Register; to configure the card's output drivers.
CSD	128bit	Card Specific Data; Information about the card operation conditions.
SCR	64bit	SD Configuration Register; Information about the SD Memory Card's Special Features capabilities
OCR	32bit	Operation conditions register.
SSR	512bit	SD Status; Information about the card proprietary features.
OCR	32bit	Card Status; Information about the card status.

Table 6-1 SD Registers

7. PHYSICAL DIMENSION

Dimension: 32mm(L) x 24mm(W) x 2.1mm(H)



8. ORDERING INFORMATION

Capacity	MPN (Diamond Grade)	MPN (Gold Grade)
32GB	FDMS032GBE-XS00	FDMS032GBG-XS00
64GB	FDMS064GBE-XS00	FDMS064GBG-XS00
128GB	FDMS128GBE-XS00	FDMS128GBG-XS00
256GB	FDMS256GBE-XS00	FDMS256GBG-XS00
512GB	FDMS512GBE-XS00	-

REVISION HISTORY

Revision	Date	History
1.0	2023/09	First Release