PCIe M.2 2280 Specification

(HIX Series)

Version 1.3

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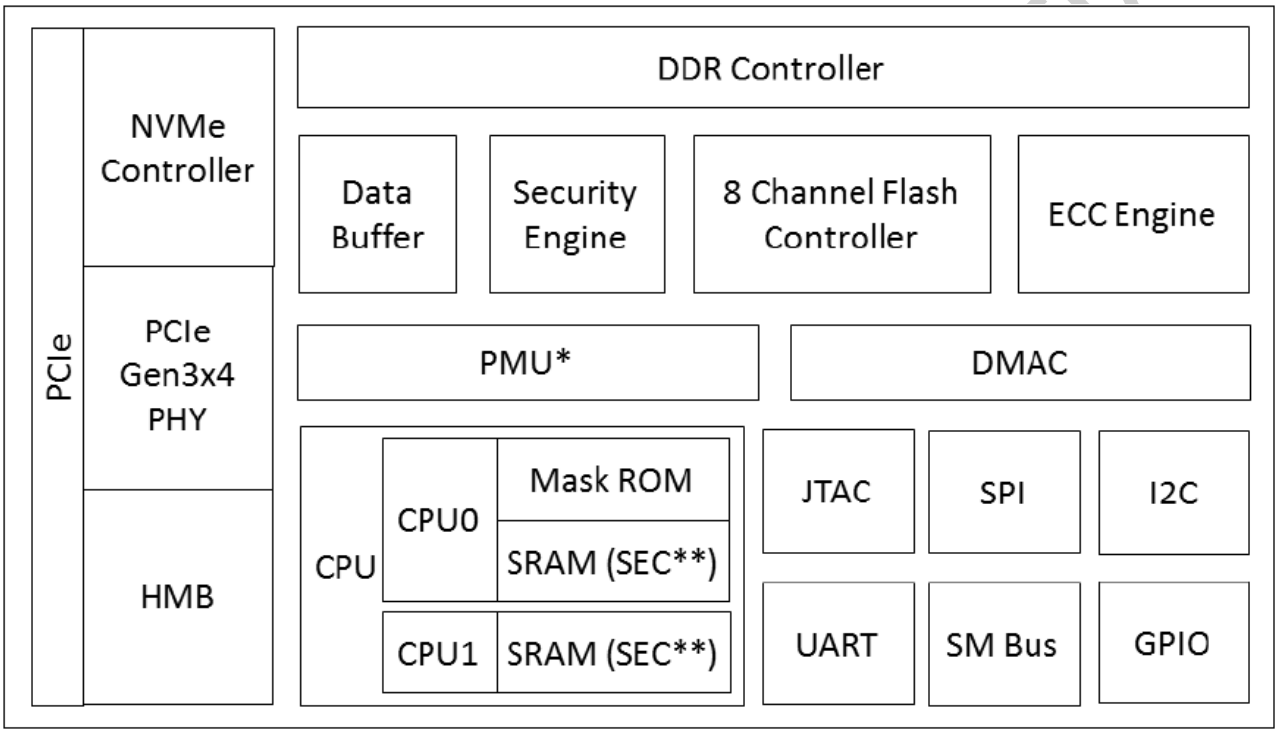
1. GENERAL DESCRIPTION

1.1. Introduction

FLEXXON's HIX PCIe M.2 2280 has PCIe Gen3x4 interface, and is fully compliant with NVMe 1.3 industrial standard. It supports ultimate performance, high density and great reliability, suitable for enterprise application.



PMU*: Power Management Unit

****SEC: Single bit Error Correct**

Figure 1-1 HIX PCIe M.2 2280 Controller Block Diagram

1.2. Product Overview

- **Capacity**
  - 128GB~4TB
- **PCIe Interface**
  - Compliant with NVMe 1.3
  - Compatible with PCIe I/II/III x4 interface
  - Support up to queue depth 64K
  - Support power management
- **ECC Scheme**
  - HIX PCIe M.2 2280 applies the LDPC (Low Density Parity Check) of ECC algorithm
- **GPIO**
- **UART**
- **Dynamic and Static Wear Leveling**
- **Support SMART and TRIM commands**
- **Power Loss Protection Algorithm**
- **Support Pyrite/AES256/TCG OPAL (OPTIONAL)**
- **Temperature Range**
  - Operation : 0°C ~ 70°C
  - Storage: -40°C ~ 85°C
- **RoHS Compliant**

2. PRODUCT SPECIFICATIONS

2.1. Performance

Table 2-1 Performance of HIX PCIe M.2 2280

Capacity	Sequential (max)		Random (max)	
	Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
128GB~4TB	3,390	3,000	680,000	650,000

NOTES:

1. Performance may differ according to flash configuration and platform.

2.2. Power

Table 2-2 Supply Voltage of HIX PCIe M.2 2280

Parameter	Rating
Operating Voltage	3.14V ~ 3.47V

2.3. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The predicted result of FLEXXON's HIX PCIe M.2 2280 is more than 2 million hours.

2.4. Data Retention

- 10 years if > 90% life remaining (@25C)
- 1 year if < 10% life remaining (@25C)

3. ENVIRONMENTAL SPECIFICATIONS

Test Items	Test Conditions
Storage Temperature	-40°C ~ 85°C
Operating Temperature	0°C ~ 70°C
Storage Humidity	40°C, 93% RH
Operating Humidity	40°C, 90% RH
Shock	1500G, Half Sin Pulse Duration 0.5ms
Vibration	80Hz ~ 2000Hz/20G, 20Hz ~ 80Hz/1.52mm, 3 axis/60min
Drop	80cm free fall, 6 face of each unit
Bending	≥ 20N, Hold 1 min/5 times
Torque	0.5N-m, Hold 1 min/5 times
ESD	24°C, 49% RH, +/-4KV

4. SUPPORTED COMMANDS

Table 4-1 Admin Commands

Identifier	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature
0Ah	Get Feature
0Ch	Asynchronous Event Request
10h	Firmware Commit
11h	Firmware Image Download
14h	Device Self-test
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

Table 4-2 I/O Commands

Identifier	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

Table 4-3 Set Feature Commands

Identifier	Command Description
00h	Reserved
01h	Arbitration
02h	Power Management
03h	LBA Range Type
04h	Temperature Threshold
05h	Error Recovery
06h	Volatile Write Cache
07h	Number of Queues
08h	Interrupt Coalescing
09h	Interrupt Vector Configuration
0Ah	Write Atomicity Normal
0Bh	Asynchronous Event Configuration
0Ch	Autonomous Power State Transition
0Dh	Host Memory Buffer
0Eh	Timestamp
10h	Host Controlled Thermal Management
11h	Non-Operational Power State Config
0Eh-7Dh	Reserved
80h	Software Progress Marker

Table 4-4 Get Log Page Commands

Identifier	Command Description
00h	Reserved
01h	Error Information
02h	SMART / Health Information
03h	Firmware Slot Information
04h	Changed Namespace List
06h	Device Self-test
09h-07h	Reserved
81h	Sanitize Status
82h-FFh	Reserved

5. PIN ASSIGNMENT

Table 5-1 Pin Assignment and Description of HIX PCIe M.2 2280

Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = GND
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect

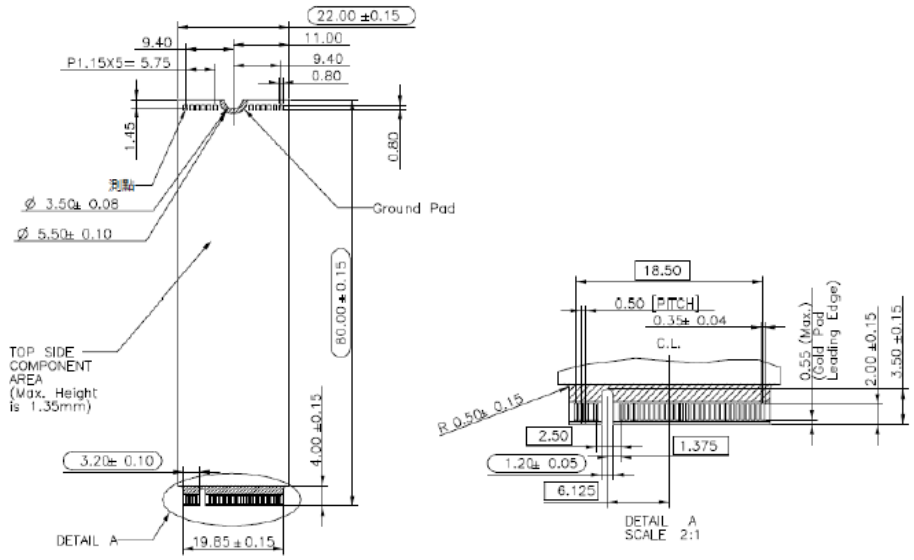
Pin No.	PCIe Pin	Description
23	PERn2	PCIe RX Differential signal defined by PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O) (0/1.8V)	SMBus Clock; Open Drain with pull-up on platform
41	PETn0	PCIe TX Differential signal defined by PCI Express M.2 spec
42	SMB_DATA (I/O) (0/1.8V)	SMBus Data; Open Drain with pull-up on platform
43	PETp0	PCIe TX Differential signal defined by PCI Express M.2 spec
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active Low

Pin No.	PCIe Pin	Description
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active low
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data Line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock Line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	

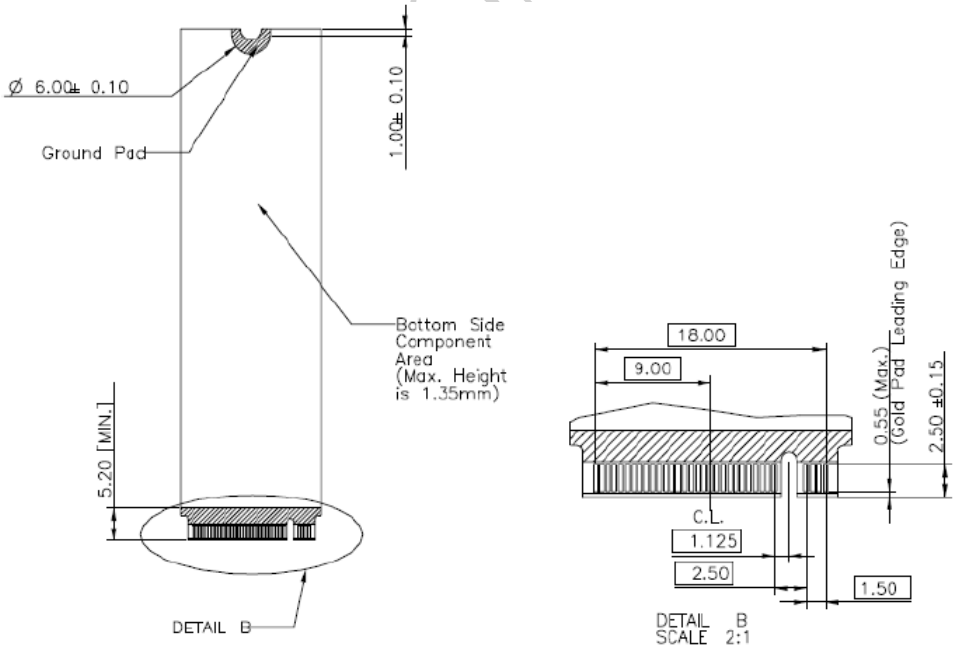
Pin No.	PCIe Pin	Description
67	N/C	No connect
68	SUSCLK (32KHz) (I)(0/3.3V)	32.768 KHz clock supply input that is provided by the platform chipset to reduce power and cost of the module.
69	NC	PEDET (NC-PCIe)
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

6. PHYSICAL DIMENSION

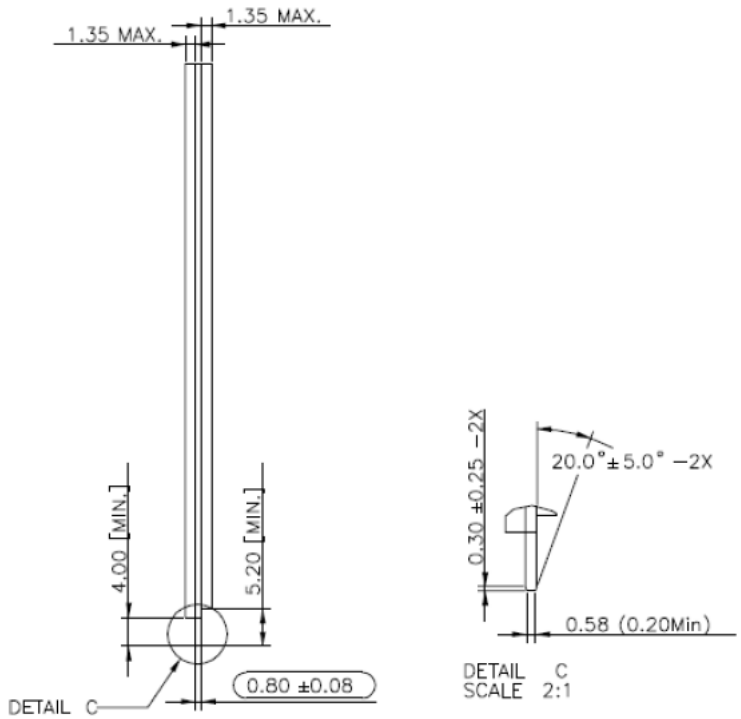
Dimension: 80mm(L) x 22mm(W) x 2.3mm(H)



Top View



Bottom View



Side View

7. ORDERING INFORMATION

Capacity	MPN
128GB	FCSO128G-P3H
120GB	FCSO120G-P3H
256GB	FCSO256G-P3H
240GB	FCSO240G-P3H
512GB	FCSO512G-P3H
480GB	FCSO480G-P3H
1TB	FCSO001T-P3H
960GB	FCSO960G-P3H
2TB	FCSO002T-P3H
1920GB	FCSO1920-P3H
4TB	FCSO004T-P3H
3840GB	FCSO3840-P3H

Revision History

Revision	Date	Description
1.0	2019/09	First release
1.1	2020/04	Update performance
1.2	2020/05	Update TBW
1.3	2022/12	Update capacity