Data Sheet

ADCA5192

5 MHz to 1794 MHz Broadband CATV Amplifier

FEATURES

- Highly flexible: bias at 5 V from 500 mW to 1.5 W for downstream applications, or as low as 250 mW for upstream applications
- Excellent linearity: NPR (MER) > 50 dB over broad input power range
- High gain: 17.0 dB at 1794 MHz
- Low noise figure (includes input balun and trace losses)
  - 1.7 dB at 108 MHz
  - 2.9 dB at 1794 MHz
- Excellent S11 return losses:
  - −20 dB from 108 MHz to 1218 MHz
  - −19 dB from 1218 MHz to 1794 MHz
- 20-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- 54 MHz to 1794 MHz CATV infrastructure amplifier systems
- 5 MHz to 684 MHz upstream
- Remote physical layer (PHY)
- DOCSIS 3.1 and DOCSIS 4.0 compliant

FUNCTIONAL BLOCK DIAGRAM

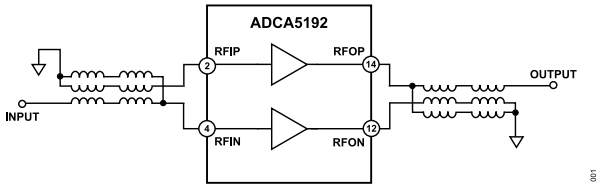

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADCA5192 is a low power, low noise gain block amplifier that provides excellent linearity across a flexible bias range allowing power efficient design implementation for various applications.

The device provides 17.0 dB of flat gain up to 1794 MHz, making this ideal for Data Over Cable Service Interface Specification (DOCSIS®) 4.0 downstream applications. The device is also well suited for upstream applications to 684 MHz as an input or intermediate stage. The device is conveniently packaged in an industry-standard, 20-lead, 4 mm × 4 mm lead frame chip-scale package (LFCSP) with an exposed pad on the bottom of the package for improved thermal performance.

Rev. 0

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REVISION HISTORY

1/2024—Revision 0: Initial Version

SPECIFICATIONS

GENERAL DOWNSTREAM PERFORMANCE

See the application circuit in Figure 37. Supply voltage (V_{DD}) = 5.0 V, supply current (I_{DD}) = 250 mA, paddle temperature (T_{PADDLE}) = 35 °C, and source impedance (Z_S) = load impedance (Z_L) = 75 Ω, unless otherwise noted.

Table 1. Downstream Performance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER GAIN	S21		17.2		dB	Frequency (f) = 108 MHz
			17.0		dB	f = 1218 MHz
			17.0		dB	f = 1794 MHz
SLOPE OF STRAIGHT LINE[1]			−0.2		dB	f = 108 MHz to 1218 MHz
			−0.2		dB	f = 108 MHz to 1794 MHz
FLATNESS OF FREQUENCY RESPONSE[2]			0.1		dB	f = 108 MHz to 1794 MHz
REVERSE ISOLATION	S12		−21.5		dB	f = 108 MHz to 1794 MHz
RETURN LOSS						
Input	S11		−20		dB	f = 108 MHz to 1218 MHz
			−19		dB	f = 1218 MHz to 1794 MHz
Output	S22		−17		dB	f = 108 MHz to 1218 MHz
			−16		dB	f = 1218 MHz to 1794 MHz
NOISE FIGURE						Includes losses of baluns (0.9 dB at 1794 MHz) shown in the Downstream Application Circuit with Passive Biasing section
			1.7		dB	f = 108 MHz
			2.1		dB	f = 1218 MHz
			2.9		dB	f = 1794 MHz
SUPPLY						Supply voltage and current can be adjusted for different applications, see the Applications Information section
DC Current	I_{DD}		250		mA	Using the downstream applications circuit with passive biasing (see the Downstream Application Circuit with Passive Biasing section); can be adjusted between 100 mA and 300 mA (see the Supply Voltage and Bias Current section and Figure 17 through Figure 21)

[1] The slope is defined as the delta of the gain at the start frequency and the gain at the stop frequency.

[2] Flatness is defined as the maximum deviation from a linear best-fit of the gain in the frequency range of operation.

SPECIFICATIONS

GENERAL UPSTREAM PERFORMANCE

See the application circuit in Figure 39. Supply voltage (V_{DD}) = 5.0 V, supply current (I_{DD}) = 100 mA, paddle temperature (T_{PADDLE}) = 35 °C, and source impedance (Z_S) = load impedance (Z_L) = 75 Ω, unless otherwise noted.

Table 2. Upstream Performance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER GAIN	S21		16.5		dB	f = 5 MHz
			16.2		dB	f = 684 MHz
SLOPE OF STRAIGHT LINE[1]			−0.3		dB	f = 5 MHz to 684 MHz
FLATNESS OF FREQUENCY RESPONSE[2]			0.2		dB	f = 5 MHz to 684 MHz
REVERSE ISOLATION	S12		−21		dB	f = 5 MHz to 684 MHz
RETURN LOSS						
Input	S11		−19		dB	f = 5 MHz to 258 MHz
			−19		dB	f = 258 MHz to 684 MHz
Output	S22		−22		dB	f = 5 MHz to 258 MHz
			−22		dB	f = 258 MHz to 684 MHz
NOISE FIGURE						Includes losses of baluns (0.6 dB at 684 MHz) shown in the Upstream Application Circuit section
			2.1		dB	f = 108 MHz
			2.3		dB	f = 684 MHz
SUPPLY						Supply voltage and current can be adjusted for different applications, see the Applications Information section
DC Current	I_{DD}		100		mA	Using the upstream applications circuit (see the Upstream Application Circuit section); can be adjusted between 50 mA and 250 mA (see the Supply Voltage and Bias Current section and Figure 30 through Figure 32)

[1] The slope is defined as the delta of the gain at the start frequency and the gain at the stop frequency.

[2] Flatness is defined as the maximum deviation from a linear best-fit of the gain in the frequency range of operation.

SPECIFICATIONS

DISTORTION DATA

Downstream All Digital Channel Plan, 258 MHz to 1794 MHz

See the application circuit in Figure 37. V_{DD} = 5.0 V, I_{DD} = 250 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 3. Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO[1]	NPR					
			54		dB	0 dB tilt, no offset, total composite power (TCP) = 58 dBmV, V_{DD} = 5.0 V, I_{DD} = 250 mA
			60/50[2]		dB	0 dB tilt, 6 dB offset at 1218 MHz, TCP = 58 dBmV, V_{DD} = 5.0 V, I_{DD} = 250 mA
			55		dB	10 dB tilt, no offset, TCP = 58 dBmV, V_{DD} = 5.0 V, I_{DD} = 250 mA
			58/53[2]		dB	10 dB tilt, 6 dB offset at 1218 MHz, TCP = 58 dBmV, V_{DD} = 5.0 V, I_{DD} = 250 mA

[1] The noise power ratio gives an equivalent result to the standard modulation error rate (MER) testing but with improved dynamic range using an industry-accepted method. Equivalent to carrier to composite noise (CCN)

[2] Typical is below or above offset.

Downstream All Digital Channel Plan, 108 MHz to 1218 MHz

See the application circuit in Figure 37. V_{DD} = 5.0 V, I_{DD} = 250 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 4. Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO[1]	NPR					
			56		dB	0 dB tilt, TCP = 60 dBmV, V_{DD} = 5.0 V, I_{DD} = 250 mA
			50		dB	10 dB tilt, TCP = 60 dBmV, V_{DD} = 5.0 V, I_{DD} = 250 mA

[1] The noise power ratio gives an equivalent result to the standard MER testing but with improved dynamic range using an industry-accepted method. Equivalent to carrier to composite noise (CCN)

Upstream All Digital Channel Plan

See the application circuit in Figure 39. V_{DD} = 5.0 V, I_{DD} = 100 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 5. Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO	NPR					
			50		dB	3 dB tilt, TCP = 54 dBmV, 54 to 684 MHz, V_{DD} = 5.0 V, I_{DD} = 100 mA

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	
DC Supply over Voltage (5 Minutes)	10 V
I_{DD} Bias Supply Current	400 mA
RF Input Power	60 dBmV
Temperature	
Operating Range, T_{PADDLE}	−40°C to +100°C
Peak Reflow (Moisture Sensitivity Level (MSL) 3)	260°C
Junction (T_J) to Maintain 1 Million Hour Mean Time to Failure (MTTF)	150°C
Nominal Junction (T_J)	
T_{PADDLE} = 100 °C, I_{DD} = 250 mA, V_{DD} = 5.0 V	121°C
Storage (T_S) Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the thermal resistance from the operating portion of the pseudomorphic, high electron mobility transistor (pHEMT) device to the outside surface of the package closest to the device mounting area (the exposed pad on the bottom of the case). See the Thermal Considerations section for additional information.

Table 7. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-20-6	17.0	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADCA5192

Table 8. ADCA5192, 20-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	350	Class 1A, passed

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

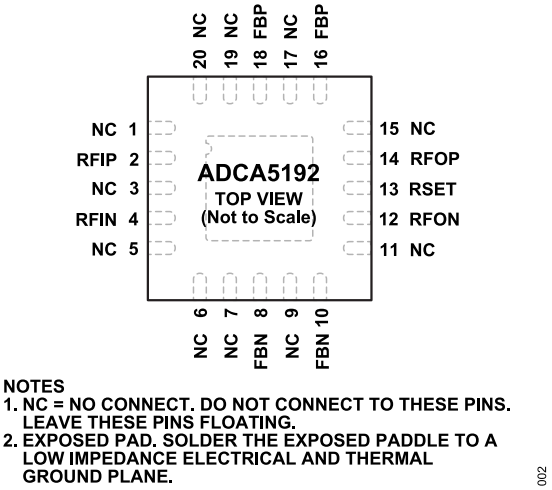

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5, 6, 7, 9, 11, 15, 17, 19, 20	NC	No Connect. Do not connect to these pins. Leave these pins floating.
2	RFIP	Positive RF Amplifier Input. RFIP and RFIN form a differential input.
4	RFIN	Negative RF Amplifier Input. RFIP and RFIN form a differential input.
8, 10	FBN	Feedback Path (Negative Side). Place an 0201 capacitor between Pin 8 and Pin 10. See Figure 37 for specific recommendations.
12	RFON	Negative Amplifier RF Output. A choke inductor is required to provide DC current and RF isolation. A DC blocking capacitor is also required. See Figure 37 for specific recommendations.
13	RSET	Bias Resistor. The voltage must be pulled up or down depending on target application and current (see Table 10 for downstream and Upstream Application Circuit for upstream.
14	RFOP	Positive Amplifier RF Output. A choke inductor is required to provide DC current and RF isolation. A DC blocking capacitor is also required. See Figure 37 for specific recommendations.
16, 18	FBP	Feedback Path (Positive Side). Place an 0201 capacitor between Pin 16 and Pin 18. See Figure 37 for specific recommendations.
	EPAD	Exposed Pad. Solder the exposed paddle to a low impedance electrical and thermal ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5.0 V, I_{DD} = 250 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

S-PARAMETERS FOR DOWNSTREAM APPLICATION (SEE FIGURE 37)

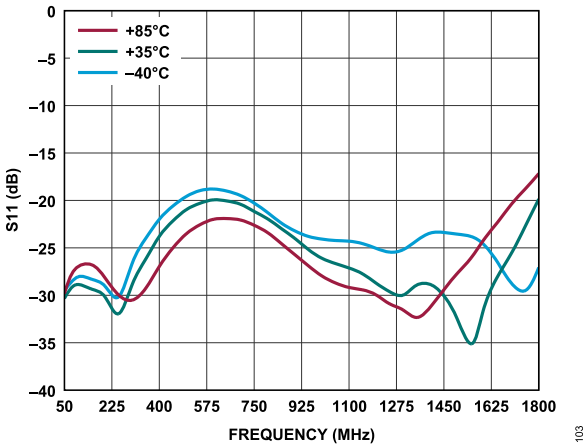

Figure 3. Downstream S11 vs. Frequency Over Temperature

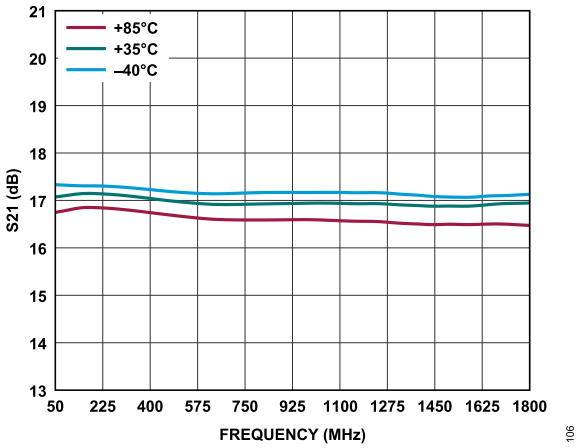

Figure 6. Downstream S21 vs. Frequency Over Temperature

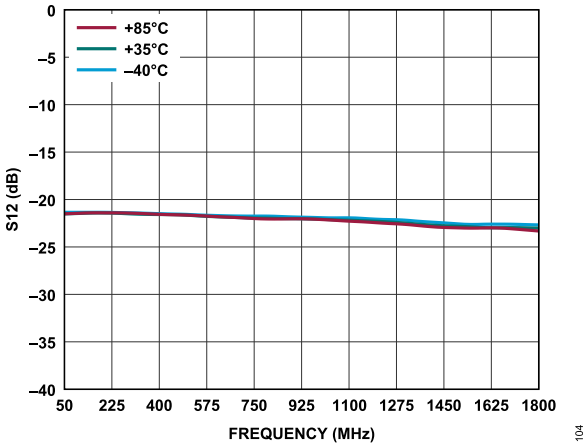

Figure 4. Downstream S12 vs. Frequency Over Temperature

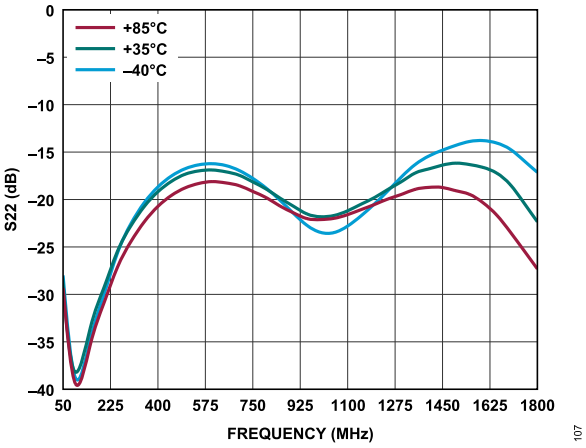

Figure 7. Downstream S22 vs. Frequency Over Temperature

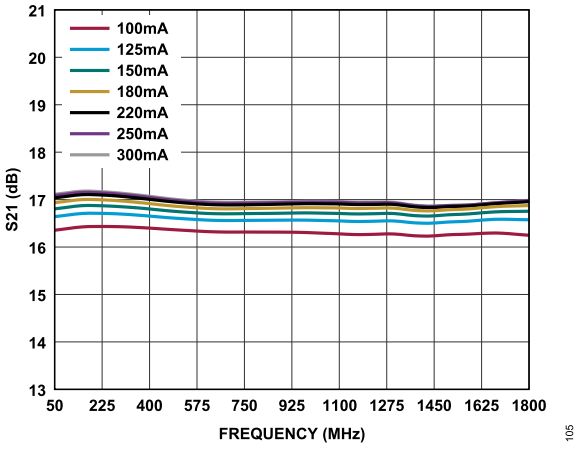

Figure 5. S21 vs. Frequency Over Bias Current

TYPICAL PERFORMANCE CHARACTERISTICS

S-PARAMETERS FOR UPSTREAM APPLICATION (SEE FIGURE 39)

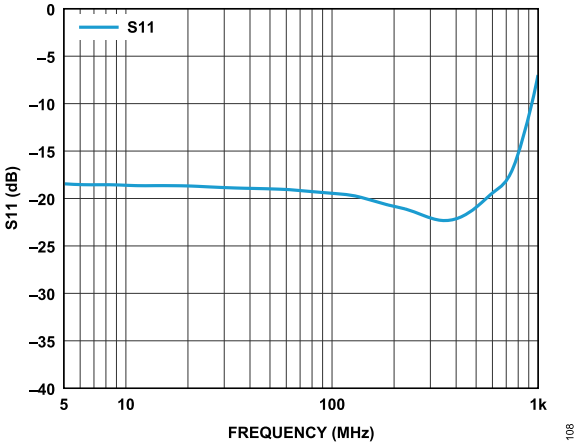

Figure 8. Upstream S11 vs. Frequency

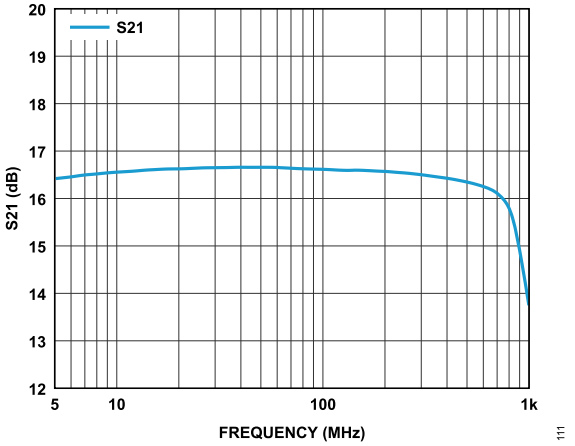

Figure 11. Upstream S21 vs. Frequency

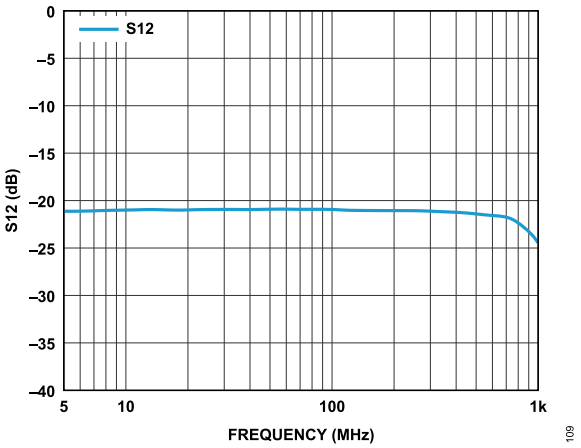

Figure 9. Upstream S12 vs. Frequency

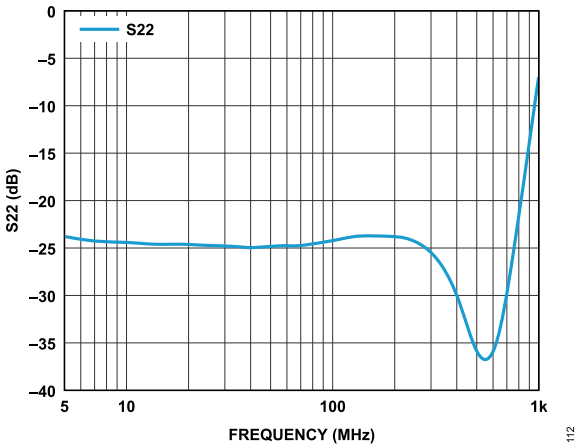

Figure 12. Upstream S22 vs. Frequency

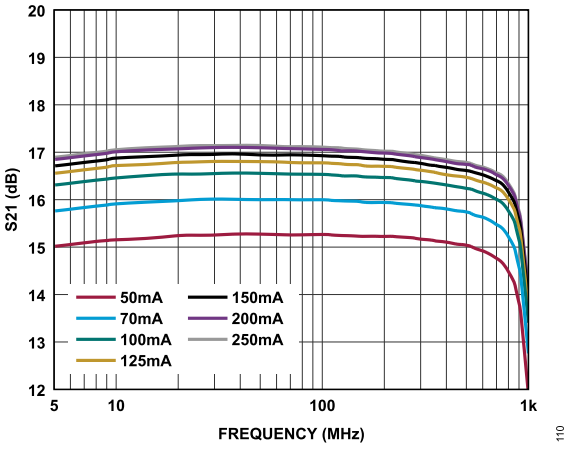

Figure 10. Upstream S21 vs. Frequency Over Bias Current

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS 4.0 DOWNSTREAM PERFORMANCE (SEE FIGURE 37)

256×, ITU-T J.83B, SCQAM 6 MHz channels, 258 MHz to 1794 MHz, no offset, V_{DD} = 5.0 V, I_{DD} = 250 mA, unless otherwise noted.

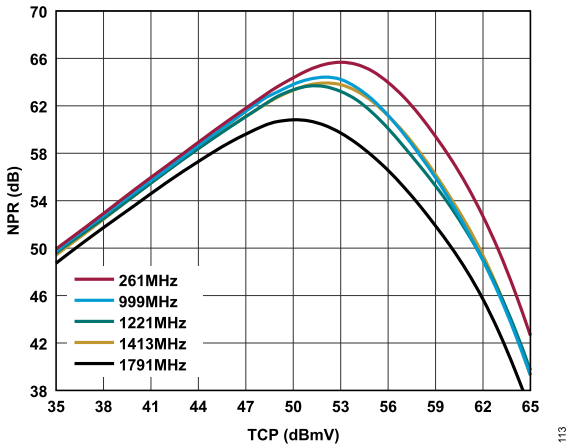

Figure 13. NPR vs. TCP Over Frequency, 0 dB Tilt

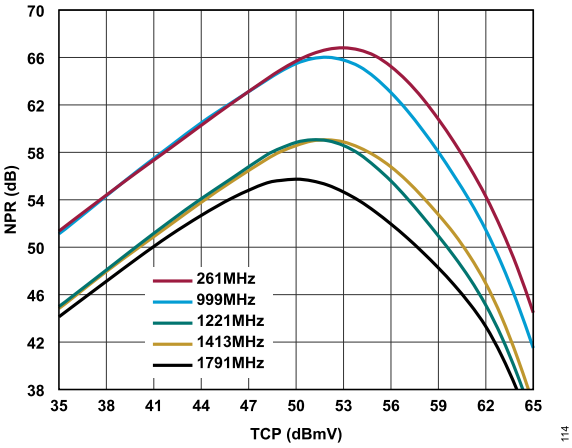

Figure 14. NPR vs. TCP Over Frequency, 0 dB Tilt, 6 dB Offset at 1218 MHz

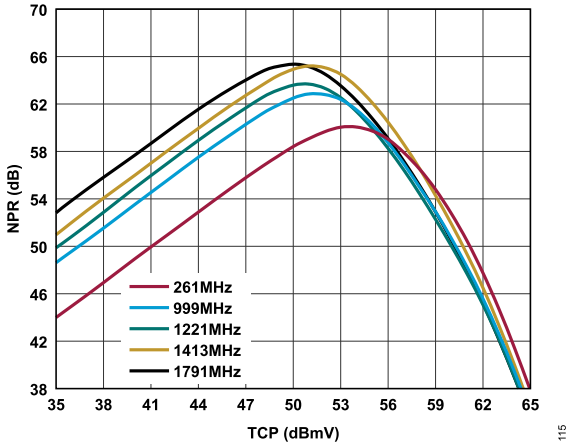

Figure 15. NPR vs. TCP Over Frequency, 10 dB Tilt, No Offset

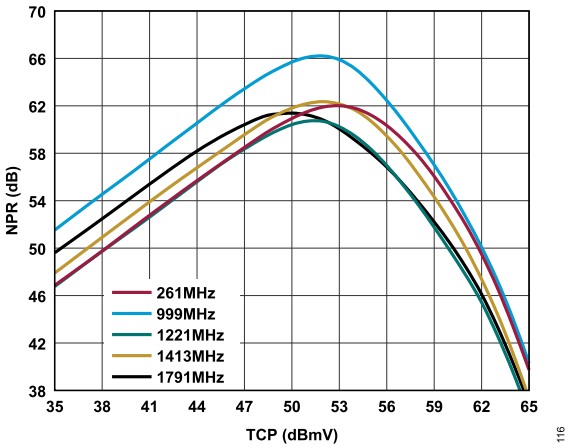

Figure 16. NPR vs. TCP Over Frequency, 10 dB Tilt, 6 dB Offset at 1218 MHz

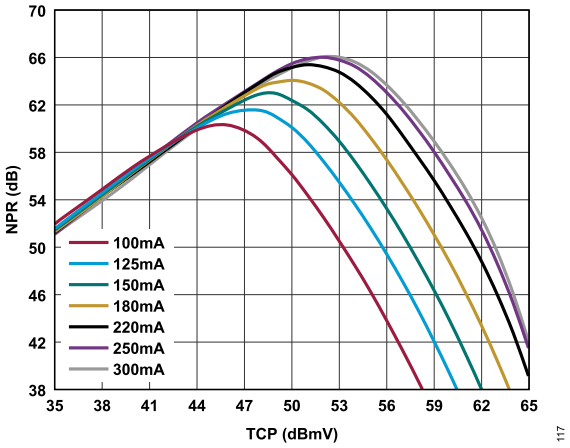

Figure 17. NPR vs. TCP Over Current, 0 dB Tilt, 261 MHz

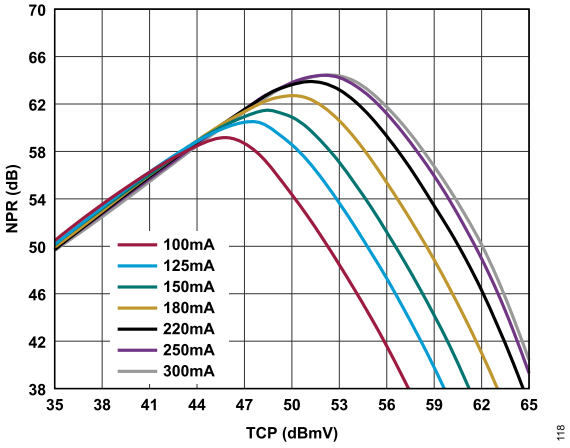

Figure 18. NPR vs. TCP Over Current, 0 dB Tilt, 999 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

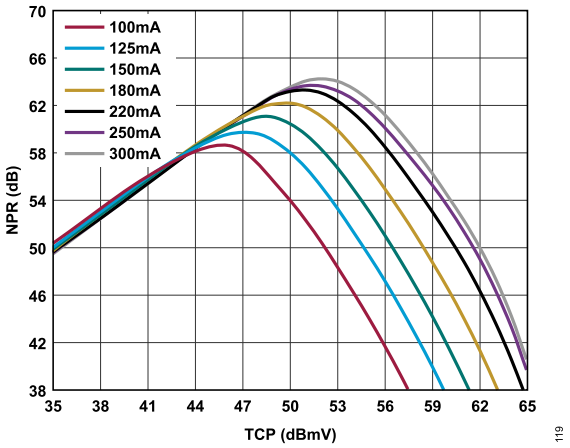

Figure 19. NPR vs. TCP Over Current, 0 dB Tilt, 1221 MHz

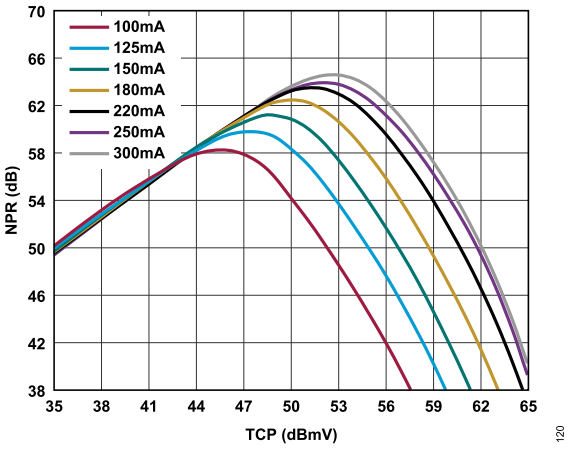

Figure 20. NPR vs. TCP Over Current, 0 dB Tilt, 1413 MHz

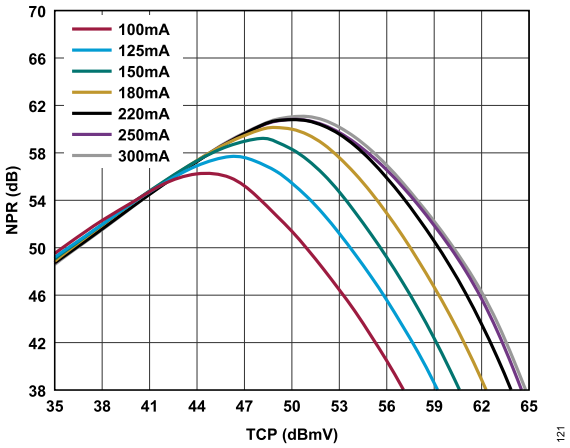

Figure 21. NPR vs. TCP Over Current, 0 dB Tilt, 1791 MHz

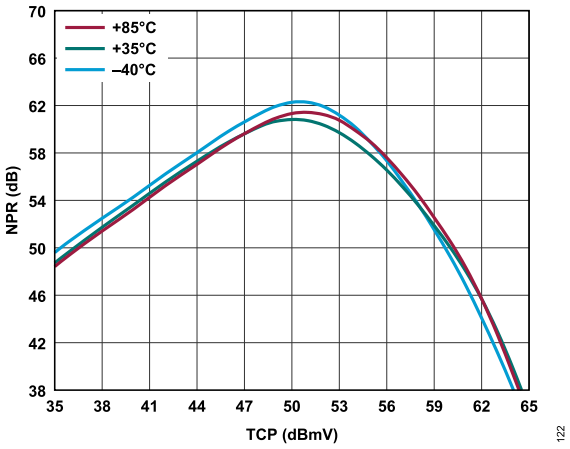

Figure 22. NPR vs. TCP Over Temperature, 0 dB Tilt, 1791 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS 3.1 DOWNSTREAM PERFORMANCE (SEE FIGURE 37)

185×, ITU-T J.83B, SCQAM 6 MHz channels, and 108 MHz to 1218 MHz, unless otherwise noted, V_{DD} = 5.0 V, I_{DD} = 250 mA, unless otherwise noted.

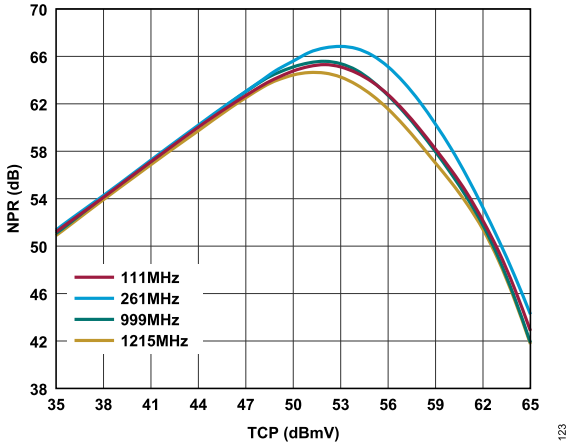

Figure 23. NPR vs. TCP Over Frequency, 0 dB Tilt

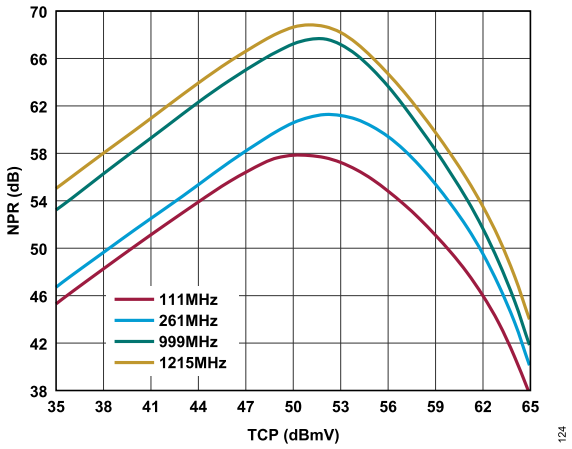

Figure 24. NPR vs. TCP Over Frequency, 10 dB Tilt

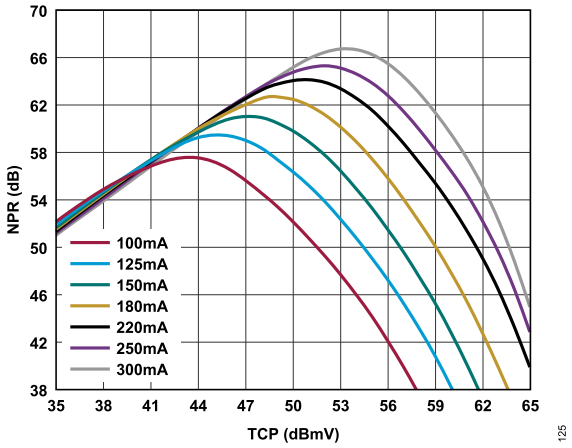

Figure 25. NPR vs. TCP Over Current, 0 dB Tilt, 111 MHz

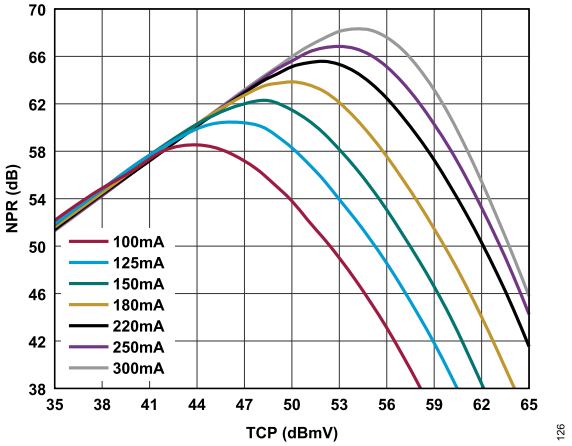

Figure 26. NPR vs. TCP Over Current, 0 dB Tilt, 261 MHz

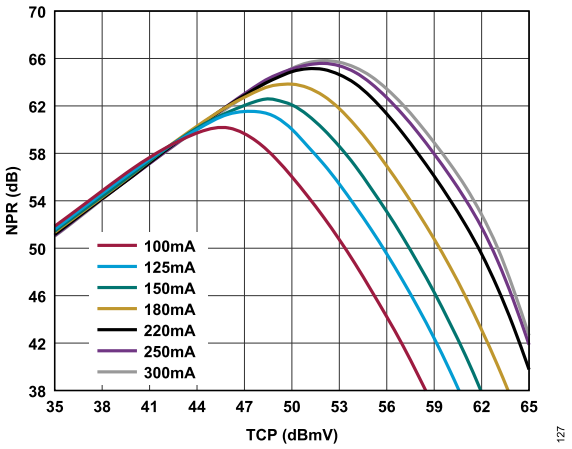

Figure 27. NPR vs. TCP Over Current, 0 dB Tilt, 999 MHz

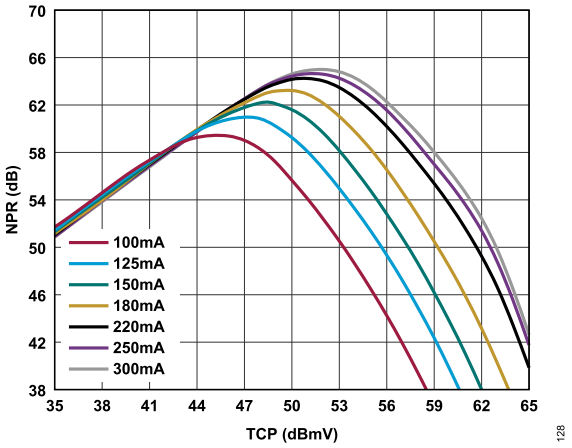

Figure 28. NPR vs. TCP Over Current, 0 dB Tilt, 1215 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS 4.0 UPSTREAM PERFORMANCE (SEE FIGURE 39)

105×, ITU-T J.83B, SCQAM 6 MHz channels, 54 MHz to 684 MHz, V_{DD} = 5.0 V, I_{DD} = 100 mA, unless otherwise noted.

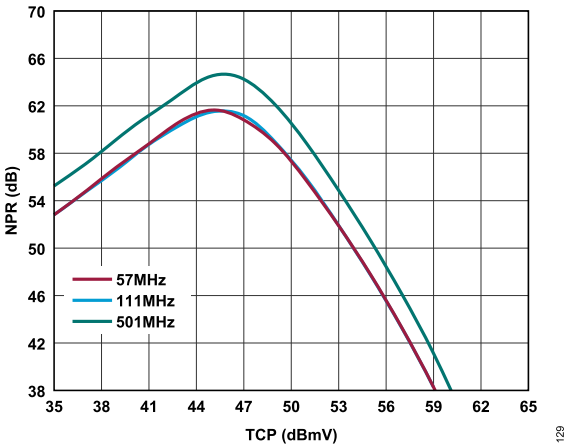

Figure 29. NPR vs. TCP Over Frequency, 3 dB Tilt

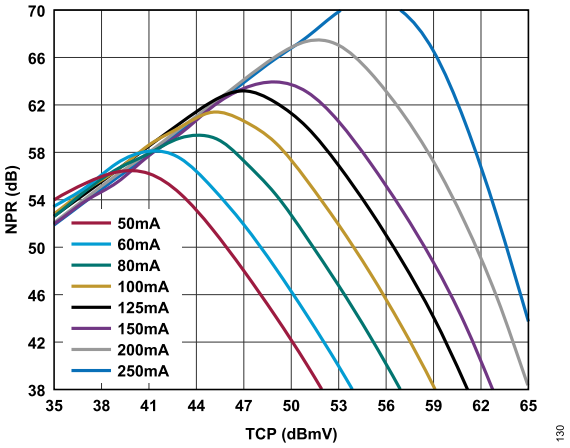

Figure 30. NPR vs. TCP Over Current, 3 dB Tilt, 57 MHz

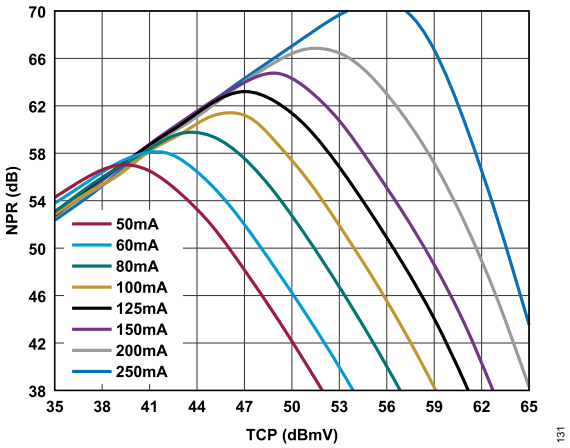

Figure 31. NPR vs. TCP Over Current, 3 dB Tilt, 111 MHz

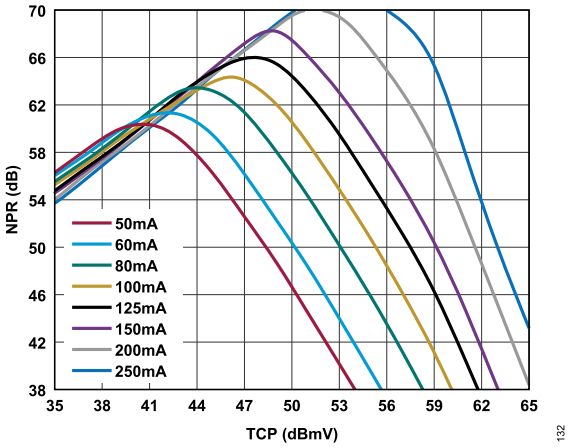

Figure 32. NPR vs. TCP Over Current, 3 dB Tilt, 501 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

NOISE PERFORMANCE

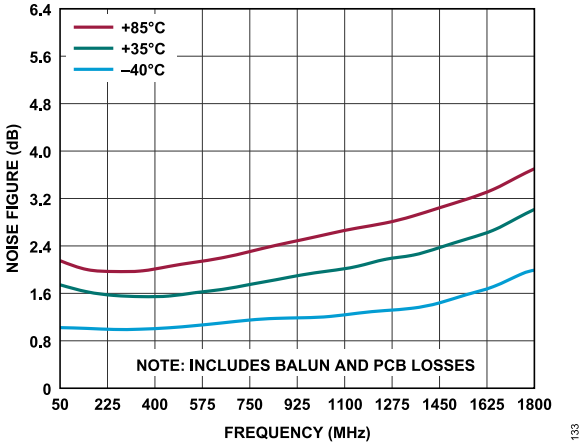

Figure 33. Noise Figure vs. Frequency Over Temperature, V_{DD} = 5.0 V, I_{DD} = 250 mA

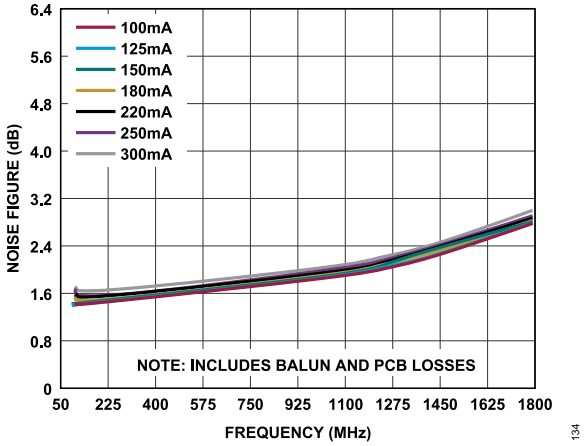

Figure 34. Noise Figure vs. Frequency Over Current, V_{DD} = 5.0 V, T_{PADDLE} = 35°C

THEORY OF OPERATION

The ADCA5192 is a single-die, 1800 MHz differential cascode amplifier fabricated on a linear gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT) process. The device provides general-purpose linear gain suitable for a wide range of applications.

When used with a recommended balun, the ADCA5192 can achieve a 2.9 dB noise figure at 1794 MHz (2.1 dB noise figure at 1218 MHz) while providing excellent linearity for extended spectrum line extender input stage applications.

The device has suitable drive capability to overcome nominal insertion losses introduced from automatic gain control and tilt functions.

The ADCA5192 can also serve in several positions for the upstream path at any DOCSIS 4.0 frequency split.

Depending on the application, the ADCA5192 can be biased from 50 mA to 300 mA.

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

The ADCA5192 is packaged in a thermally efficient, 20-lead LFCSP. The thermal resistance from junction to case, θ_{JC}, is 17.0°C/W, where the case is defined by the exposed pad on the bottom of the package. For the best thermal performance, it is recommended to add as many thermal vias as possible under the exposed pad of the LFCSP. Thermal transfer is maximized when the amount of copper under the exposed pad is maximized. It is also recommended that the array of vias under the ADCA5192 interface to an external heat sink such as a pedestal on the system chassis.

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 35 shows the recommended land pattern for the ADCA5192. To minimize thermal impedance, the exposed pad on the 4 mm × 4 mm LFCSP is soldered to a ground plane. To improve thermal dissipation, 23 thermal vias are arranged in an array under the exposed pad. The array consists of alternating rows of five vias and four vias, maximizing the number of vias within the area. The area under the pad is also tied to ground on the bottom layer of the PCB. If multiple ground layers exist, tie these layers together by the vias. The external layer of the PCB must be a minimum of 1 oz. copper. The minimum average plated hole wall thickness of the vias must not be less than 0.001 inches.

For further information on optimizing the thermal performance while using the ADCA5192, refer to the AN-1604 Application Note, Thermal Management Calculations for RF Amplifiers in LFCSP and Flange Packages.

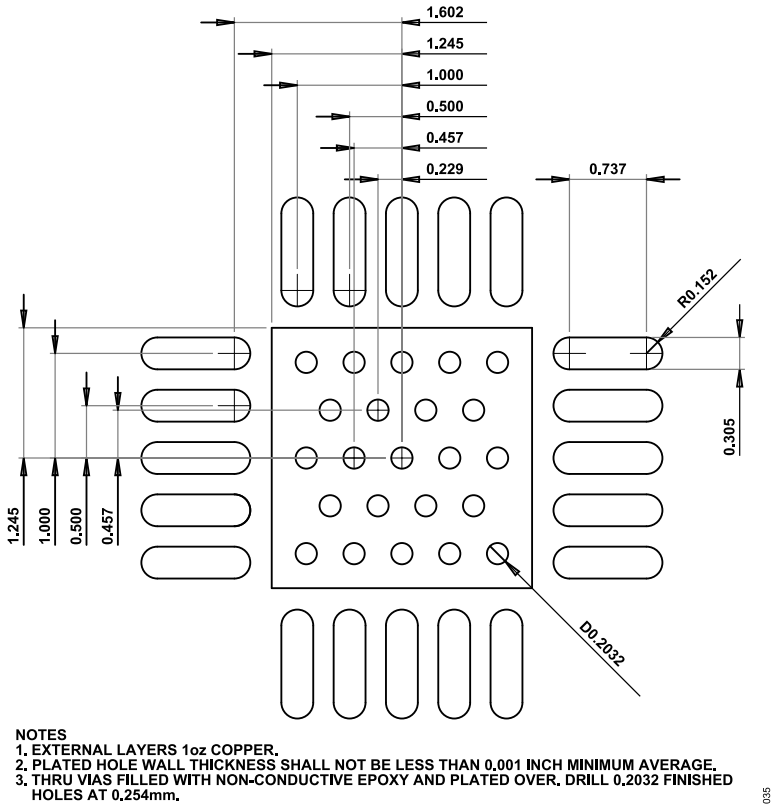

Figure 35. Recommended PCB Layout (Dimensions Shown in Millimeters)

APPLICATIONS INFORMATION

SUPPLY VOLTAGE AND BIAS CURRENT

The ADCA5192 provides flexible biasing options for various applications. The bias current can be adjusted between 100 mA and 300 mA nominal (for downstream) or 50 mA and 250 mA nominal (for upstream) to optimize power consumption and linearity for a given application. Set the RSET pin (Pin 13) to a corresponding voltage to optimize performance for a given bias current.

There are several options for setting the bias current, I_{DD}, of the ADCA5192. The passive bias approach is the most basic and provides a DC voltage at the RF inputs, RFIP (Pin 2) and RFIN (Pin 4), that is generated from a resistor divider (R3 and R4) off the V_{DD} supply rail, as seen in Figure 37. The output voltage of the resistor divider (V_{BIAS_ADJ}) is connected through two ferrite beads (E1 and E3) to the AC ground terminal of T1. This voltage also sets the DC bias at the outputs of T1, which drive the RF inputs. The typical relationship between V_{BIAS_ADJ} and I_{DD} is shown in Figure 36. This approach requires the fewest components, but process variation results in the bias current varying ~±20% from the typical I_{DD} value, which also affects device performance in the same way as intentionally adjusting the current of a nominal device. Noise or variation on the V_{DD} supply also directly affects the bias current. In applications where some variation in performance is acceptable, this simple approach to biasing is ideal.

If more tightly controlled bias current is required, there are several options available. When supply voltage imprecision is a concern, adding a voltage reference diode, such as the ADR5041 to develop the gate voltages, removes bias current dependence on the supply rail. If process variation is a concern, there is a simple and low cost analog circuit employing matched PNP devices that can be used to compensate for the vast majority of process variation in the ADCA5192. This circuit is referred to as active biasing. A schematic for such a circuit is provided in Figure 38. The values of the three resistors (R1, R7, and R15) surrounding the dual PNP (Q1) vary depending on the supply voltage and target current. Values for some typical bias targets are supplied in Table 11, and the same approach can be used for any bias current target. If the target application already has a digital-to-analog converter (DAC) available with an extra output, driving the voltage at Pin 1 of E1 in Table 12, and monitoring I_{DD}, allows the user to precisely servo the targeted I_{DD} level with no additional components.

In both the passive and active biasing approaches for downstream applications, once a bias current is set, optimize performance by setting the voltage at the RSET pin (Pin 13) to match that target bias current. This voltage can be pulled down by selecting the R8 value as shown in Table 10. In the upstream application, this voltage is pulled up and is already appropriately set for all currents without adjustment in the recommended application circuit.

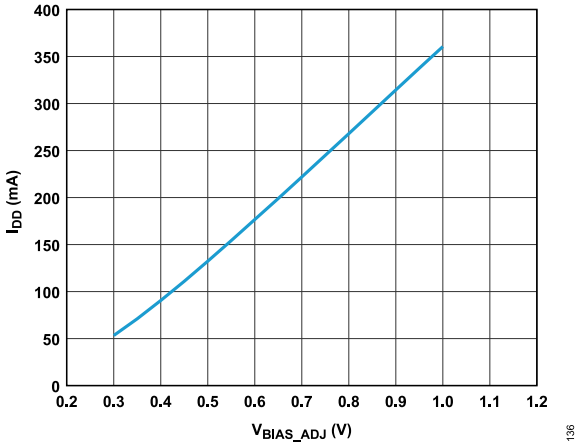

Figure 36. I_{DD} vs. V_{BIAS_ADJ}

Table 10. Suggested Values for R8 vs. I_{DD} in Downstream Application

I_{DD} (mA)	R8 Downstream Pull-Down (Ω)
100	0
125	0
150	27.4
180	121
200	174
220	274
250	442
300	768

Table 11. Suggested Values for R1, R7, and R15 vs. I_{DD} Target

I_{DD} (mA)	R1 (Ω)	R7	R15 (kΩ)
100	499	619 Ω	25.5
200	499	1 kΩ	16.2
250	499	1.87 kΩ	14

APPLICATIONS INFORMATION

DOWNSTREAM APPLICATION CIRCUIT WITH PASSIVE BIASING

The schematic in Figure 37 is recommended for downstream cable system applications from 45 MHz to 1794 MHz that employ passive biasing. Recommended values for all components are in the BOM listed in Downstream Application Circuit with Passive Biasing Bill of Materials. T1 is an RF transformer configured to transform the single-ended 75 Ω RF input to a differential signal that drives the 37.5 Ω inputs of the ADCA5192 (RFIN and RFIP). The voltage at Pin 1 of E2 is the filtered supply voltage, V_{DD}. A resistor divider (R3 and R4) sets V_{BIAS_ADJ}. See the Supply Voltage and Bias Current section for more information about how to set this voltage to adjust I_{DD}. C6 filters the gate bias and serves as the AC ground for the RF input signal. The C29 capacitor between the FBN pins (Pin 8 and Pin 10) provides feedback for the negative side of the amplifier, and the C30 capacitor between the FBP pins (Pin 16 and Pin 18) provides feedback for the positive side of the amplifier.

T2 is an RF transformer configured to transform the differential 37.5 Ω outputs (RFON and RFOP) to a single-ended 75 Ω RF output.

The C1, C2, C3, C5, C7, C8, C13, C14, C19, C20, C21, C22, L8, L9, L10, L11, R2, and R13 components are intended for impedance matching, and these components must be optimized to match the RF input source and RF output load. C4 blocks the DC voltage of the RF input source. C27 and C28 block the DC voltage at the RFOP (Pin 14) and RFON (Pin 12) output pins. The L2 and L3 inductors are RF chokes connected to the filtered V_{DD} supply voltage.

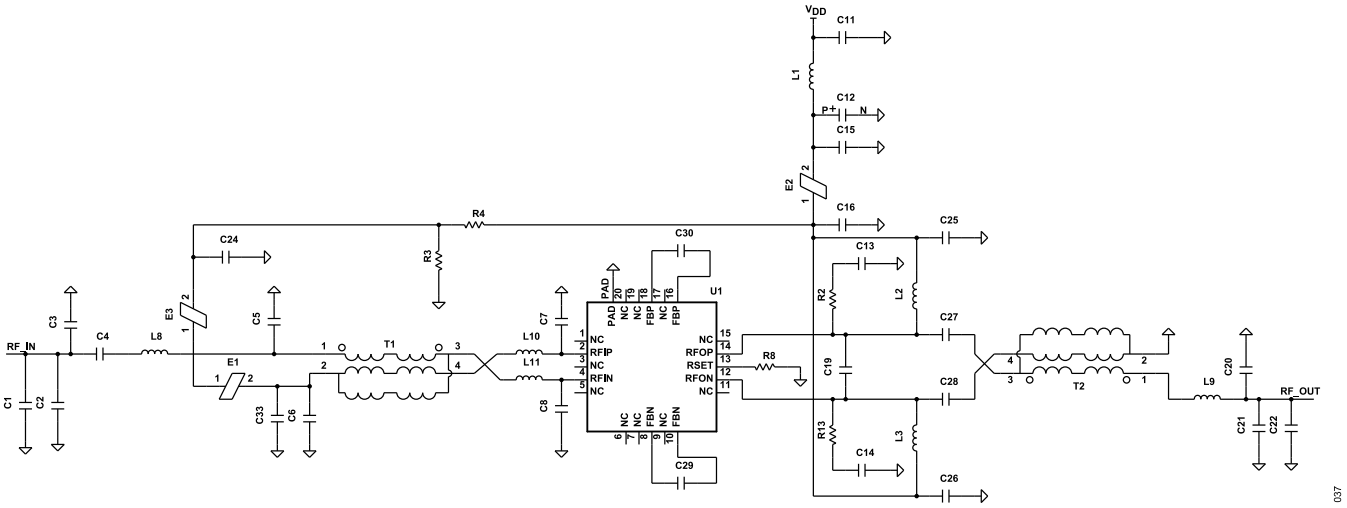

Figure 37. Downstream Application Circuit with Passive Biasing Schematic

APPLICATIONS INFORMATION

DOWNSTREAM APPLICATION CIRCUIT WITH PASSIVE BIASING BILL OF MATERIALS

Table 12. Downstream Bill of Materials with Passive Biasing[1]

Reference Designator	Value	Tolerance	Minimum Rating	Footprint	Suggested Vendor	Suggested Part Number
C4, C6, C16	0.01 µF	±10%	50 V	0402	Samsung	CL05B103KB5NNNC
C7, C8	1.1 pF	±0.1 pF	25 V	0201	Johanson	250R05L1R1BV4T
C11	0.01 µF	±10%	100 V	0603	TDK	C1608X7R2A103K080AA
C12	2.2 µF	±10%	50 V	1411	Kyocera	TAJB225K050RNJ
C15	0.047 µF	±5%	25 V	0603	Kyocera	06033C473JAT2A
C19	0.3 pF	±0.1 pF	50 V	0402	Murata	GJM1555C1HR30BB01D
C25, C26	0.01 µF	±10%	50 V	0402	Murata	GCM155R71H103KA55D
C27, C28	220 pF	±5%	50 V	0402	Murata	GCM1555C1H221JA16D
C29, C30	330 pF	±10%	25 V	0201	Murata	GRM033R71E331KA01D
E1, E3	1 kΩ ferrite	±25%	N/A	0201	Taiyo Yuden	BKH0603LM102-T
E2	220 Ω ferrite	±25%	N/A	0603	Taiyo Yuden	FBMH1608HM221-T
L1	2.2 µH	±20%	N/A	1210	Taiyo Yuden	BRL3225T2R2M
L2, L3	270 nH	±5%	N/A	0402	Coilcraft	0402DF-271XJRW
L8	1 nH	±0.1 nH	N/A	0402	Murata	LQG15HH1N0B02D
L9	2.2 nH	±0.2 nH	N/A	0402	Murata	LQW15AN2N2C10D
L10, L11	2.7 nH	±0.2 nH	N/A	0402	Murata	LQW15AN2N7C00D
R3	1 kΩ	±1%	100 mW	0402	Panasonic	ERJ-2RKF1001X
R4	4.12 kΩ	±1%	100 mW	0402	Panasonic	ERJ-2RKF4121X
R8	Select[2]	1%	50 mW	0201	N/A	N/A
T1, T2	TRS1-182-75-3+	N/A	N/A	TT1618-2	Mini-Circuits	TRS1-182-75-3+
U1	ADCA5192	N/A	N/A	4 mm × 4 mm, 20-lead LFSCP	Analog Devices, Inc.	ADCA5192
C5, C13, C14, R2, R13	Do not install (DNI)	N/A	N/A	0201	N/A	N/A
C1, C2, C3, C20, C21, C22	DNI	N/A	N/A	0402	N/A	N/A

[1] N/A means not applicable.

[2] See Table 10 for suggested values.

APPLICATIONS INFORMATION

DOWNSTREAM APPLICATION CIRCUIT WITH ACTIVE BIASING

The schematic in Figure 38 is recommended for downstream cable system applications from 45 MHz to 1794 MHz that employ active biasing. Recommended values for all components are in Table 13. The voltage at Pin 1 of E2 is the filtered supply voltage, V_{DD}. T1 is an RF transformer configured to transform the single-ended 75 Ω RF input to a differential signal that drives the 37.5 Ω inputs of the ADCA5192 (RFIN and RFIP). The active bias circuit comprises the C9, C31, C32, R1, R7, R11, R12, R15, Q1 components. The circuit is connected to Pin 1 of E1. See the Supply Voltage and Bias Current section for more information about how to control I_{DD} using this circuit. C6 stabilizes the output of the active bias circuit and serves as the AC ground for the RF input signal. The C29 capacitor between the FBN pins (Pin 8 and Pin 10) provides feedback for the negative side of the amplifier, and the C30 capacitor between the FBP pins (Pin 16 and Pin 18) provides feedback for the positive side of the amplifier.

T2 is an RF transformer configured to transform the differential 37.5 Ω outputs (RFON and RFOP) to a single-ended 75 Ω RF output.

The C1, C2, C3, C5, C7, C8, C13, C14, C19, C20, C21, C22, L8, L9, L10, L11, R2, and R13 components are intended for impedance matching, and these components must be optimized to match the RF input source and RF output load. C4 blocks the DC voltage of the RF input source. C27 and C28 block the DC voltage at the RFOP (Pin 14) and RFON (Pin 12) output pins. The L2 and L3 inductors are RF chokes connected to the filtered V_{DD} supply voltage.

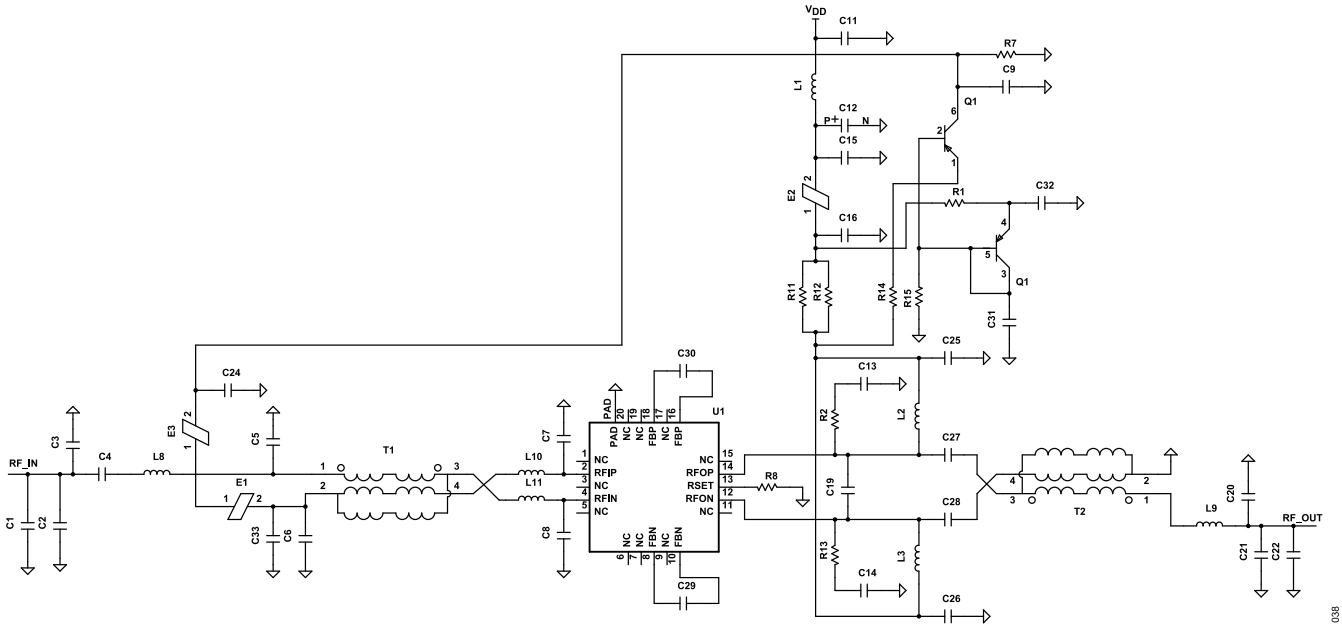

Figure 38. Downstream Application Circuit with Active Biasing Schematic

APPLICATIONS INFORMATION

DOWNSTREAM APPLICATION CIRCUIT WITH ACTIVE BIASING BILL OF MATERIALS

Table 13. Downstream Bill of Materials with Active Biasing[1]

Reference Designator	Value	Tolerance	Minimum Rating	Footprint	Suggested Vendor	Suggested Part Number
C4, C6, C9, C16, C31, C32	0.01 µF	±10%	50 V	0402	Samsung	CL05B103KB5NNNC
C7, C8	1.1 pF	±0.1 pF	25 V	0201	Johanson	250R05L1R1BV4T
C11	0.01 µF	±10%	100 V	0603	TDK	C1608X7R2A103K080AA
C12	2.2 µF	±10%	50 V	1411	Kyocera	TAJB225K050RNJ
C15	0.047 µF	±5%	25 V	0603	Kyocera	06033C473JAT2A
C19	0.3 pF	±0.1 pF	50 V	0402	Murata	GJM1555C1HR30BB01D
C25, C26	0.01 µF	±10%	50 V	0402	Murata	GCM155R71H103KA55D
C27, C28	220 pF	±5%	50 V	0402	Murata	GCM1555C1H221JA16D
C29, C30	330 pF	±10%	25 V	0201	Murata	GRM033R71E331KA01D
E1, E3	1 kΩ ferrite	±25%	N/A	0201	Taiyo Yuden	BKH0603LM102-T
E2	220 Ω ferrite	±25%	N/A	0603	Taiyo Yuden	FBMH1608HM221-T
L1	2.2 µH	±20%	N/A	1210	Taiyo Yuden	BRL3225T2R2M
L2, L3	270 nH	±5%	N/A	0402	Coilcraft	0402DF-271XJRW
L8	1 nH	±0.1 nH	N/A	0402	Murata	LQG15HH1N0B02D
L9	2.2 nH	±0.2 nH	N/A	0402	Murata	LQW15AN2N2C10D
L10, L11	2.7 nH	±0.2 nH	N/A	0402	Murata	LQW15AN2N7C00D
Q1	BCM857BV	N/A	45 V	SOT666	Nexperia	BCM857BV,115
R1, R7, R15	Select[2]	±1%	N/A	N/A	N/A	N/A
R8	Select[3]	1%	50 mW	0201	N/A	N/A
R11, R12	1 Ω	±1%	N/A	0402	Panasonic	ERJ-2BQF1R0X
R14	0 Ω	N/A	N/A	0603	Panasonic	ERJ-3GEY0R00V
T1, T2	TRS1-182-75-3+	N/A	N/A	TT1618-2	Mini-Circuits	TRS1-182-75-3+
U1	ADCA5192	N/A	N/A	4 mm × 4 mm, 20-lead LFSCP	Analog Devices	ADCA5192
C5, C13, C14, R2, R13	DNI	N/A	N/A	0201	N/A	N/A
C1, C2, C3, C20, C21, C22	DNI	N/A	N/A	0402	N/A	N/A

[1] N/A means not applicable.

[2] See Table 11 for suggested values.

[3] See Table 10 for suggested values.

APPLICATIONS INFORMATION

UPSTREAM APPLICATION CIRCUIT

The schematic in Figure 39 is recommended for upstream cable system applications at all DOCSIS 4.0 splits that employ passive biasing. Recommended values for all components are in Table 14. X1 is an RF transformer configured to transform the single-ended 75 Ω RF input to a differential signal that drives the 37.5 Ω inputs of the ADCA5192 (RFIN and RFIP). The voltage at Pin 2 of E2 is the filtered supply voltage, V_{DD}. A resistor divider (R3 and R4) sets V_{BIAS_ADJ}. See the Supply Voltage and Bias Current section for more information about how to set this voltage to adjust I_{DD}. C6 stabilizes this reference and serves as the AC ground for the RF input signal. The C30 capacitor between the FBN pins (Pin 8 and Pin 10) provides feedback for the negative side of the amplifier, and the C29 capacitor between the FBP pins (Pin 16 and Pin 18) provides feedback for the positive side of the amplifier.

X2 is an RF transformer configured to transform the differential 37.5 Ω outputs (RFON and RFOP) to a single-ended 75 Ω RF output.

The C1, C2, C3, C5, C7, C8, C20, C21, C22, L10, and L11 components are intended for impedance matching, and these components must be optimized to match the RF input source and RF output load. C4 blocks the DC voltage of the RF input source. C23 blocks the DC voltage at the RF output. The output balun serves to DC connect to the filtered V_{DD} supply voltage.

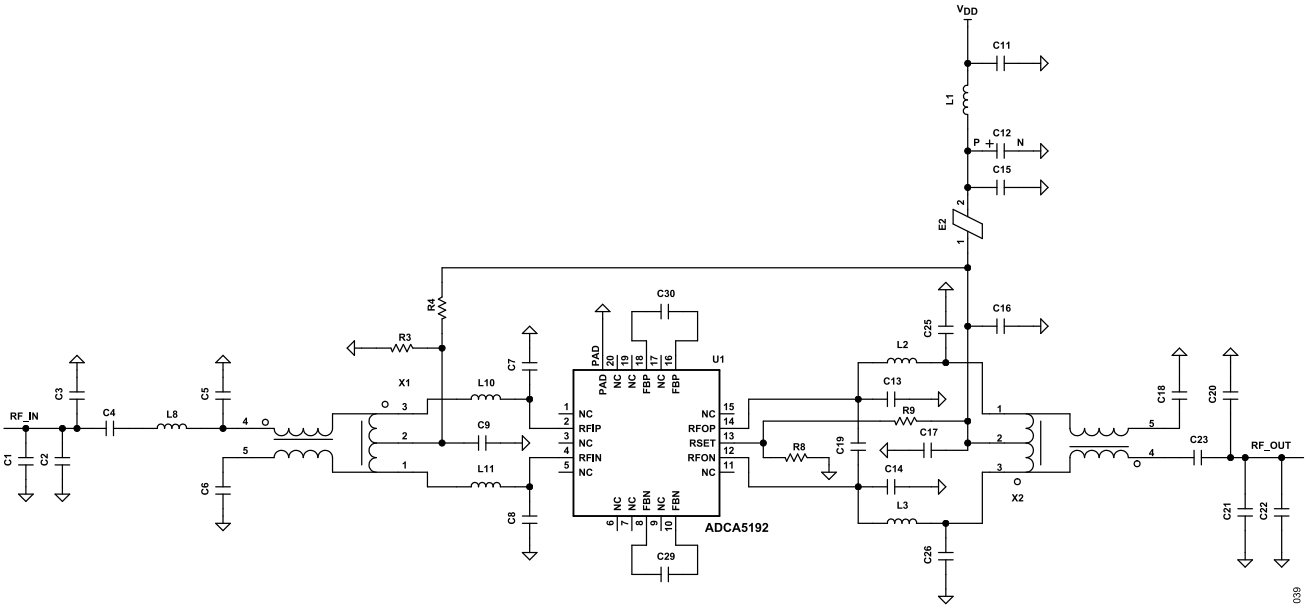

Figure 39. Upstream Application Circuit with Passive Biasing Schematic

APPLICATIONS INFORMATION

UPSTREAM APPLICATION CIRCUIT BILL OF MATERIALS

Table 14. Upstream Bill of Materials[1]

Reference Designator	Value	Tolerance	Minimum Rating	Footprint	Suggested Vendor	Suggested Part Number
C4, C6, C16, C18, C23	0.1 µF	±10%	50 V	0402	Kyocera	KGM05CR71H104KH
C7, C8	1.6 pF	±0.1 pF	50 V	0201	Murata	GRM0335C1H1R6BA01D
C9, C17, C29, C30	0.1 µF	±10%	25 V	0201	Kyocera	02013D104KAT2A
C11	0.1 µF	±10%	25 V	0603	Kyocera	KGM15BR71E104KT
C12	2.2 µF	±10%	50 V	1411	Kyocera	TAJB225K050RNJ
C13, C14	4 pF	±0.05 pF	50 V	0201	Murata	GRM0335C1H4R0WA01D
C15	0.047 µF	±5%	25 V	0603	Kyocera	06033C473JAT2A
C20	0.4 pF	±0.1pF	100 V	0402	Murata	GRM1555C2AR40BA01D
C25, C26	3.3 pF	±0.1pF	50 V	0402	Murata	GRM1555C1H3R3BA01D
E2	220 Ω ferrite	±25%	N/A	0603	Taiyo Yuden	FBMH1608HM221-T
L1	2.2 µH	±20%	N/A	1210	Taiyo Yuden	BRL3225T2R2M
L2, L3	9.5 nH	±2%	1.4 A	0402	Murata	LQW15AN9N5G80D
L10, L11	3.6 nH	±0.1 nH	1.95 A	0402	Murata	LQW15AN3N6G8ZD
L8	0 Ω	N/A	N/A	0402	Panasonic	ERJ-2GE0R00X
R3	499 Ω	±1%	100 mW	0402	Panasonic	ERJ-2RKF4990X
R9	499 Ω	±1%	50 mW	0201	Panasonic	ERJ-1GNF4990C
U1	ADCA5192	N/A	N/A	4 mm × 4 mm, 20-lead LFSCP	Analog Devices, Inc.	ADCA5192
X1, X2	MRFXF5R17	N/A	N/A	S20	MiniRF	MRFXF5R17
R4	9.1 kΩ	±1%	100 mW	0402	Panasonic	ERJ-2RKF9101X
C1, C2, C3, C19, C21, C22, R8	DNI	N/A	N/A	0402	N/A	N/A
C5	DNI	N/A	N/A	0201	N/A	N/A

[1] N/A means not applicable.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS

The recommended layout for the ADCA5192 is demonstrated by the evaluation circuit shown in the EVAL-ADCA5192 evaluation board user guide (UG-2191). The evaluation circuit includes both passive and active biasing approaches, while a final application will likely only have one of these. Components can be removed from that layout per the schematic recommendations. When deviating from this recommended layout, keep the following points in mind:

- All RF components must be kept as close as possible to the ADCA5192. These components include the transformers and all tuning components in series or shunt to the RF traces.
- Differential symmetry must be strictly maintained between the input and output balun.
- C29 and C30, the feedback capacitors, must be kept as close as possible to the ADCA5192 and must be referenced to the RF ground plane.
- When using active biasing, components around Q1 must be kept physically close to Q1.
- Place E1 and E3 ferrite beads on either side of the pass-through under the balun if laying out on the same layer as RF. If this line is on an isolated layer, only one of the two ferrite beads is necessary.

OUTLINE DIMENSIONS

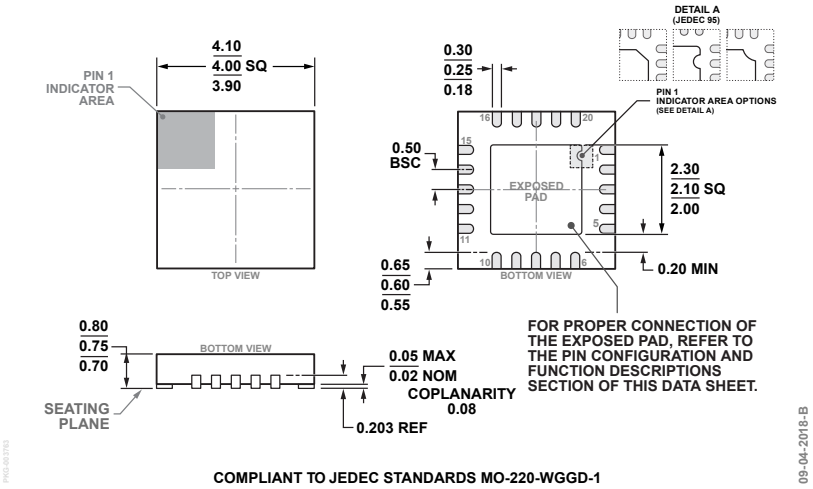

Figure 40. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADCA5192ACPZ	−40°C to +100°C	20-Lead LFCSP (4 mm × 4 mm with EPAD)		CP-20-6
ADCA5192ACPZ-REEL7	−40°C to +100°C	20-Lead LFCSP (4 mm × 4 mm with EPAD)	Reel, 1500	CP-20-6

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADCA5192-EVALZ	Evaluation Board for the Downstream Cable System Application

[1] Z = RoHS Compliant Part.