



# PSMN3R2-40YLB

N-channel 40 V, 3.3 mOhm, 120 A logic level MOSFET in LFAK56 using optimized NextPowerS3 Schottky-Plus technology

13 February 2024

Product data sheet

## 1. General description

120 A, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LFAK56 package, using advanced TrenchMOS Superjunction technology with optimization to provide improved EMC performance (up to 6 dB). This product has been designed and qualified for high performance power switching applications.

## 2. Features and benefits

- Optimized for improved EMC Performance
- 120 A continuous  $I_{D(max)}$  rating
- Avalanche rated, 100% tested at  $I_{AS} = 120$  A
- Strong SOA (linear-mode) rating
- NextPowerS3 technology delivers 'superfast switching with soft body-diode recovery'
- Low  $Q_{rr}$ ,  $Q_G$  and  $Q_{GD}$  for high system efficiency and low EMI designs
- Schottky-Plus body-diode with low  $V_{SD}$ , low  $Q_{rr}$ , soft recovery and low  $I_{DSS}$  leakage
- Optimized for 4.5 V gate drive utilizing NextPowerS3 Superjunction technology
- High reliability LFAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints providing excellent board level reliability
- Low parasitic inductance and resistance

## 3. Applications

- Automation, control and instrumentation
- Autonomous systems, Robotics and Cobots
- DC-to-DC converters
- Brushless DC motor control
- Brushed motors
- Battery isolation
- Industrial load-switch and eFuse
- Inrush management, hotswap

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	-	120	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	-	115	W
$T_j$	junction temperature			-55	-	175	°C

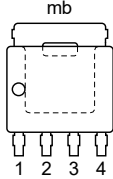
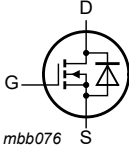
N-channel 40 V, 3.3 mOhm, 120 A logic level MOSFET in LPAK56 using optimized NextPowerS3 Schottky-Plus technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	2.9	3.3	mΩ
		$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	3.6	4.2	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	1.3	4.2	8.4	nC
$Q_{G(tot)}$	total gate charge		12	19	27	nC

[1] 120 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R2-40YLB	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R2-40YLB	3B2L40Y

## 8. Limiting values

Table 5. Limiting values

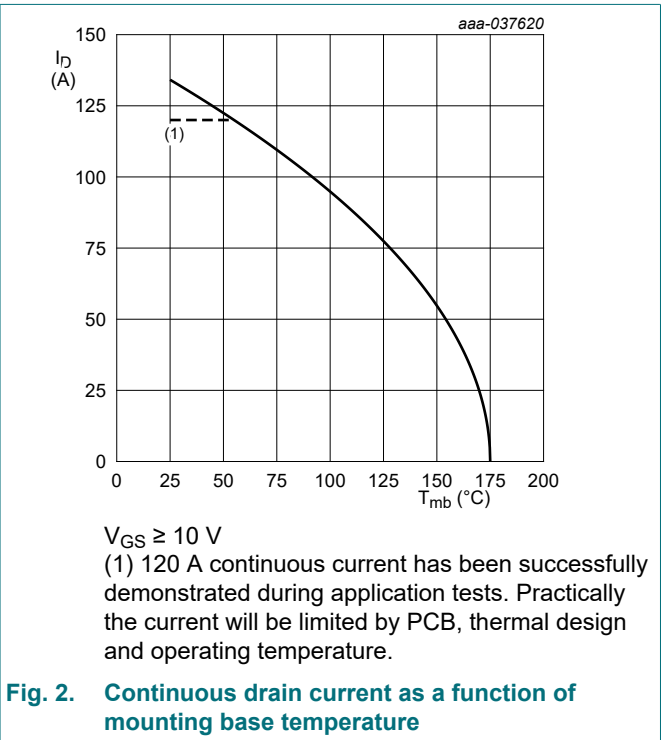
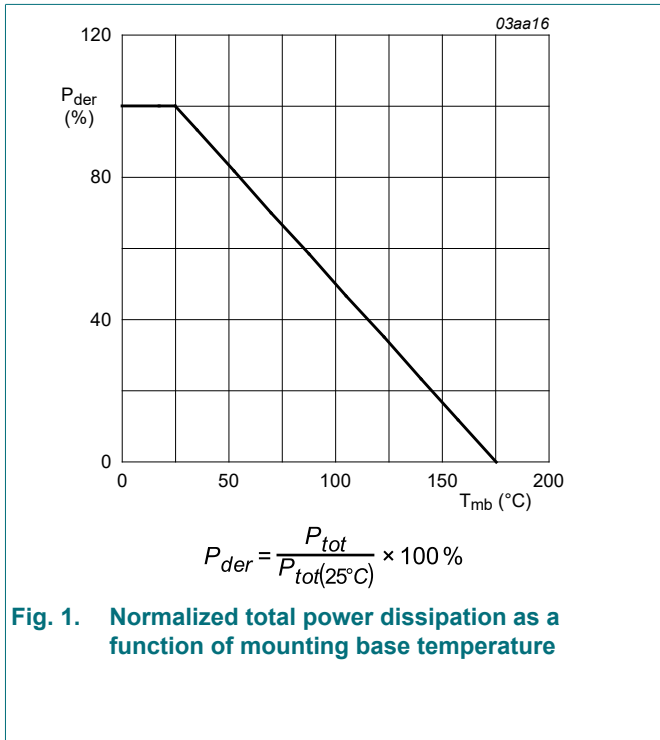
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ }^\circ\text{C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	40	V
$V_{DSM}$	peak drain-source voltage	$t_p \leq 20\text{ ns}$ ; $f = 500\text{ kHz}$ ; $E_{DS(AL)} \leq 200\text{ nJ}$ ; pulsed	-	45	V
$V_{DGR}$	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	40	V

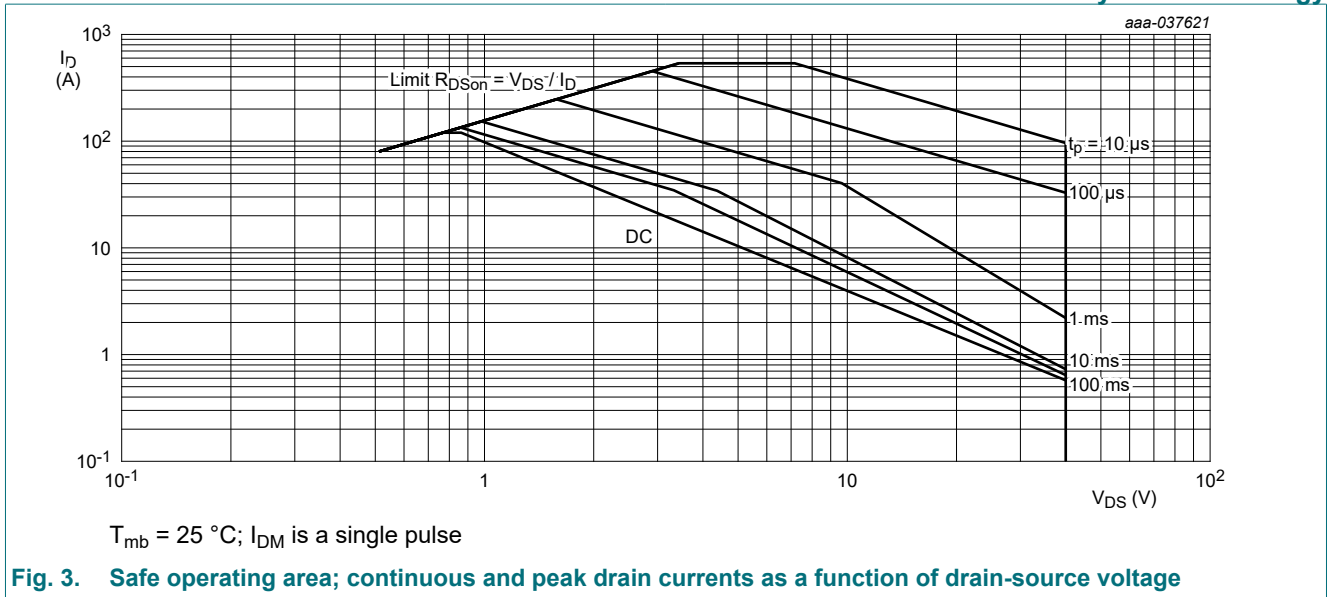
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Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>GS</sub>	gate-source voltage		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; Fig. 1	-	115	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; Fig. 2 [1]	-	120	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; Fig. 2	-	95	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; Fig. 3	-	537	A
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	115	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	537	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 39 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 146 μs [2]	-	148	mJ
		I <sub>D</sub> = 25 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 374 μs [2]	-	243	mJ
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω [2]	-	120	A

- [1] 120 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test



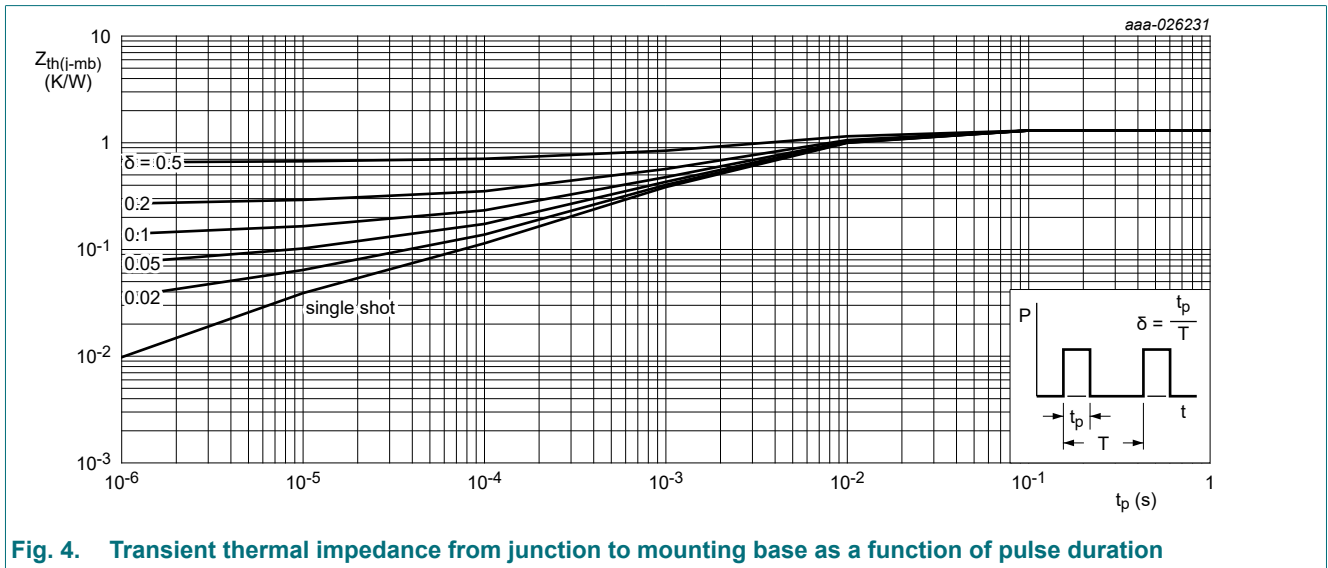
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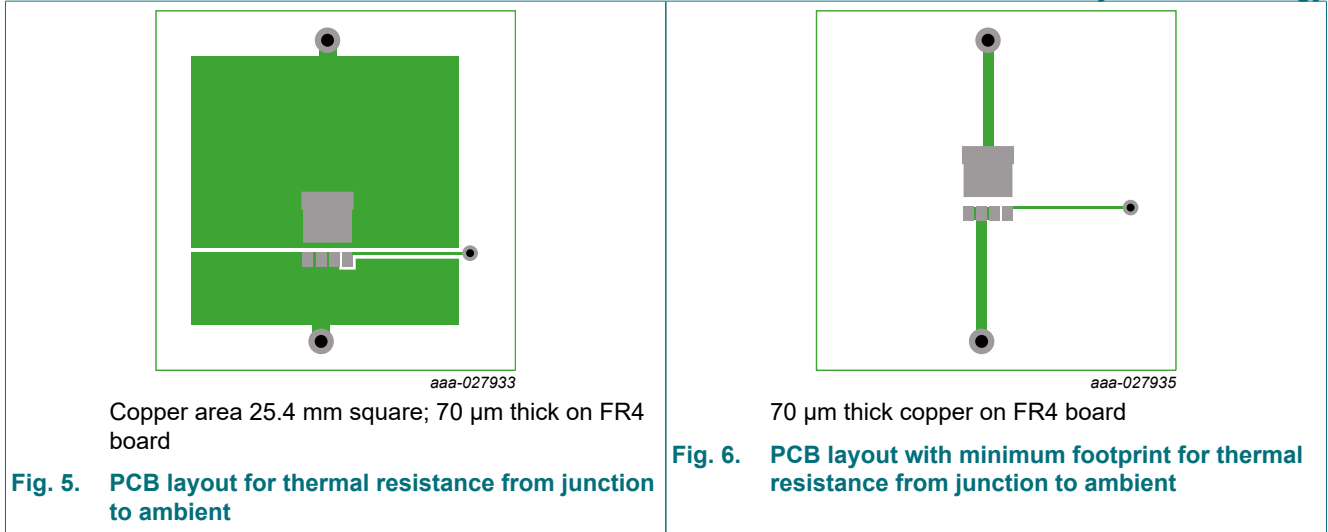
### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.18	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5 Fig. 6	-	42	-	K/W
			-	85	-	K/W



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## 10. Characteristics

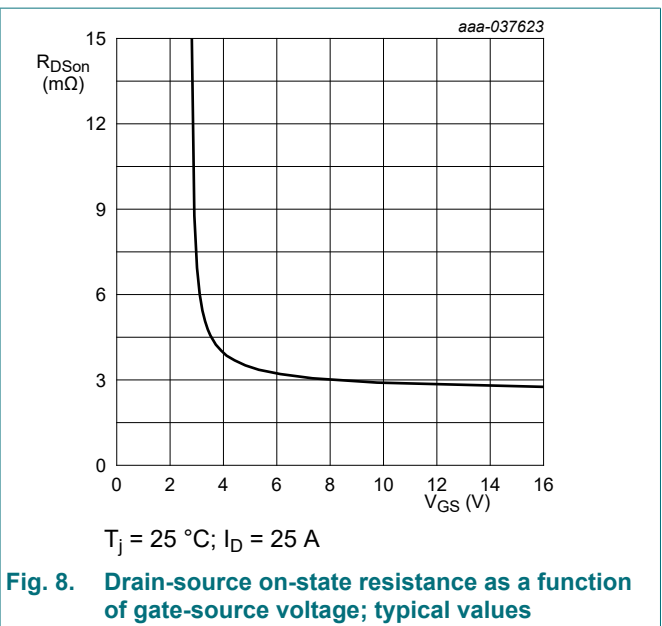
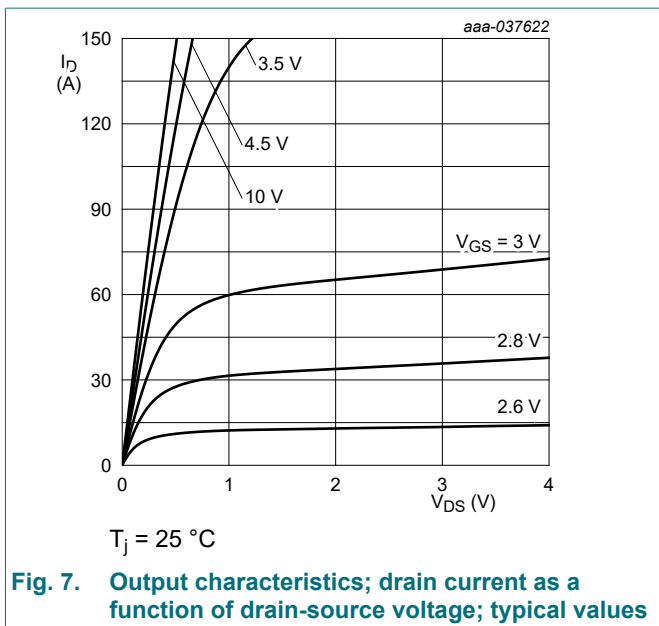
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.35	1.8	2.05	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.7	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	$\mu A$
		$V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	1	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	2.9	3.3	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	6.4	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	3.6	4.2	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	8.1	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.3	0.7	1.8	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	12	19	27	nC
		$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	27	42	59	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C$	-	40	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 20\text{ V}; V_{GS} = 4.5\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	4.6	7.7	12	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		2.7	4.5	6.8	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		1.8	3	4.5	nC
$Q_{GD}$	gate-drain charge		1.3	4.2	8.4	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	2.8	-	V
$C_{iss}$	input capacitance	$V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 14</a>	1955	3008	4211	pF
$C_{oss}$	output capacitance		644	991	1387	pF
$C_{riss}$	reverse transfer capacitance		30	99	218	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}; R_L = 0.8\text{ }\Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	17	-	ns
$t_r$	rise time		-	21	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
$t_f$	fall time		-	12	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$	-	29	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	0.8	1	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	24	-	ns
$Q_r$	recovered charge		[1]	14	-	nC
$t_a$	reverse recovery rise time		-	12	-	ns
$t_b$	reverse recovery fall time		-	12	-	ns

[1] includes capacitive recovery



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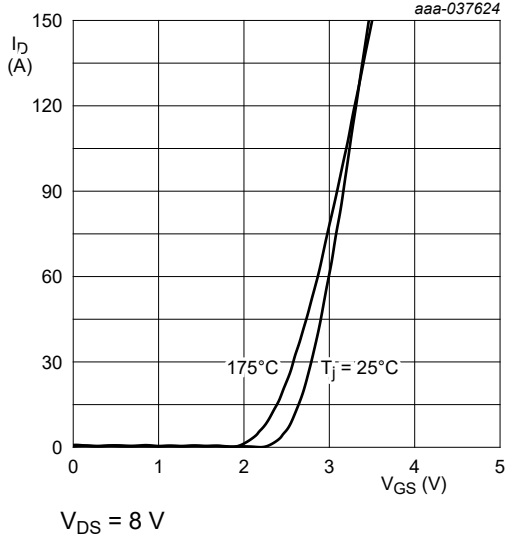


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

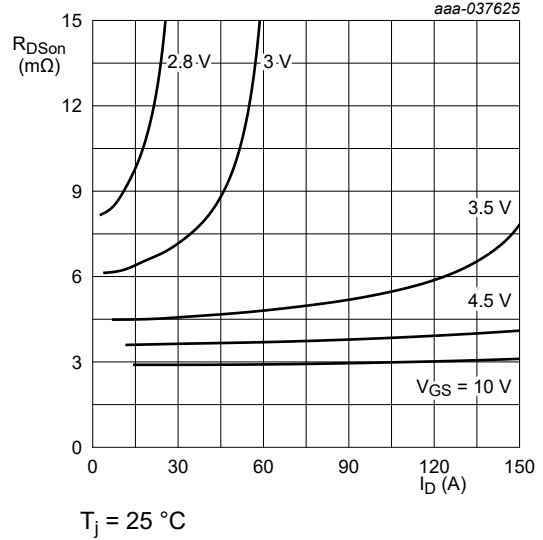


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

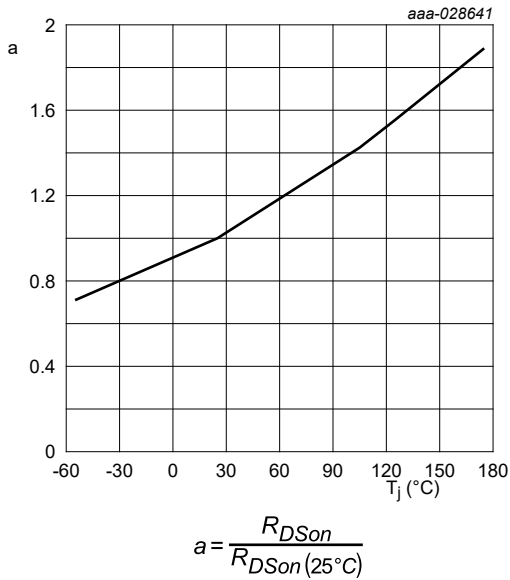


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

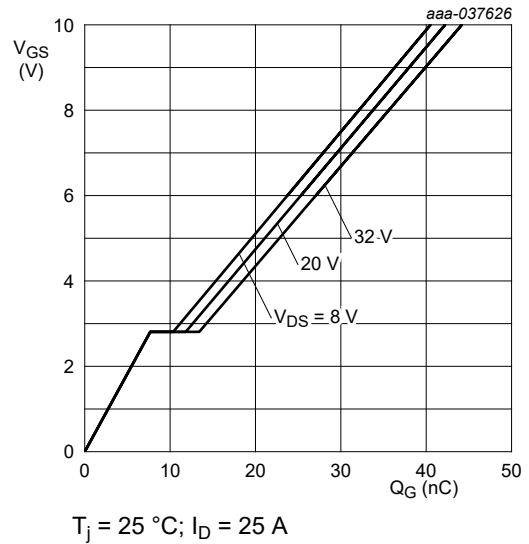


Fig. 12. Gate-source voltage as a function of gate charge; typical values

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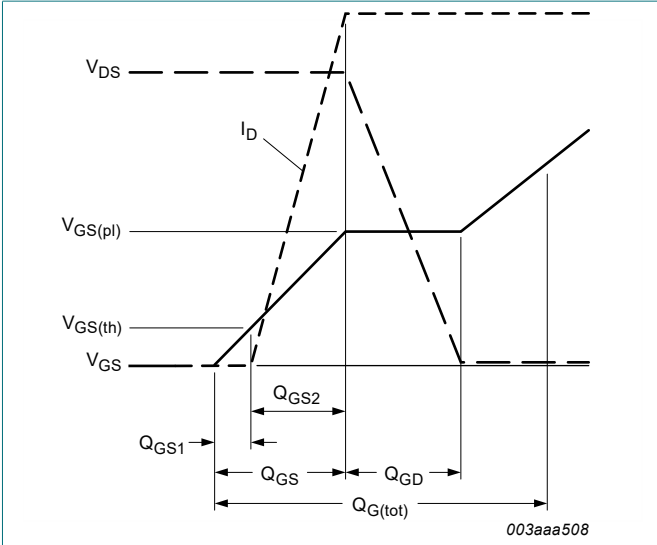


Fig. 13. Gate charge waveform definitions

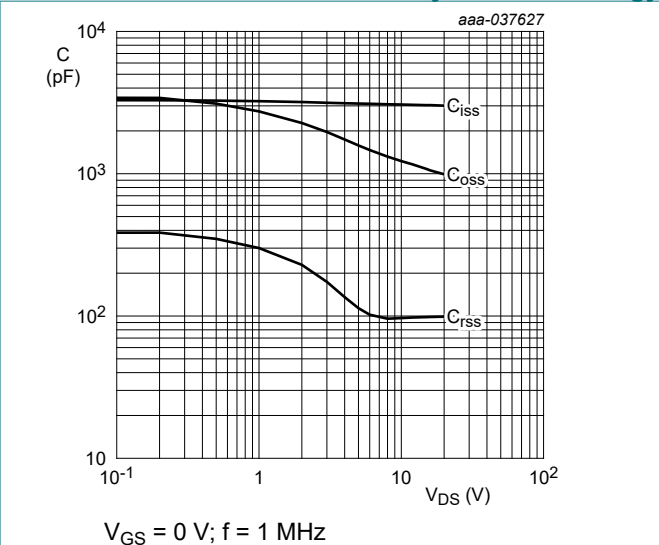


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

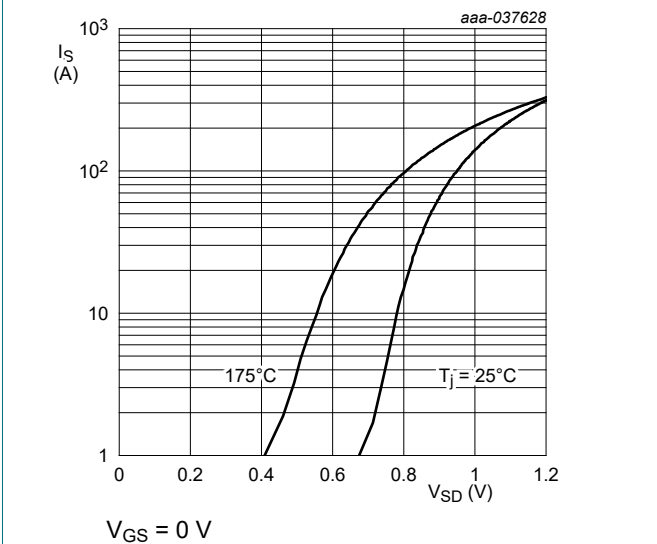


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

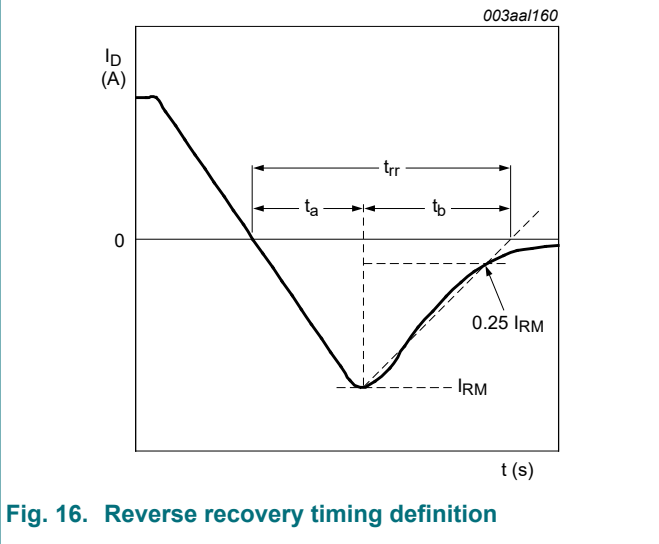


Fig. 16. Reverse recovery timing definition



11. Package outline

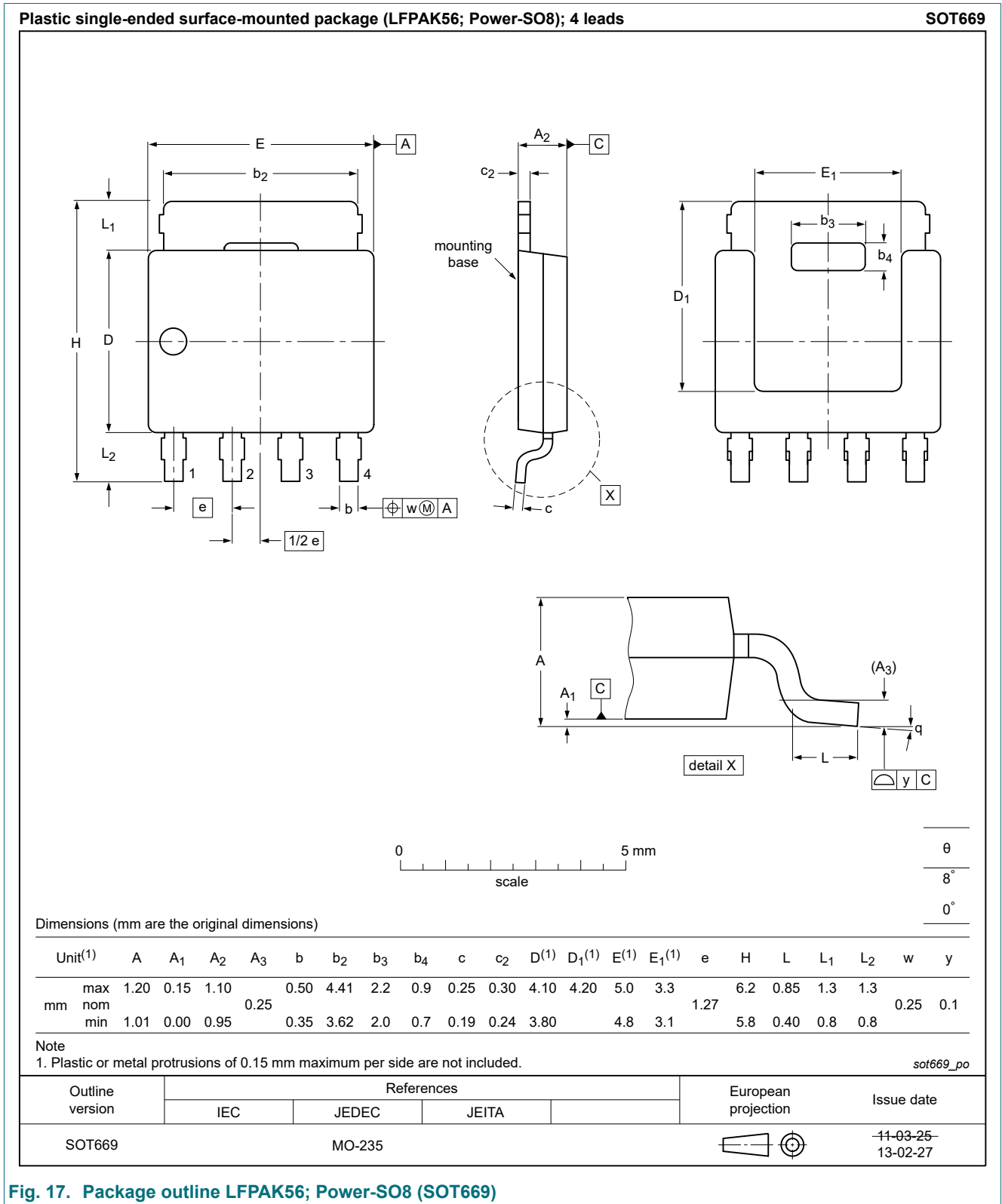


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Soldering

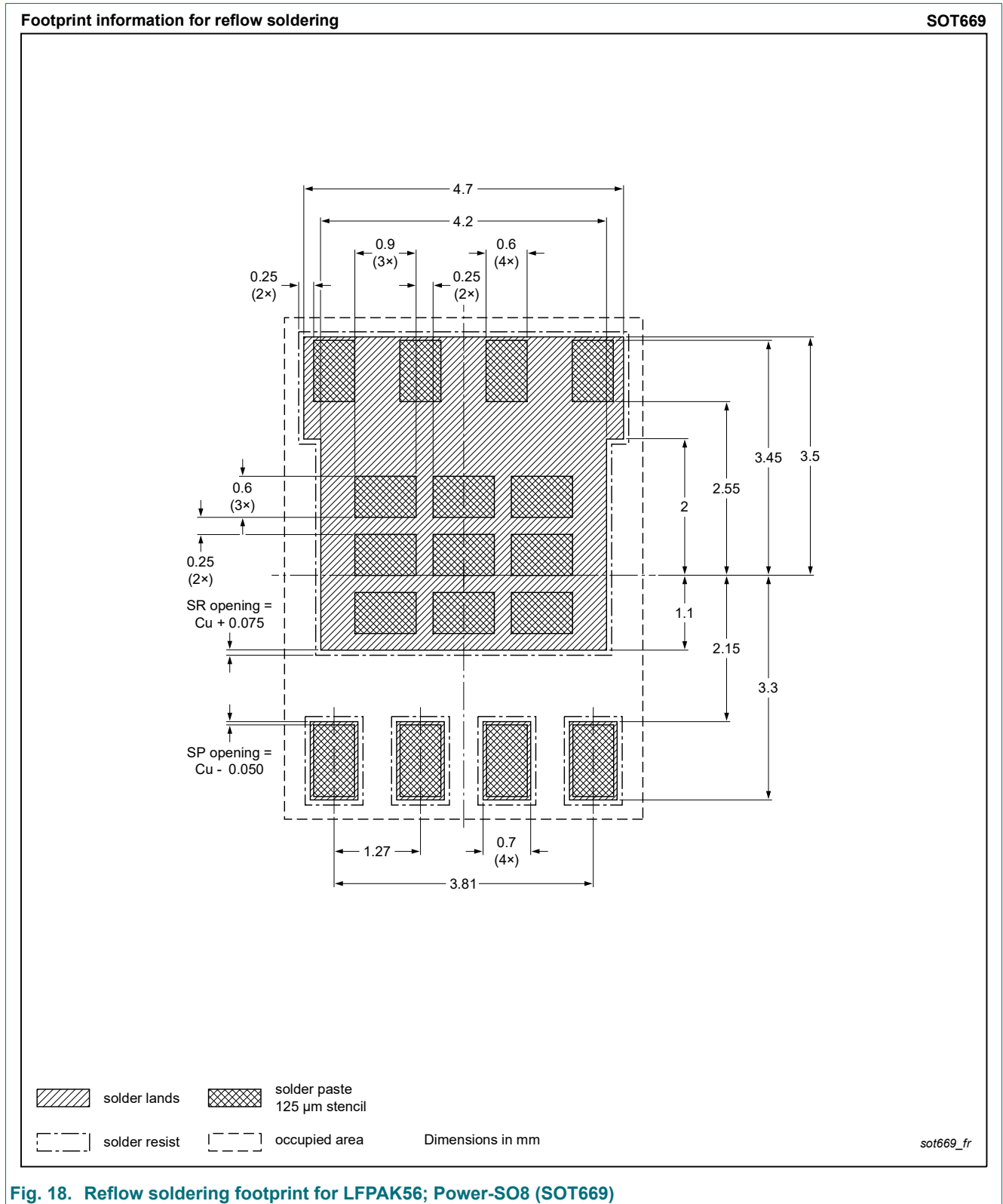
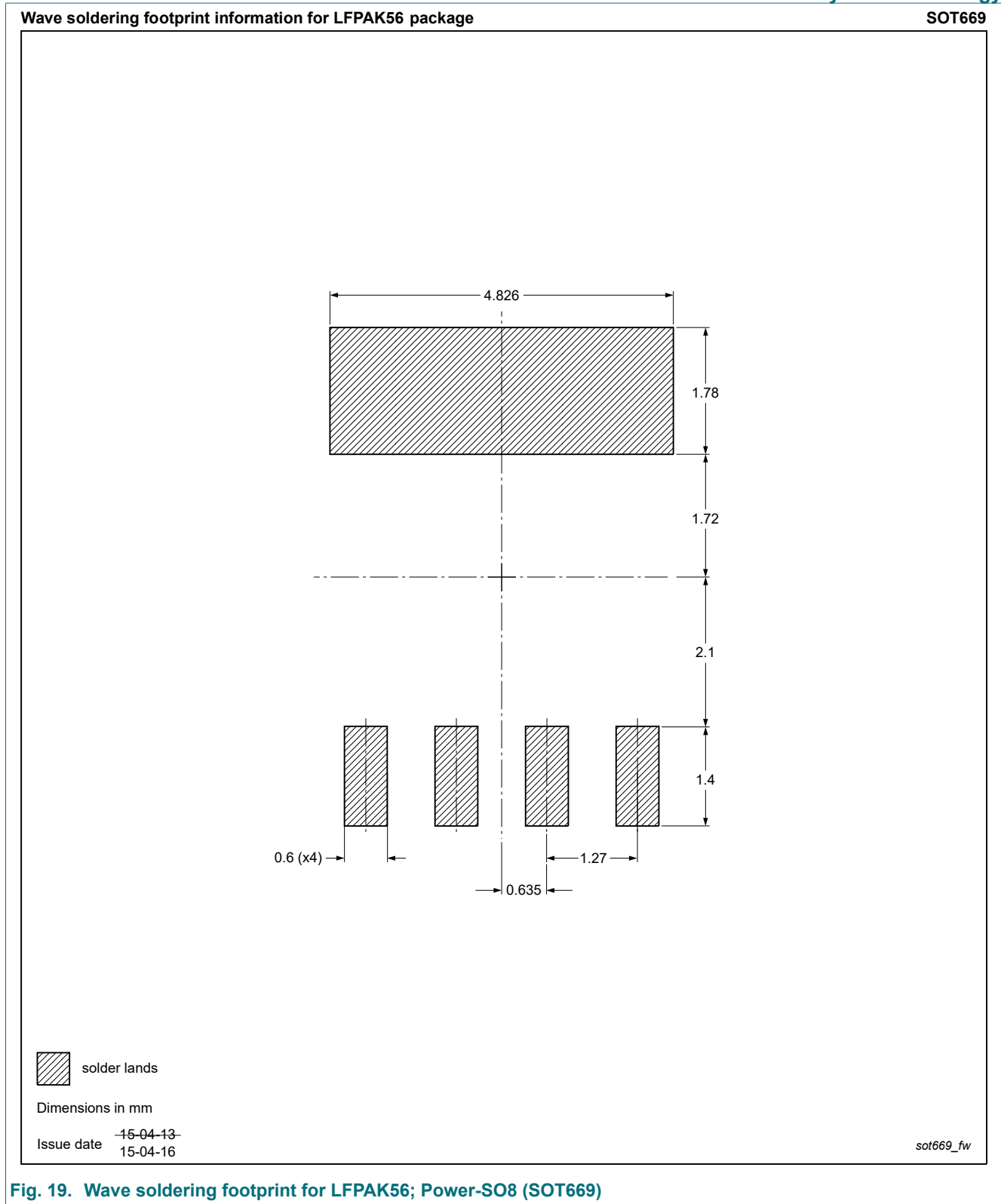


Fig. 18. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)



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### 13. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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