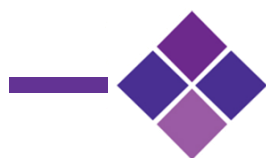




WORM microSD Specification



Version 1.5

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TABLE OF CONTENTS

1. GENERAL DESCRIPTION	1
1.1 Introduction	1
1.2 Product Overview	1
2. PRODUCT SPECIFICATIONS	2
2.1 Performance.....	2
2.2 Power.....	2
2.3 MTBF	2
3. ENVIRONMENTAL SPECIFICATIONS.....	3
4. ELECTRICAL SPECIFICATIONS	4
4.1 DC Characteristics.....	4
4.1.1 Bus Operation Conditions for 3.3V Signaling.....	4
4.1.2 Bus Signal Line Load	5
4.2 AC Characteristic	6
4.2.1 microSD Interface timing (Default)	6
4.2.2 microSD Interface Timing (High-Speed Mode).....	7
4.2.3 microSD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes).....	9
4.2.4 microSD Interface timing (DDR50 Modes)	11
5. PAD ASSIGNMENT	12
6. REGISTERS.....	12
7. PHYSICAL DIMENSION	12
8. ORDERING INFORMATION.....	12

1. GENERAL DESCRIPTION

1.1 Introduction

Write Once Read Many (WORM) microSD card is designed for special application such as Financial Industry Regulatory Authority, Exchange Commission for records protection.

Write Once Read Many (WORM) microSD card is WORM mode by default. The WORM microSD card will change to write protect mode if the user performs illegal action such as delete file/directory, rename file/directory, change existed data, overwrite file data and disk format. This can prevent the data be erased, modified or overridden.

1.2 Product Overview

◆ Flash MLC	◆ Support SD System Specification 6.1
◆ Capacity 4GB to 128GB	◆ Support SD SPI Mode
◆ Card Mode WORM Mode by default	◆ Support FAT32
◆ Support Auto Read Refreshment	◆ File is written one by one sequentially
◆ Read disturbance management	◆ SMART function support
◆ Adaptive wear leveling	◆ Support management of sudden power fails
◆ Do not support Erase/Lock/ Unlock SD Commands	◆ Temperature Range Operation (Gold): -25°C ~ 85°C Operation (Diamond): -40°C ~ 85°C Storage: -40°C ~ 85°C

2. PRODUCT SPECIFICATIONS

2.1 Performance

Capacity	Sequential	
	Read (MB/s)	Write (MB/s)
4GB	72	25
8GB	72	25
16GB	75	45
32GB	75	68
64GB	75	68
128GB	78	69

Table 2-1 Performance of WORM microSD

NOTES:

1. The performance is obtained from TestMetrix
2. Performance may vary from flash configuration and platform.

2.2 Power

Capacity	Read (mA)	Write (mA)	Standby (mA)
4GB	169	89	198
8GB	169	89	198
16GB	169	89	198
32GB	169	89	198
64GB	169	89	198
128GB	169	89	198

Table 2-2 Typical Power Consumption of WORM microSD

2.3 MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The higher the MTBF value, the higher the reliability of the device. The predicted result of WORM microSD Card is more than 3,000,000 hours.

3. ENVIRONMENTAL SPECIFICATIONS

Test Items	Test Conditions
Storage Temperature	-40°C ~ 85°C
Operating Temperature	Gold: -25°C ~ 85°C Diamond: -40°C ~ 85°C
Storage Humidity	40°C, 93% RH
Operating Humidity	25°C, 95% RH
Shock	1500G, Half Sin Pulse Duration 0.5ms
Vibration	80Hz ~ 2000Hz/20G, 20Hz ~ 80Hz/1.52mm, 3 axis/30min
Drop	150cm free fall, 6 face of each unit
Bending	≥ 10N, Hold 1 min/5 times
Torque	0.1N-m or +/-2.5 deg, Hold 30 seconds/5 times
ESD	Contact: +/- 4KV each item 25 times Air: +/- 8KV 10 times

Table 3-1 Environmental Specification

4. ELECTRICAL SPECIFICATIONS

4.1 DC Characteristics

4.1.1 Bus Operation Conditions for 3.3V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	$0.75 \cdot V_{DD}$		V	$I_{OH} = -2mA$ V_{DD} Min
Output Low Voltage	V_{OL}		$0.125 \cdot V_{DD}$	V	$I_{OL} = 2mA$ V_{DD} Min
Input High Voltage	V_{IH}	$0.625 \cdot V_{DD}$	$V_{DD} + 0.3$	V	
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	$0.25 \cdot V_{DD}$	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Table 4-1 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	$I_{OH} = -2mA$
Output Low Voltage	V_{OL}	-	0.45	V	$I_{OL} = 2mA$
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	0.58	V	

Table 4-2 Threshold Level for 1.8V Signaling

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	μA	DAT3 pull-up is disconnected.

Table 4-3 Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	$V_{DD}+0.3$	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 4-4 Peak Voltage and Leakage Current

4.1.2 Bus Signal Line Load

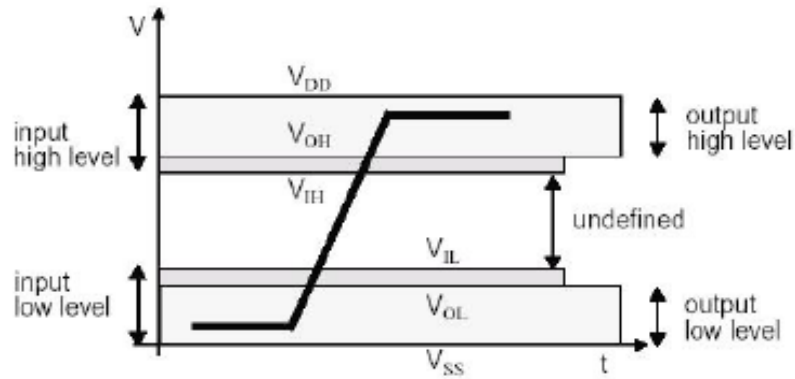
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = $C_{HOST} + C_{BUS} + N C_{CARD}$

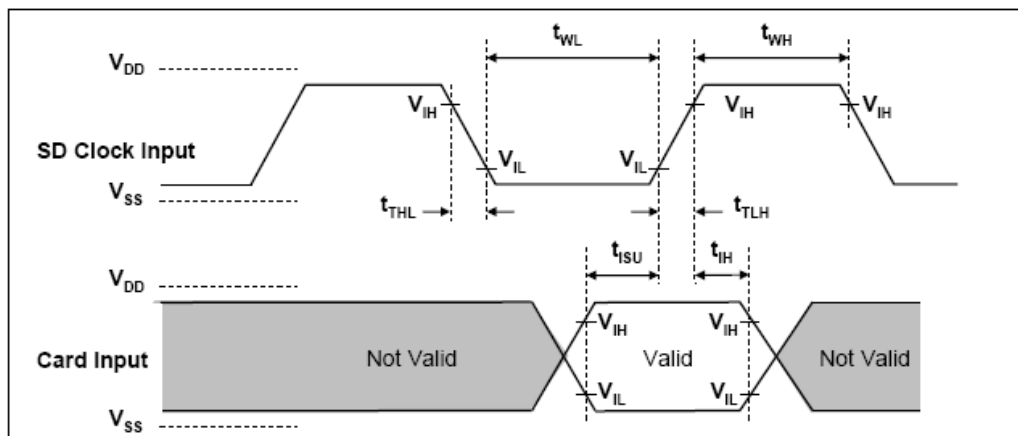
Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	k Ω	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card $C_{HOST}+C_{BUS}$ shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10^1	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	k Ω	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

Table 4-5 Peak Voltage and Leakage Current

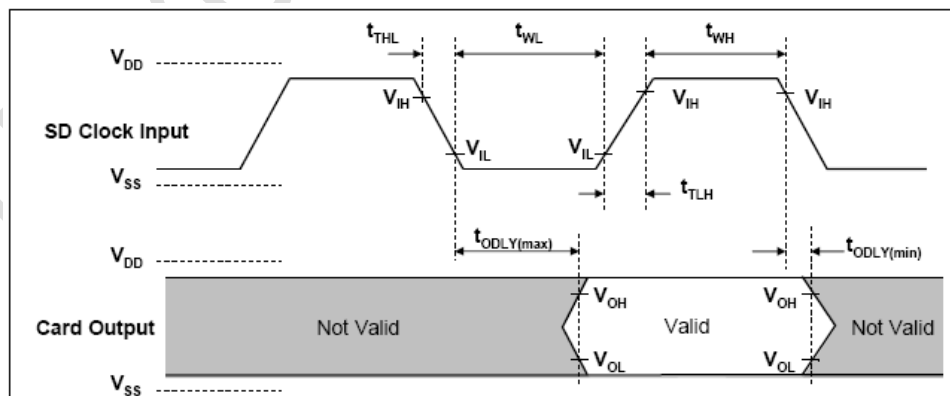
4.2 AC Characteristic



4.2.1 microSD Interface timing (Default)



Card Input Timing (Default Speed Card)

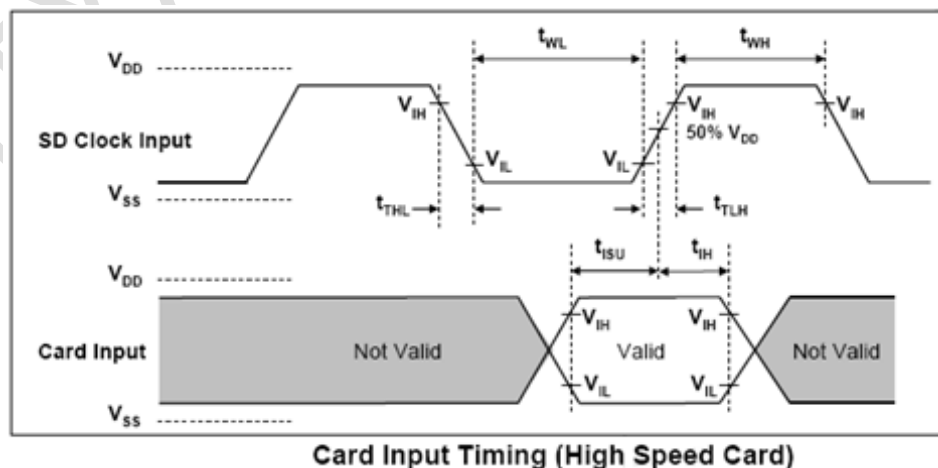


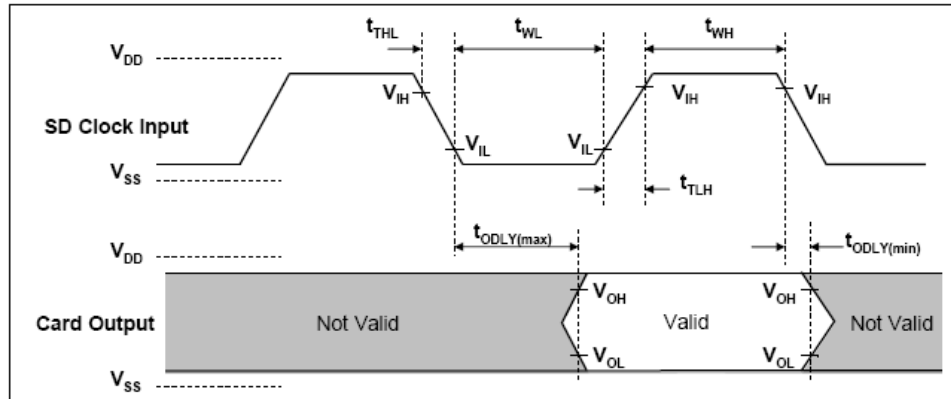
Card Output Timing (Default Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock frequency Identification Mode	f_{OD}	0 ₍₁₎ /100	400	KHz	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock low time	t_{WL}	10		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock high time	t_{WH}	10		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock rise time	t_{TLH}		10	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock fall time	t_{THL}		10	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Input hold time	t_{IH}	5		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	$C_L \leq 40 \text{ pF}$ (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	$C_L \leq 40 \text{ pF}$ (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continues clock is required.

4.2.2 microSD Interface Timing (High-Speed Mode)





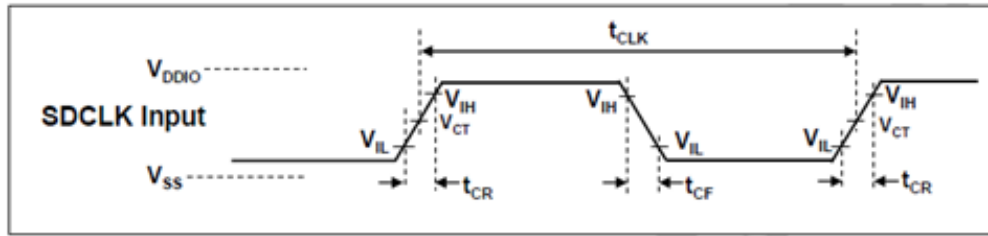
Card Output Timing (Default Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f_{pp}	0	50	MHz	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock low time	t_{WL}	7		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock high time	t_{WH}	7		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Clock fall time	t_{THL}		3	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Input hold time	t_{IH}	2		ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	$C_L \leq 40 \text{ pF}$ (1 card)
Output Hold time	T_{OH}	2.5		ns	$C_L \leq 15 \text{ pF}$ (1 card)
Total System capacitance of each line ¹	C_L		40	pF	$C_L \leq 15 \text{ pF}$ (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

4.2.3 microSD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes)

Input:

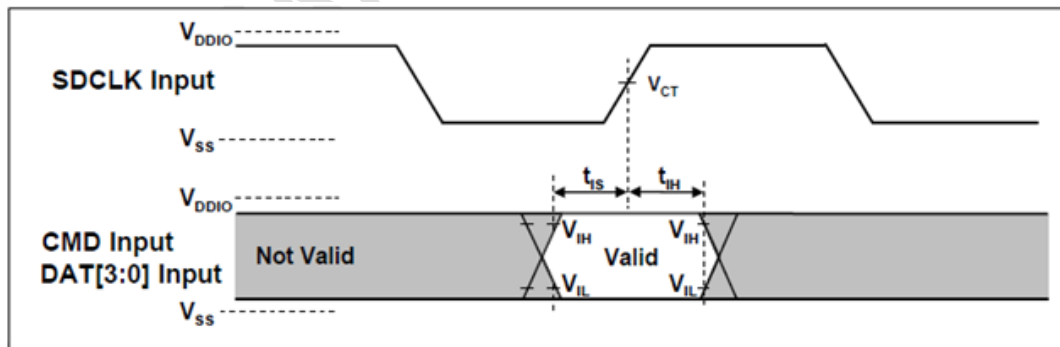


Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, $V_{CT}=0.975V$
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 0.96ns$ (max.) at 208MHz, $C_{CARD}=10pF$ $t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD}=10pF$ The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Clock Signal Timing

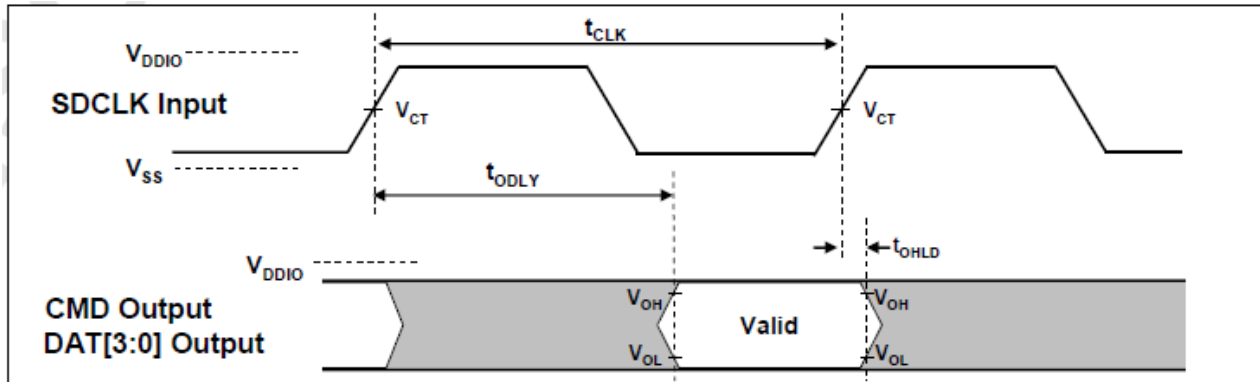
SDR50 and SDR104 Input Timing:



Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
t_{IH}	0.8	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$
Symbol	Min	Max	Unit	SDR50 Mode
t_{IS}	3.00	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
t_{IH}	0.8	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$

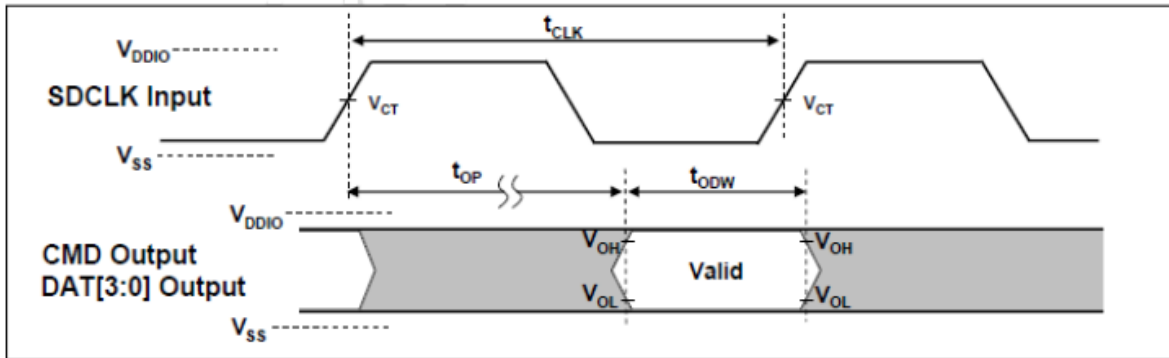
Output (SDR12, SDR25, SDR50):



Output Timing of Fixed Data Window

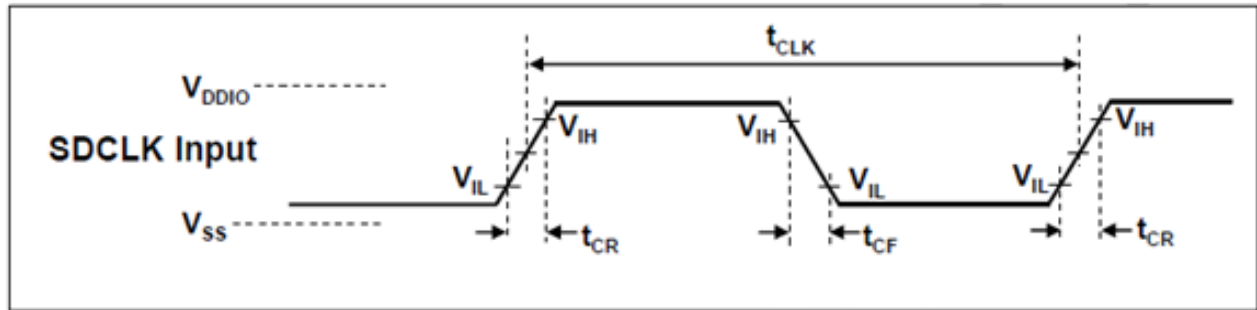
Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	$t_{CLK} \geq 10.0\text{ns}$, $C_L = 30\text{pF}$, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	$t_{CLK} \geq 20.0\text{ns}$, $C_L = 40\text{pF}$, using driver Type B, for SDR25 and SDR12,
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), $C_L = 15\text{pF}$

Output (SDR104 Mode):



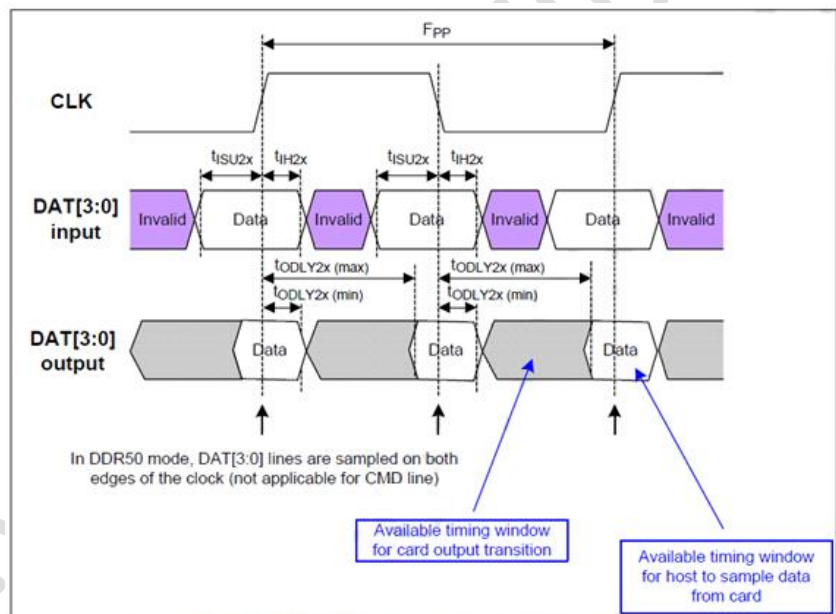
Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	$t_{ODW} = 2.88\text{ns}$ at 208MHz

4.2.4 microSD Interface timing (DDR50 Modes)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00\text{ns}$ (max.) at 50MHz, $C_{CARD}=10\text{pF}$
Clock Duty	45	55	%	

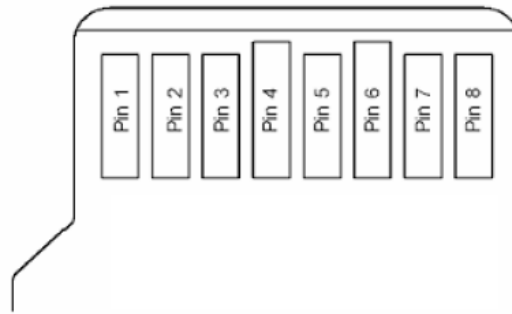


Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	$C_L \leq 30 \text{ pF}$ (1 card)
Output Hold time	T_{OH}	1.5	-	ns	$C_L \geq 15 \text{ pF}$ (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq 25 \text{ pF}$ (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	$C_L \geq 15 \text{ pF}$ (1 card)

Table 4-6 Bus Timings – Parameters Values (DDR50 Mode)

5. PAD ASSIGNMENT



Pin #	SD Mode			SPI Mode		
	Name	Type ¹	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[bit2]	RSV		
2	CD/DAT3 ²	I/O/PP ³	Card Detect/ Data Line[bit3]	CS	I ³	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V _{DD}	S	Supply voltage	V _{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V _{SS}	S	Supply voltage ground	V _{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		

Table 5-1 microSD Pad Assignment

NOTE:

- (1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers
- (2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.
- (3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, with SET_CLR_CARD_DETECT (ACMD42) command.

6. REGISTERS

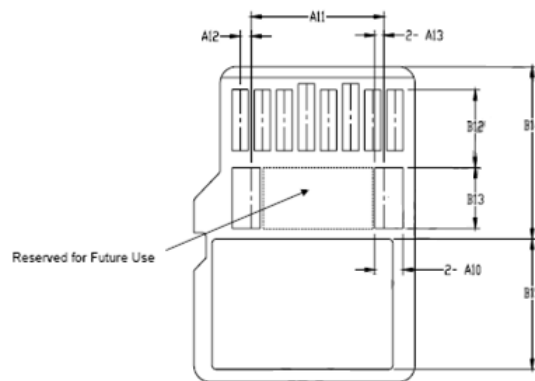
Name	Width	Description
CID	128bit	Card identification number; card individual number for identification.
RCA	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization.
DSR	16bit	Driver Stage Register; to configure the card's output drivers.
CSD	128bit	Card Specific Data; Information about the card operation conditions.
SCR	64bit	SD Configuration Register; Information about the SD Memory Card's Special Features capabilities
OCR	32bit	Operation conditions register.
SSR	512bit	SD Status; Information about the card proprietary features.
OCR	32bit	Card Status; Information about the card status.

Table 6-1 microSD Registers

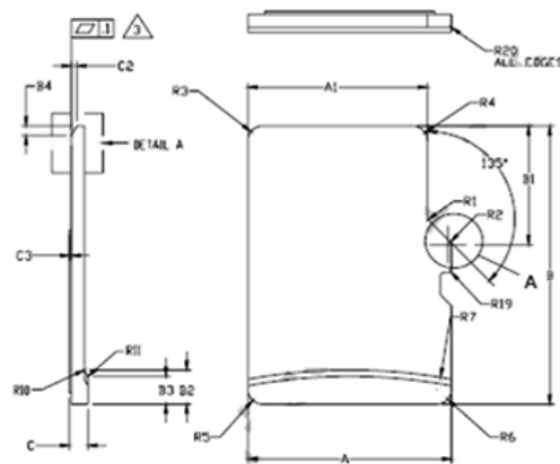
7. PHYSICAL DIMENSION

Dimension: 15mm (L) x 11mm (W) x 1mm (H)

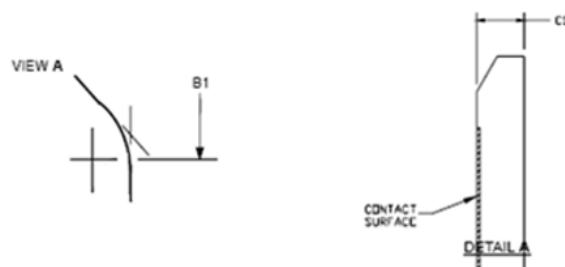
Top View



Bottom View



Side View



Common Dimensions				
Symbol	Min	Nom	Max	Note
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	Basic
A3	7.60	7.70	7.80	
A4	-	1.10	-	Basic
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.60	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	-	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Dimensions are in millimeters.
3. Coplanarity is additive to C1 Max. thickness

8. ORDERING INFORMATION

Capacity	MPN (Diamond Grade)	MPN (Gold Grade)
4GB	FDMM004GME-XE00	FDMM004GMG-XE00
8GB	FDMM008GME-XE00	FDMM008GMG-XE00
16GB	FDMM016GME-XE00	FDMM016GMG-XE00
32GB	FDMM032GME-XE00	FDMM032GMG-XE00
64GB	FDMM064GME-XE00	FDMM064GMG-XE00
128GB	FDMM128GME-XE00	FDMM128GMG-XE00

REVISION HISTORY

Revision	Date	History
Preliminary Version	2019/02	Preliminary Release
1.0	2019/03	First Release
1.1	2019/03	Update Product Specifications
1.2	2019/04	Update Ordering Information
1.3	2020/03	Update Product Overview and Ordering Information
1.4	2020/08	Update Performance
1.5	2020/11	Update Capacity

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