NMUX1309

1.5 V to 5.5 V, dual 4-channel switch analog multiplexer and demultiplexer with injection-current control

Rev. 1.2 — 16 April 2024 Product data sheet

1. General description

The NMUX1309 is a general purpose, CMOS, bi-directional, dual 4 channel analog switch, with an operating voltage range of 1.5 V to 5.5 V. The NMUX1309 is dual source compatible with existing 4852 and 4052 devices. The NUMX1309 extends the digital logic thresholds to be compatible with 1.8 V systems without the need for voltage translation.

The analog signal pins are comprised of two common inputs/outputs (nZ) and eight independent inputs/outputs (nY0 to nY3). All analog signal pins are bi-directional and support a voltage range from GND to V_{CC}.

All analog signal pins integrate injection current control circuitry. This control circuitry isolates overvoltage spikes on disconnected analog signal pins from coupling to the connected analog signal path, thereby preserving measurement accuracy. Additionally, this integration makes the use of external overvoltage clamp components (e.g. resistive diode network) unnecessary.

There are three control signal pins (S0, S1, and $\overline{E}$). S0 and S1 determine the analog channels to connect between nZ and nYn. $\overline{E}$ can be used to override S0 and S1, disconnecting all analog channels. The control signal pins support 1.8 V logic thresholds across all operating voltages. In addition, these pins are 5.5 V tolerant, enabling up to 5.5 V operation independent of supply voltage.

2. Features and benefits

- Wide operating range: 1.5 V to 5.5 V
- 2x SP4T-Z functionality
- Rail-to-Rail operation on analog signal pins
- Injection current control
- 1.8 V digital logic thresholds
  - Digital pins compatible with 1.8 V logic thresholds across full V_{CC} range
  - Removes need for up-translation device for compatibility with low voltage GPIOs
- I_{off} circuitry
  - Enables wider latitude for power sequencing considerations
  - Isolates backflow between supply rail and any biased digital/analog input when V_{CC} = 0 V
  - Prevents any biased digital/analog input from backpowering V_{CC} when V_{CC} = 0 V
  - Maintains Hi-Z state of analog switch when V_{CC} = 0 V
- 5.5 V overvoltage tolerant digital inputs
  - Supports switching of 5.5 V digital signals across full V_{CC} operating range
  - Removes need for down-translation when switching thresholds are met
- Pin compatible with industry standard 4052 and 4852 analog switch products
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C2b exceeds 750 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

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3. Applications

- Analog or digital multiplexing/demultiplexing
- System monitoring and diagnostics
- Enterprise computing
- Appliances

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NMUX1309PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
NMUX1309BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Marking

Table 2. Marking

Type number	Marking code
NMUX1309PW	NMU1309
NMUX1309BQ	NM1309

6. Functional diagram

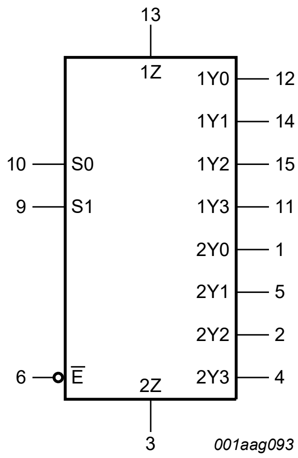


Fig. 1. Logic symbol

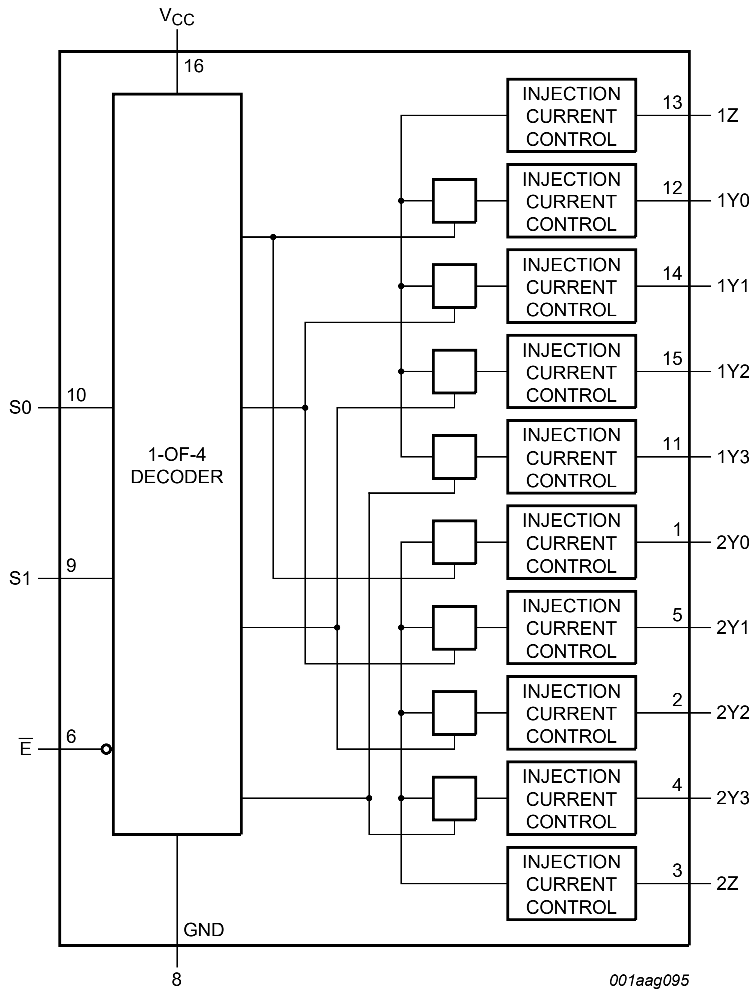
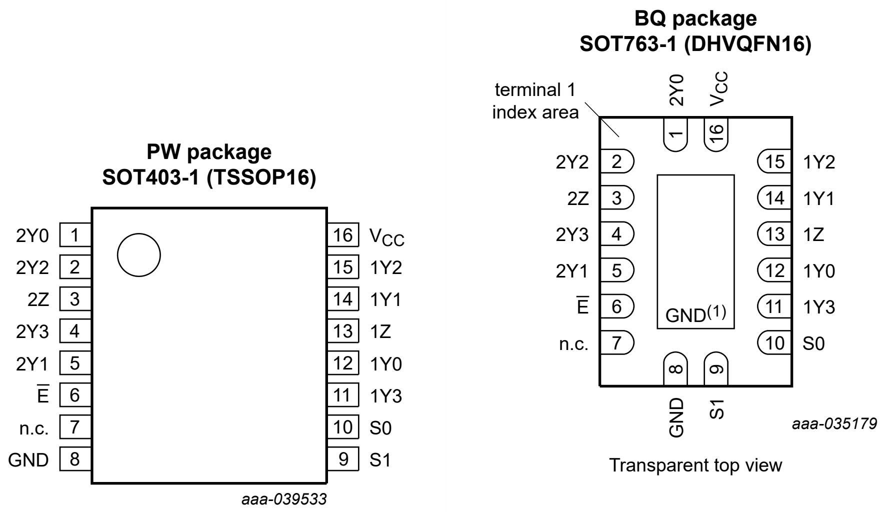


Fig. 2. Functional diagram

7. Pinning information

7.1. Pinning



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
2Y0	1	independent input/output
2Y2	2	independent input/output
2Z	3	common input/output
2Y3	4	independent input/output
2Y1	5	independent input/output
$\overline{E}$	6	enable input (active LOW); do not leave this pin floating
n.c.	7	not connected
GND	8	ground (0 V)
S1	9	select input; do not leave this pin floating
S0	10	select input; do not leave this pin floating
1Y3	11	independent input/output
1Y0	12	independent input/output
1Z	13	common input/output
1Y1	14	independent input/output
1Y2	15	independent input/output
V_{CC}	16	supply voltage

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input			Channel ON
$\overline{E}$	S1	S0	
L	L	L	nY0 to nZ
L	L	H	nY1 to nZ
L	H	L	nY2 to nZ
L	H	H	nY3 to nZ
H	X	X	-

8.1. Overview

The NMUX1309 is a general purpose analog switch with a 2 poles, each of which can be configured to select between one of four possible connection paths (2x SP4T). Each analog connection path is bi-directional, with similar electrical characteristics independent of the direction of signal propagation.

8.2. Key features

Injection current control

Current injection can occur in systems where an analog voltage can experience transient spikes due to signal propagation over long distances with high inductance. Voltage exposure above the supply voltage will source excessive current into an analog input, which is referred to as positive injection. Voltage exposure below the ground voltage will sink excessive current from an analog input, which is referred to as negative injection. Both types of injection current elevate the risk of device damage to an analog input and can introduce a large voltage error to the analog signal itself.

The NMUX1309 mitigates both risks by integrating an injection current control circuit to divert both positive injection and negative injection through a bypass FET that connects to GND. This implementation minimizes any shift in the supply voltage, therefore minimizing any shift in the device's ON Resistance, and thus minimizes changes in the measured analog voltage. The injection current control circuit is active on all analog pins, independent of whether the channel is selected/unselected.

1.8 V Compatible digital logic thresholds

It is common for modern systems to operate digital signals from lower voltage nodes such as 1.8 V, while operating their analog signals at higher voltage nodes such as 3.3 V or 5.0 V. To remove the requirements for a voltage translation device, the NMUX1309 digital control pins maintain 1.8 V logic compatible thresholds at higher operating voltages, up to 5.5 V.

I_{off} protection circuitry of digital inputs

The NMUX1309 implements I_{off} protection circuitry on the digital control pins, isolating those pins from the internal circuits when the supply is unpowered (i.e., V_{CC} = 0 V). The ESD protection diodes on the digital input pins do not have a connection path to V_{CC}. If the digital input pins are biased when the V_{CC} pin is unpowered:

1. The high impedance of the digital input pins minimizes input current leakage.

2. The isolation between the digital input pins and the V_{CC} pin ensures no back-powering to the supply rail.

I_{off} protection circuitry of analog inputs/outputs

The NMUX1309 implements I_{off} protection circuitry on the analog switch pins, isolating those pins from the internal circuits when the supply is unpowered (i.e., V_{CC} = 0 V). The ESD protection diodes on the analog switch pins do not have a connection path to V_{CC}. If the analog switch pins are biased when the V_{CC} pin is unpowered:

1. The high impedance of the analog pins minimizes input current leakage.
2. The isolation between the analog pins and the V_{CC} pin ensures no back-powering to the supply rail.
3. The high impedance of the analog switch path itself minimizes signal coupling across the switch.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.0	V
V_I	input voltage	$\overline{E}$, S0, S1 [1]	-0.5	+6.0	V
V_{SW}	switch voltage	nYn, nZ [2]	-0.5	V_{CC} + 0.5	V
I_{SW}	switch current	nYn, nZ; V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V; T_{amb} = -40 °C to +85 °C	-50	+50	mA
		nYn, nZ; V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V; T_{amb} = -40 °C to +125 °C	-25	+25	mA
I_I	input current	$\overline{E}$, S0, S1	-30	30	mA
I_{GND}	ground current		-100	100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [3]	-	500	mW
T_j	junction temperature		-	+150	°C

[1] The minimum and maximum input voltage rating may be exceeded if the input clamping current rating is observed.
[2] The minimum and maximum switch voltage rating may be exceeded if the switch clamping current rating is observed.
[3] For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.50	-	5.5	V
V_I	input voltage	$\overline{E}$, S0, S1	0	-	5.5	V
V_{SW}	switch voltage	nYn, nZ; enable and disable mode	0	-	V_{CC}	V
		nYn, nZ; V_{CC} = 0 V	0	-	5.5	V
I_{SW}	switch current	nYn, nZ; V_{SW} > GND or V_{SW} < V_{CC}; T_{amb} = -40 °C to + 85 °C	-50	-	50	mA
		nYn, nZ; V_{SW} > GND or V_{SW} < V_{CC}; T_{amb} = -40 °C to +125 °C	-25	-	25	mA
I_{SK}	switch clamping current	nYn, nZ; V_{SW} < GND or V_{SW} > V_{CC} [1]	-50	-	50	mA
I_{GND}	ground current		-100	-	100	mA
I_{INJ}	injected current	single off switch	-25	-	50	mA
		all off switches combined	-100	-	100	mA
T_{amb}	ambient temperature		-40	-	+125	°C

[1] If the V_{SW} > V_{CC} or if V_{SW} < GND, the pin will be shunted to GND through an internal FET. The current must be limited within the specified value.

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 4.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Analog switch										
R_{ON}	ON resistance	V_I = V_{CC} to GND; I_{SW} = 0.5 mA; $\overline{E}$ = V_{IL}; see Fig. 5								
		V_{CC} = 1.8 V ± 10%	-	450	1151	-	1245	-	1245	Ω
		V_{CC} = 2.5 V ± 10%	-	160	388	-	419	-	436	Ω
		V_{CC} = 3.3 V ± 10%	-	95	231	-	262	-	278	Ω
		V_{CC} = 5 V ± 10%	-	60	146	-	167	-	178	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = 0.5V_{CC}; I_{SW} = 0.5 mA; $\overline{E}$ = V_{IL}								
		V_{CC} = 1.8 V ± 10%	-	5	91	-	91	-	91	Ω
		V_{CC} = 2.5 V ± 10%	-	4	35	-	39	-	41	Ω
		V_{CC} = 3.3 V ± 10%	-	2	17	-	19	-	19	Ω
		V_{CC} = 5 V ± 10%	-	1	11	-	11	-	12	Ω

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_{S(OFF)}$	OFF-state leakage current	nYn pins; switch off; $\overline{E} = V_{IH}$; $V_I = 0.8V_{CC}$ or $0.2V_{CC}$; $V_O = 0.2V_{CC}$ or $0.8V_{CC}$; see Fig. 3								
		V_{CC} = 1.8 V ± 10%	-	±1	-	-25	25	-800	800	nA
		V_{CC} = 2.5 V ± 10%	-	±1	-	-25	25	-800	800	nA
		V_{CC} = 3.3 V ± 10%	-	±1	-	-25	25	-800	800	nA
		V_{CC} = 5 V ± 10%	-	±1	-	-25	25	-800	800	nA
		Z pins; switch off; $\overline{E} = V_{IH}$; $V_I = 0.8V_{CC}$ or $0.2V_{CC}$; $V_O = 0.2V_{CC}$ or $0.8V_{CC}$; see Fig. 3								
		V_{CC} = 1.8 V ± 10%	-	±1	-	-45	45	-800	800	nA
		V_{CC} = 2.5 V ± 10%	-	±1	-	-45	45	-800	800	nA
		V_{CC} = 3.3 V ± 10%	-	±1	-	-45	45	-800	800	nA
		V_{CC} = 5 V ± 10%	-	±1	-	-45	45	-800	800	nA
$I_{S(ON)}$	ON-state leakage current	nZ, nYn pins; switch on; $\overline{E} = V_{IL}$; $V_I = V_O = 0.8V_{CC}$ or $V_I = V_O = 0.2V_{CC}$; see Fig. 4								
		V_{CC} = 1.8 V ± 10%	-	±1	-	-45	45	-800	800	nA
		V_{CC} = 2.5 V ± 10%	-	±1	-	-45	45	-800	800	nA
		V_{CC} = 3.3 V ± 10%	-	±1	-	-45	45	-800	800	nA
		V_{CC} = 5 V ± 10%	-	±1	-	-45	45	-800	800	nA
C_{SW}	switch capacitance	nYn pins, OFF-state; $V_I = 0.5V_{CC}$; f = 1 MHz								
		V_{CC} = 1.8 V ± 10%	-	4	10	-	10	-	10	pF
		V_{CC} = 2.5 V ± 10%	-	4	9	-	9	-	9	pF
		V_{CC} = 3.3 V ± 10%	-	4	9	-	9	-	9	pF
		V_{CC} = 5 V ± 10%	-	4	9	-	9	-	9	pF
		nZ pins, OFF-state; $V_I = 0.5V_{CC}$; f = 1 MHz								
		V_{CC} = 1.8 V ± 10%	-	10	23	-	23	-	23	pF
		V_{CC} = 2.5 V ± 10%	-	10	22	-	22	-	22	pF
		V_{CC} = 3.3 V ± 10%	-	9	21	-	22	-	22	pF
		V_{CC} = 5 V ± 10%	-	9	20	-	20	-	20	pF
		nZ, nYn pins; ON-state; $V_I = 0.5V_{CC}$; f = 1 MHz								
		V_{CC} = 1.8 V ± 10%	-	16	31	-	32	-	32	pF
		V_{CC} = 2.5 V ± 10%	-	16	31	-	31	-	31	pF
		V_{CC} = 3.3 V ± 10%	-	16	30	-	31	-	31	pF
		V_{CC} = 5 V ± 10%	-	15	29	-	30	-	30	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Power supply										
I_{CC}	supply current	$\overline{E}$, Sn inputs; V_I = GND or V_{CC}								
		V_{CC} = 1.8 V ± 10%	-	-	1	-	1	-	1	μA
		V_{CC} = 2.5 V ± 10%	-	-	1	-	1	-	1	μA
		V_{CC} = 3.3 V ± 10%	-	-	1	-	1	-	1	μA
		V_{CC} = 5 V ± 10%	-	-	1	-	1	-	1	μA

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 to +125 °C			Unit
			Min	Typ [1]	Max	
Injection current coupling						
ΔV_O	output voltage variation	I_{SW} ≤ 1 mA; R_S ≤ 3.9 kΩ [2] [3]				
		V_{CC} = 1.8 V ± 10%	-	0.1	1	mV
		V_{CC} = 3.3 V ± 10%	-	0.2	1	mV
		V_{CC} = 5 V ± 10%	-	0.4	2	mV
		I_{SW} ≤ 10 mA; R_S ≤ 3.9 kΩ [2] [3]				
		V_{CC} = 1.8 V ± 10%	-	0.1	2	mV
		V_{CC} = 3.3 V ± 10%	-	0.2	2	mV
		V_{CC} = 5 V ± 10%	-	0.4	2	mV
		I_{SW} ≤ 1 mA; R_S ≤ 20 kΩ [2][3]				
		V_{CC} = 1.8 V ± 10%	-	0.1	2	mV
		V_{CC} = 3.3 V ± 10%	-	0.2	2	mV
		V_{CC} = 5 V ± 10%	-	0.4	2	mV
		I_{SW} ≤ 10 mA; R_S ≤ 20 kΩ [2][3]				
		V_{CC} = 1.8 V ± 10%	-	0.1	5	mV
		V_{CC} = 3.3 V ± 10%	-	0.2	5	mV
		V_{CC} = 5 V ± 10%	-	0.4	5	mV
Logic inputs						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.8 V ± 10%	0.99	-	5.5	V
		V_{CC} = 2.5 V ± 10%	1.08	-	5.5	V
		V_{CC} = 3.3 V ± 10%	1.15	-	5.5	V
		V_{CC} = 5 V ± 10%	1.32	-	5.5	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.8 V ± 10%	0	-	0.53	V
		V_{CC} = 2.5 V ± 10%	0	-	0.61	V
		V_{CC} = 3.3 V ± 10%	0	-	0.68	V
		V_{CC} = 5 V ± 10%	0	-	0.79	V
I_{IH}	HIGH-level input current	V_I = 1.8 V or V_{CC}	-	-	1	μA
I_{IL}	LOW-level input current	V_I = 0 V	-1	-	-	μA

Symbol	Parameter	Conditions	-40 to +125 °C			Unit
			Min	Typ [1]	Max	
C_I	input capacitance	S0, S1, and $\overline{E}$ pins; V_I = 0 V, 1.8 V, or V_{CC}; f = 1 MHz	-	1.5	3.5	pF

[1] Typical values are measured at T_{amb} = 25 °C.
[2] ΔV_O here is the maximum variation of output voltage of an enabled analog channel when current is injected into any disabled channel.
[3] I_{SW} = total current injected into all disabled channels.

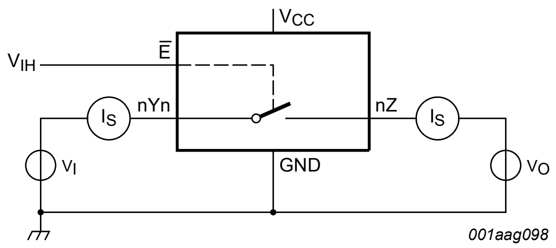
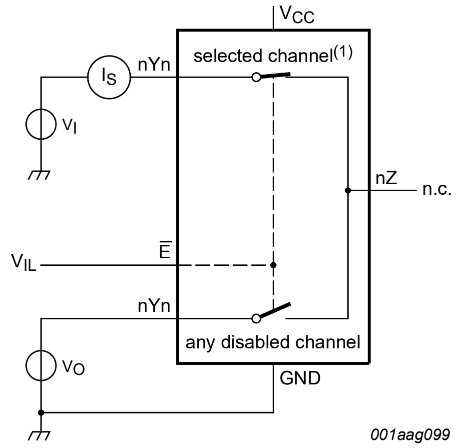
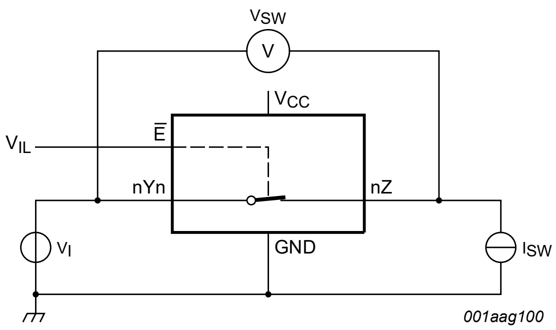


Fig. 3. Test circuit for measuring OFF-state leakage current



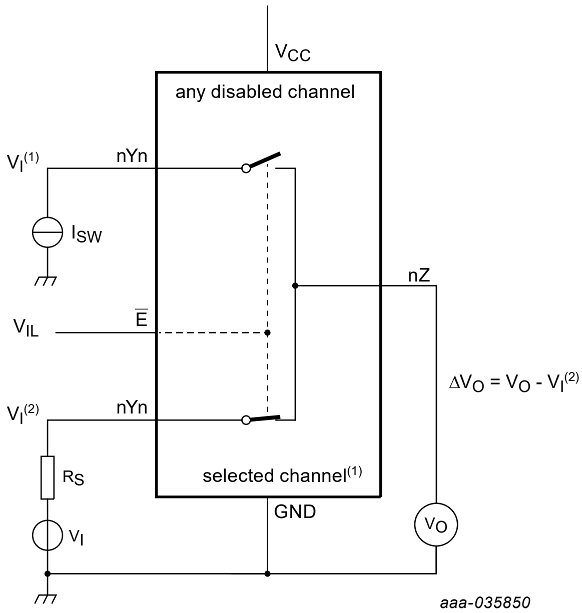
(1) Channel is selected by S0 and S1.

Fig. 4. Test circuit for measuring ON-state leakage current



$R_{ON} = V_{SW} / I_{SW}$.

Fig. 5. Test circuit for measuring ON resistance



(1) Channel is selected by S0 and S1.
V_I (1) < GND or V_I (1) > V_{CC}.
GND < V_I (2) < V_{CC}.

Fig. 6. Test circuit for injection current coupling

12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	nZ to nYn, nYn to nZ; C_L = 50 pF; see Fig. 7 [1]								
		V_{CC} = 1.8 V ± 10%	-	9	22	-	25	-	26	ns
		V_{CC} = 2.5 V ± 10%	-	6	10	-	11	-	12	ns
		V_{CC} = 3.3 V ± 10%	-	4	6	-	7	-	8	ns
		V_{CC} = 5 V ± 10%	-	2	4	-	5	-	5	ns
		V_{CC} = 5.0 V ± 10%; C_L = 15 pF	-	1	3	-	3	-	3	ns
t_{pd}	transition time between inputs	Sn to nZ; R_L = 10 kΩ; C_L = 50 pF; see Fig. 8 [1]								
		V_{CC} = 1.8 V ± 10%	-	52	93	-	93	-	93	ns
		V_{CC} = 2.5 V ± 10%	-	40	67	-	74	-	74	ns
		V_{CC} = 3.3 V ± 10%	-	36	61	-	71	-	71	ns
		V_{CC} = 5.0 V ± 10%	-	33	60	-	70	-	70	ns
		V_{CC} = 5.0 V ± 10%; C_L = 15 pF	-	31	58	-	70	-	70	ns
		Sn to nYn; R_L = 10 kΩ; C_L = 50 pF; see Fig. 8 [1]								
		V_{CC} = 1.8 V ± 10%	-	108	359	-	363	-	364	ns
		V_{CC} = 2.5 V ± 10%	-	96	349	-	351	-	351	ns
		V_{CC} = 3.3 V ± 10%	-	93	344	-	344	-	344	ns
		V_{CC} = 5.0 V ± 10%	-	85	335	-	335	-	336	ns
		V_{CC} = 5.0 V ± 10%; C_L = 15 pF	-	40	93	-	94	-	94	ns
t_{en}	enable time	$\overline{E}$ to nZ, $\overline{E}$ to nYn; R_L = 10 kΩ; C_L = 50 pF; see Fig. 9 [2]								
		V_{CC} = 1.8V ± 10%	-	15	25	-	27	-	29	ns
		V_{CC} = 2.5 V ± 10%	-	12	17	-	18	-	18	ns
		V_{CC} = 3.3 V ± 10%	-	12	17	-	18	-	18	ns
		V_{CC} = 5 V ± 10%	-	12	17	-	18	-	18	ns
		V_{CC} = 5.0 V ± 10%; C_L = 15 pF	-	11	16	-	17	-	17	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{dis}	disable time	$\overline{E}$ to nZ, $\overline{E}$ to nYn; R_L = 10 kΩ; C_L = 50 pF; S1 = GND; see Fig. 9 [3]								
		V_{CC} = 1.8 V ± 10%	-	23	47	-	48	-	49	ns
		V_{CC} = 2.5 V ± 10%	-	16	37	-	37	-	37	ns
		V_{CC} = 3.3 V ± 10%	-	16	37	-	37	-	37	ns
		V_{CC} = 5 V ± 10%	-	16	31	-	32	-	33	ns
		V_{CC} = 5.0 V ± 10%; C_L = 15 pF	-	3	5	-	5	-	6	ns
		$\overline{E}$ to nYn; R_L = 10 kΩ; C_L = 50 pF; S1 = V_{CC}; see Fig. 9								
		V_{CC} = 1.8 V ± 10%	-	13	72	-	72	-	72	ns
		V_{CC} = 2.5 V ± 10%	-	10	70	-	70	-	71	ns
		V_{CC} = 3.3 V ± 10%	-	9	70	-	70	-	70	ns
		V_{CC} = 5 V ± 10%	-	7	69	-	69	-	70	ns
		V_{CC} = 5.0 V ± 10%; C_L = 15 pF	-	5	34	-	34	-	35	ns
t_{b-m}	break-before-make time	R_L = 10 kΩ; C_L = 15 pF; nYn to nZ								
		V_{CC} = 1.8 V ± 10%	1	35	-	1	-	1	-	ns
		V_{CC} = 2.5 V ± 10%	1	30	-	1	-	1	-	ns
		V_{CC} = 3.3 V ± 10%	1	29	-	1	-	1	-	ns
		V_{CC} = 5 V ± 10%	1	27	-	1	-	1	-	ns

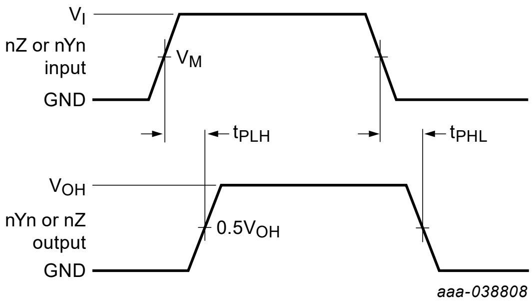
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_{en} is the same as t_{PZH} and t_{PZL}.
[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

Table 10. Dynamic characteristics

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	
Q_{inj}	charge injection	V_I = 0.5V_{CC}; R_S= 0 Ω; C_L = 100 pF				
		V_{CC} = 1.8 V ± 10%	-	1	-	pC
		V_{CC} = 2.5 V ± 10%	-	2	-	pC
		V_{CC} = 3.3 V ± 10%	-	3	-	pC
		V_{CC} = 5 V ± 10%	-	8	-	pC

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	
α_{iso}	isolation (OFF-state)	V_{bias} = 0.5V_{CC}; V_I = 200 mVpp; R_L = 50 Ω; C_L = 5 pF; f = 100 kHz				
		V_{CC} = 1.8 V ± 10%	-	-105	-	dB
		V_{CC} = 2.5 V ± 10%	-	-105	-	dB
		V_{CC} = 3.3 V ± 10%	-	-105	-	dB
		V_{CC} = 5 V ± 10%	-	-105	-	dB
		V_{bias} = 0.5V_{CC}; V_I = 200 mVpp; R_L = 50 Ω; C_L = 5 pF; f = 1 MHz				
		V_{CC} = 1.8 V ± 10%	-	-80	-	dB
		V_{CC} = 2.5 V ± 10%	-	-80	-	dB
		V_{CC} = 3.3 V ± 10%	-	-80	-	dB
		V_{CC} = 5 V ± 10%	-	-80	-	dB
X_{talk}	crosstalk	V_{bias} = 0.5V_{CC}; V_I = 200 mVpp; R_L = 50 Ω; C_L = 5 pF; f = 100 kHz				
		V_{CC} = 1.8 V ± 10%	-	-105	-	dB
		V_{CC} = 2.5 V ± 10%	-	-105	-	dB
		V_{CC} = 3.3 V ± 10%	-	-105	-	dB
		V_{CC} = 5 V ± 10%	-	-105	-	dB
		V_{bias} = 0.5V_{CC}; V_I = 200 mVpp; R_L = 50 Ω; C_L = 5 pF; f = 1 MHz				
		V_{CC} = 1.8 V ± 10%	-	-80	-	dB
		V_{CC} = 2.5 V ± 10%	-	-80	-	dB
		V_{CC} = 3.3 V ± 10%	-	-80	-	dB
		V_{CC} = 5 V ± 10%	-	-80	-	dB
BW	Bandwidth	V_{bias} = 0.5V_{CC}; V_I = 200 mVpp; R_L = 50 Ω; C_L = 5 pF				
		V_{CC} = 1.8 V ± 10%	-	330	-	MHz
		V_{CC} = 2.5 V ± 10%	-	355	-	MHz
		V_{CC} = 3.3 V ± 10%	-	365	-	MHz
		V_{CC} = 5 V ± 10%	-	380	-	MHz

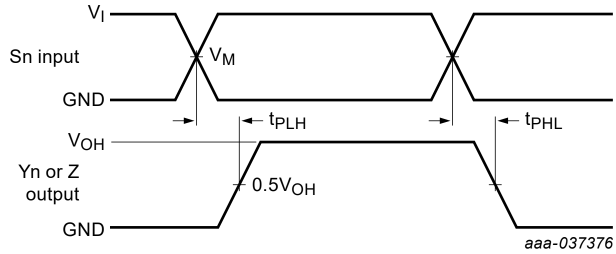
12.1. Waveforms and test circuit



Measurement points are given in Table 11.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

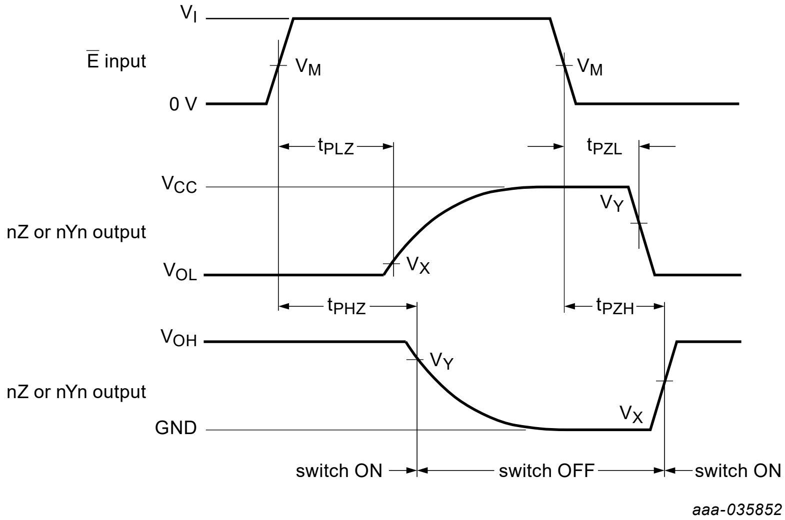
Fig. 7. Input (nZ, nYn) to output (nYn, nZ) propagation delays



Measurement points are given in Table 11.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Input (Sn) to output (nYn, nZ) propagation delays



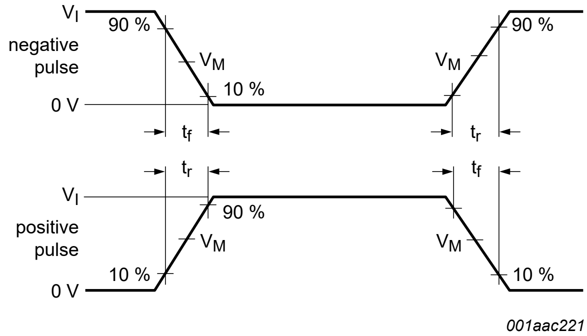
Measurement points are shown in Table 11.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

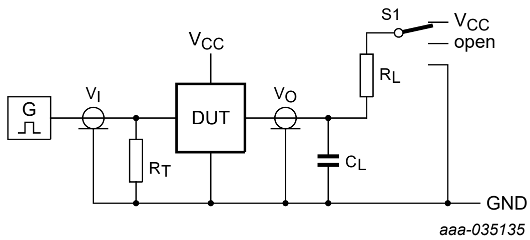
Fig. 9. Enable and disable times

Table 11. Measurement points

Input		Output	
V_M	V_I	V_X	V_Y
$0.5 \times V_{CC}$	V_{CC}	$V_{OL} + 0.1(V_{CC} - V_{OL})$	$0.9 \times V_{OH}$



a. Input pulse definition



Test data is given in Table 12.
Definitions for test circuit:
R_L = load resistance;
C_L = load capacitance including jig and probe capacitance;
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
b. Test circuit

Fig. 10. Input pulse definition and test circuit

Table 12. Test data

Test	Input			Output		S1 position
	Control $\overline{E}$, Sn	Switch nYn (nZ)	t_r, t_f	Switch nZ (nYn)		
	V_I	V_I		C_L	R_L	
t_{PHL}, t_{PLH}	V_{CC}	V_{CC}	< 5 ns	50 pF	-	open
t_{PHZ}, t_{PZH}	V_{CC}	V_{CC}	< 5 ns	50 pF	10 kΩ	GND
t_{PLZ}, t_{PZL}	V_{CC}	V_{CC}	< 5 ns	50 pF	10 kΩ	V_{CC}

13. Application information

NMUX1309

The NMUX1309 is a versatile CMOS bi-directional dual (4:1) analog switch designed for general-purpose use, operating within a voltage range of 1.5 V to 5.5 V. It features 5.5V overvoltage tolerant digital inputs and is compatible with 1.8 V CMOS levels, eliminating the need for voltage translation.

Each analog signal pin on the NMUX1309 incorporates injection current control circuitry. This innovative feature serves to isolate overvoltage spikes on disconnected analog signal pins, preventing them from affecting the connected analog signal path. Two other protective features include Fail-Safe-Logic and Power-off-Protection. These attributes make the NMUX130X family of devices the ideal choice for applications aiming to simplify signal management and reduce system complexity, resulting in a lower component count and a smaller PCB area. This utilization allows users to adopt a design approach centered around modularity, reuse, and scalability.

Typical application schematic

A typical example is provided in Fig. 11. In this instance, two sensors or voltage inputs are simultaneously sampled, such as 1Y0 and 2Y0, while sequentially stepping to the next two inputs based on the control input values. These inputs are read and accessed by the input of the SAR ('Successive Approximation Register') ADC. In the example below, the SAR ADC is integrated in the Microcontroller – ADC1 and ADC2. The operational amplifiers serve the purpose of satisfying the SAR ADCs recommendation of being driven with a low-impedance source, especially when input sensors or signals have large output impedance. This enhancement improves the performance of the SAR ADC, ensuring fast and accurate conversions while minimizing errors during the sampling process. Additionally, the op-amp eliminates potential error sources, such as ADC input leakage current, that can cause a small drop, resulting in a minor voltage error across the analog multiplexer.

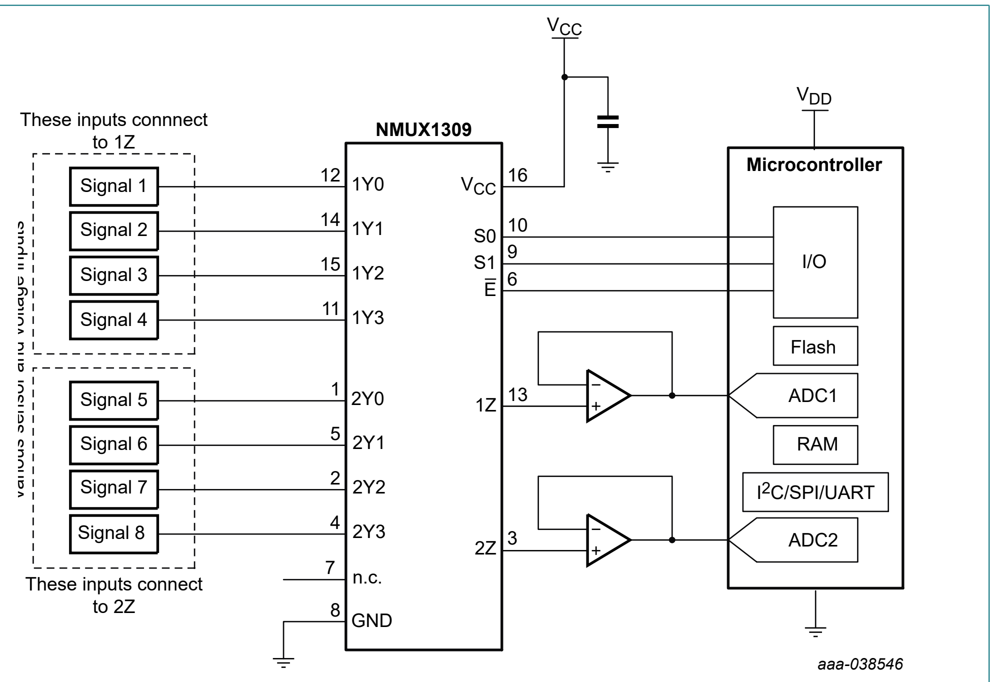


Fig. 11. Dual (4:1) -channel multiplexing with NMUX1309 to microcontroller with integrated ADC

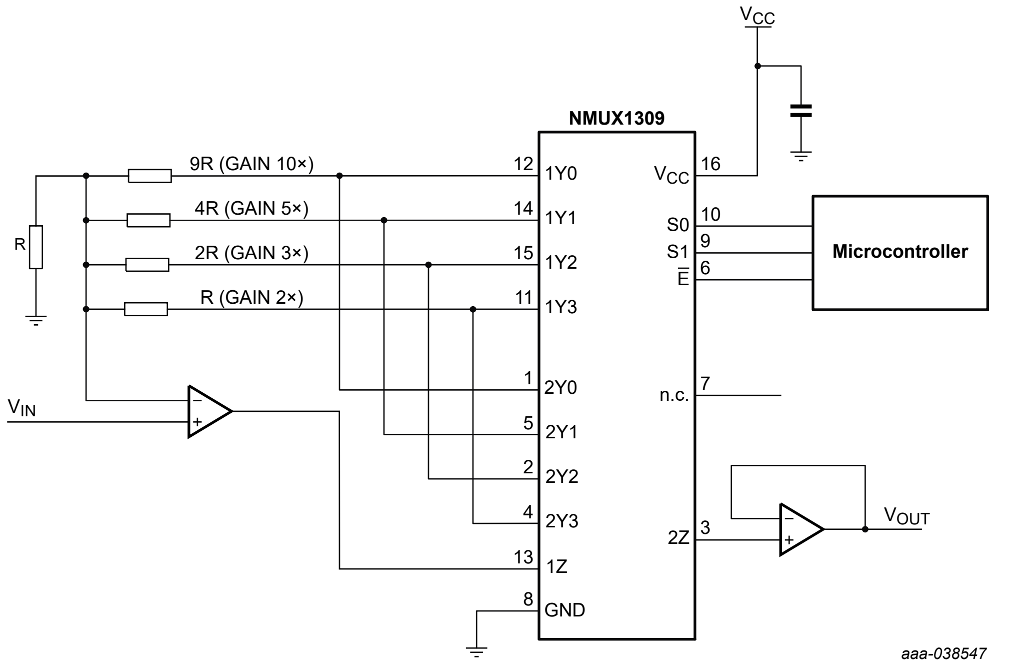
The benefits of this design type include the capability to route and switch multiple analog signals through two output channels. This is particularly crucial when the number of ADC input channels is limited.

Table 13. Example design parameters with NMUX1309

Important Design Parameters	Example Value
Supply range (V_{CC})	1.5 V to 5.5 V
Analog input voltage range	0 V to V_{CC} (rail-to-rail)
Control input logic	1.8 V compatible (5.5 V overvoltage tolerant)
I_{SW} independent switch current (maximum)	50 mA
Total analog input continuous current to GND (maximum)	100 mA

Additional example application

The circuit shown in Fig. 12 highlights the use of the NMUX1309 to create a high-precision selectable gain circuit. It eliminates error sources attributed to on-resistance and non-linearities by establishing a Kelvin sense connection from the second-stage buffer to the selected connected inputs.



See also Table 14

Fig. 12. High precision selectable GAIN circuit with NMUX1309. Connected in Kelvin sense configuration to eliminate error due to switch on-resistance

Table 14. Gain select

S1	S0	Gain
0	0	V_{OUT} = 10x V_{IN}
0	1	V_{OUT} = 5x V_{IN}
1	0	V_{OUT} = 3x V_{IN}
1	1	V_{OUT} = 2x V_{IN}

NMUX1309 layout example

The image provided below (Fig. 13) offers a glimpse into an example PCB layout with the (PW) package. Bypass capacitors should be positioned near the V_{CC} pin, and the GND pin should be connected to external/internal GND planes. A uniform GND plane helps in reducing noise and minimizing loop inductance, thereby ensuring optimal performance.

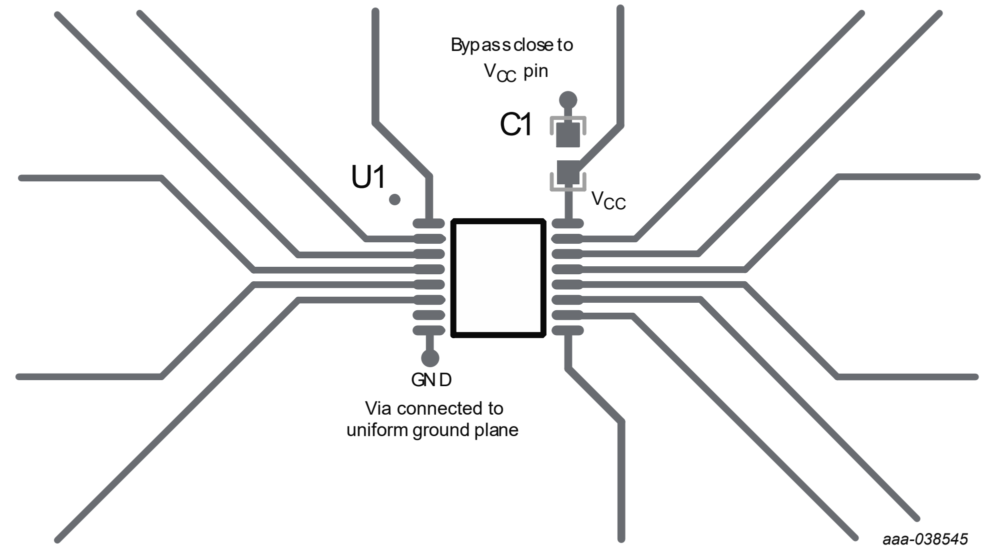


Fig. 13. NMUX1309 layout example with NMUX1309PW (TSSOP16/SOT403-1) package

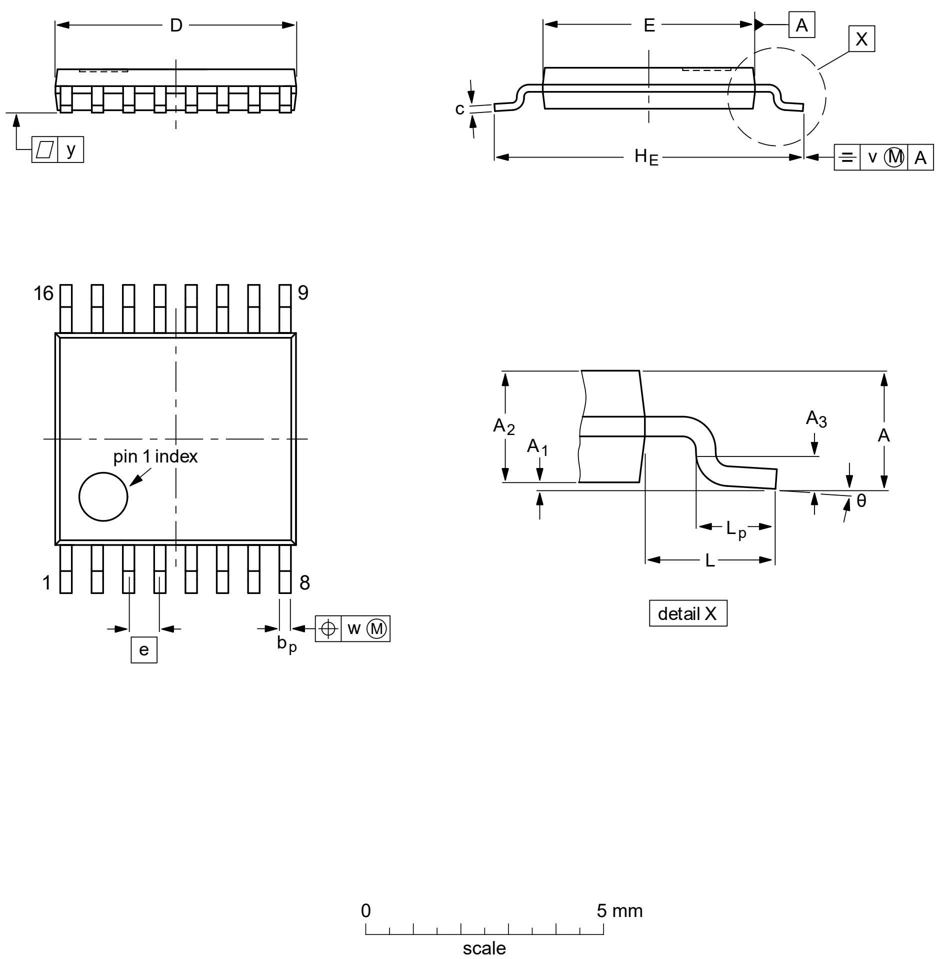
Layout recommendations

As with all board designs, proper layout techniques should be employed. Some quick good layout practices and considerations are listed below for quick reference.

- Ceramic capacitors with low ESR should be used to properly decouple or bypass power-supply pins. Ceramic capacitors with high temperature coefficients and low dissipation factors include X5R, X7R and NP0. The recommended minimum value is 0.1 μF.
- For improved noise suppression, additional bypass capacitors can be implemented. It is a common practice to use two different capacitor values to ensure proper filtering of both low-frequency and high-frequency transients. The smaller capacitor, typically in a 0402 package, is placed very near the device pin, while the larger capacitor is positioned farther away.
- To minimize coupling and improve performance all switching nets should travel across a uniform ground plane. Reducing crosstalk can also be achieved by separating traces with a small polygon ground plane.
- Net traces should only have serpentine or 45° bend. Sharper bends, such as 90° should be avoided.

14. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
mm	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 14. Package outline SOT403-1 (TSSOP16)

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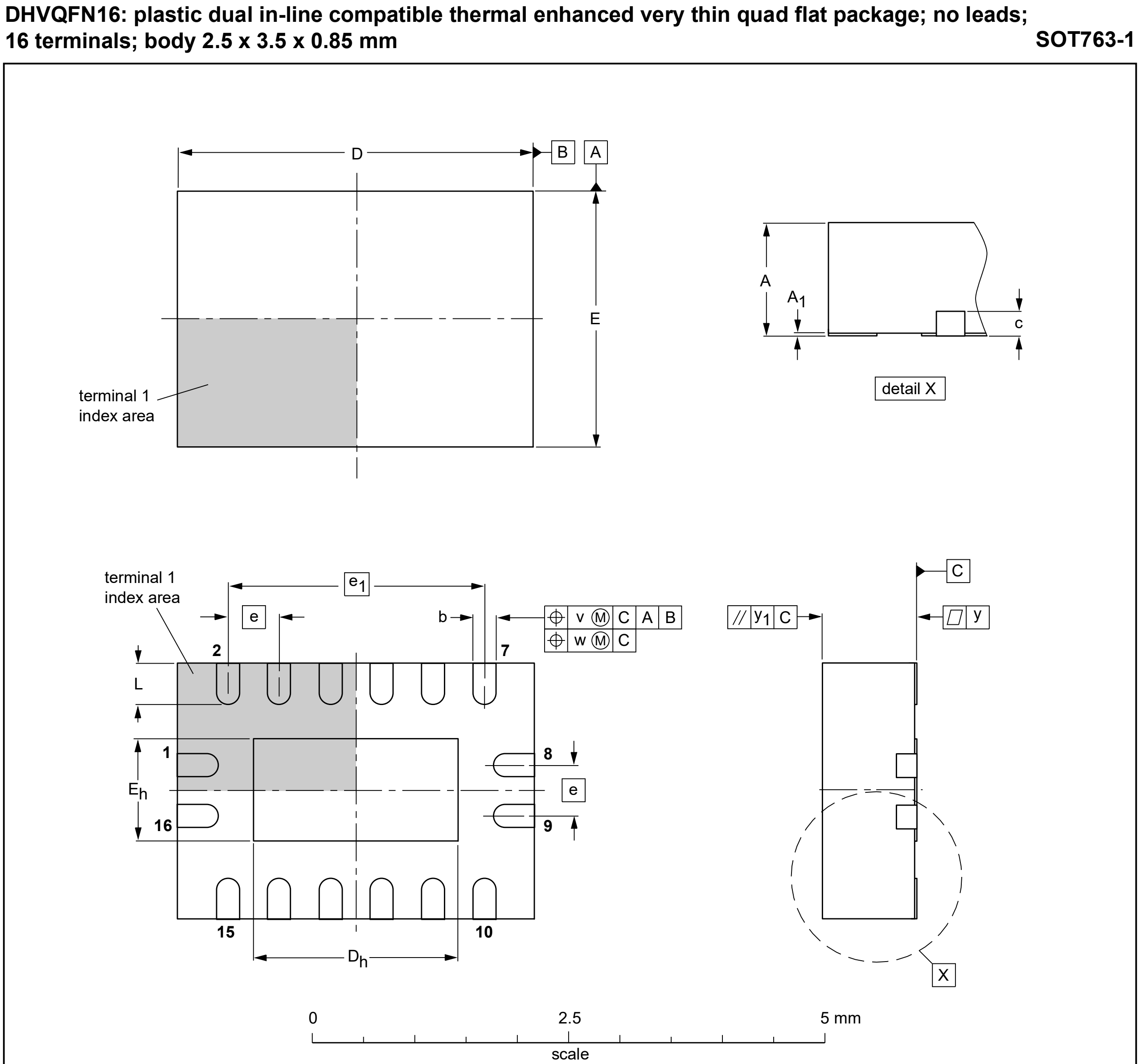

DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 15. Package outline SOT763-1 (DHVQFN16)

15. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

16. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NMUX1309 v. 1.2	20240416	Product data sheet	-	NMUX1309 v. 1.1
Modification	• Section 7.1: Pin configuration drawing of the SOT403-1/TSSOP16 package corrected. (Errata)			
NMUX1309 v. 1.1	20240221	Product data sheet	-	NMUX1309 v. 1
Modification	• Fig. 10: Errata. • Section 5: added.			
NMUX1309 v. 1	20240118	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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